

Recent Progress in Superconductive Digital Electronics
Part I - Western Contributions
(Overview of the Special Section of IEICE Transactions on Electronics,
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Abstract- This overview (Part I) contains highlights of articles contributed by western authors to the Special Section of IEICE Transactions on Electronics, vol. E91-C (March 2008). Included are reflections on how to bring superconductive digital electronics (SDE) to the market place, a global overview of past, present and future of SDE, a view on SDE (termed fluxonics) and superconductive electronics effort in Europe, and two status reports: (1) on RSFQ (Rapid Single Flux Quantum) baseband digital processing for wireless telecommunication, and (2) on superconductor digital-RF receiver systems. Conclusions endorsed by all authors summarize the status of SDE technology, and directions of work still needed for its technical and economic fruition.

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I. INTRODUCTION

The Japanese *IEICE Transactions on Electronics*, devoted a Special Section of their March 2008 issue (vol. E91-C, see [A41](#)) to superconductive digital electronics (SDE). This special section was guest-edited by Dr. Shinya Hasuo of ISTECH, a well-known expert on the topic and, in the past two decades, the leader of the prominent SDE effort at Fujitsu [1]. The Special Section contains five articles by Western contributors, who are the authors of this brief overview (Part I), and seven articles describing the Japanese work, which are overviewed by Th. Orltapp and H. Uhlmann (Part II, see the following

article, below). Their overview of Japanese work was authorized by Dr. Hasuo and the individual Japanese authors, who also provided a few figures highlighting their work.

Overall, the Special Section provides a good worldwide overview of the status of the field in 2007 and deserves attention of readers interested in the field of SDE. Unfortunately, the *IEICE Transactions on Electronics* journal is not readily accessible in Europe, because many institutional libraries do not subscribe to it. Access to the full text of articles is not possible without subscription. Therefore, the News Forum took the initiative to invite brief overviews highlighting these articles and to offer direct e-mail links to individual authors, who are willing to provide hardcopy reprints on request (click on author's name in the text or in the list of references). To provide enhanced visibility, the Western and Japanese contributions are highlighted together, as sections of this and the following review article. Individual highlights are presented in the order of articles in the IEICE Special Section.

II. BRINGING SUPERCONDUCTOR DIGITAL TECHNOLOGY TO THE MARKET PLACE

[Martin Nisenoff](#) (Nisenoff Associates, formerly of US Naval Research Laboratory, USA) discusses the possible application areas for SDE beyond special instrumentation (for, *e.g.*, metrology), and emphasizes the following, which he considers to be the most promising: (a) devices and circuits based on counting flux quanta, such as analog-to-digital converters (ADCs) of performance unattainable in semiconductor technology, (b) medium-sized computers where power management is critical, and (c) very large (serial) supercomputers [2]. In these areas, SDE can provide the “ultimate” performance in terms of lowest power dissipation, very high switching, counting or computation speed, very low attenuation and low-dispersion transmission lines, and, generally, the quantum mechanical nature of the technology. Subsequently, the author summarizes what he believes would be necessary to successfully introduce single flux quantum technology into the market place. Today, penetration of the market place by SDE is still as elusive as it ever was, in spite of the intellectual brilliance of this technology. While the author quotes an observation from a different field of technology that “the brilliance of a new technology should not take precedence over the market case”, he, unfortunately, cannot liberate himself from the fascination by that brilliance. The pre-conditions for success in the market include, in addition to a viable commercial target (the importance of which should not be minimized), the availability of a suitable fabrication infrastructure, suitable closed/cycle cryogenic refrigeration (mechanical cryocoolers transparent or invisible to the end user) and packaging, a competent team of experts (both researchers and engineers), and, extremely important, the availability of adequate and stable funding.

III. SUPERCONDUCTOR DIGITAL ELECTRONICS PAST, PRESENT AND FUTURE

[Ted Van Duzer](#) (Univ. of California at Berkeley, USA) provides a general overview of superconductor digital technology worldwide beginning with materials defining the

Josephson junction and integrated circuit technology [3]. The only reliable technology is still that of niobium circuits and tunnel junctions with Al_2O_3 barriers, which requires cooling to around 4 kelvin. In spite of intense worldwide efforts in the past decade, the high- T_c junction technology still does not provide the necessary parameter control and sufficiently narrow spreads to permit large and very large scale circuit integration (LSI and VLSI).

After a brief historical sketch of the voltage-state logic, the first approach pursued and demonstrated during the IBM Josephson project [4], but largely abandoned by the middle of 1990s due to its limitations, the Single-Flux-Quantum (SFQ) logic and current approaches to memory are discussed in the rest of the article. Principles of this pulse-based logic, in its original embodiment as RSFQ (now the acronym for Rapid SFQ) [5,6] are reviewed, and milestones of RSFQ development presented.

To date, the most ambitious worldwide effort has been the one in the US, initiated in 1992, which was directed towards the goal of advancing the state of digital computing beyond the CMOS-based technology. It culminated in the project on petaflop computing using a hybrid technology multi/threaded (HTMT) architecture and included an RSFQ processor. That rather large effort was curtailed early in this decade, but, due to the suitability for serial computing, it remains of interest to potential users until present [7]. The suspended project produced still unsurpassed advances towards a fabrication technology with tunnel junction critical current density up to 20 kA/cm^2 , and a partially successful demonstration of a 20 GHz 8-bit processor chip FLUX-1R containing over 60 thousand junctions [8].

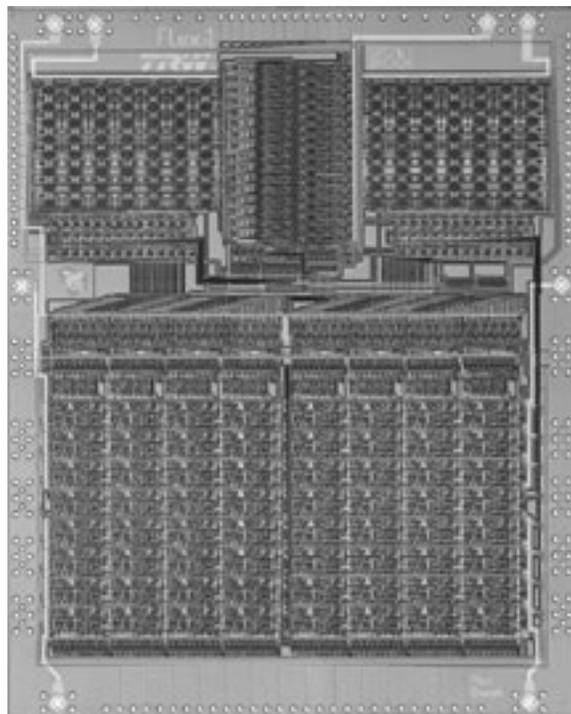


Fig. 1. Photograph of the Flux-1 chip, developed as part of HTMT project [8].

Figure 1 shows the photograph of this processor chip. One important finding was that the limitations of the present fabrication technology (especially the defect rate per chip) will necessitate more than one chip for the processor, with chip interconnections being made through a superconducting MCM (multichip module). A related large-scale US project on a switch for very high data rate throughput used a 128 x 128 self-routing crossbar architecture [9]. After the termination or severe curtailing of these US efforts, analogous, but more cautious and gradual, projects were pursued in past and current Japanese programs, whose recent achievements are highlighted in Part II.

The main weaknesses of the SFQ/RSFQ technology are the extreme difficulty of attaining VLSI level of integration, lack of random-access memory with speed adequately close to the speed of the logic circuits, susceptibility to flux trapping and the destructive effect of trapped flux on the bit error rate (BER), *etc.* These are especially forbidding when high-end computing is contemplated. A possible solution to the memory problem could be hybrid memory pioneered by the author's group. Its concept dates back to 1993 [10]. The memory core, drivers and decoders are in CMOS technology, which can be fabricated with high cell densities, while the bit/line detection is done with Josephson devices. Figure 2 shows the current version of the conceptual block diagram of the hybrid memory being developed at Berkeley with collaboration of Yokohama National University [11].

For the future, the author presents a wish list and some suggestions for directions to take. The list includes a technology with junction tunneling current density, j_c , at 20 kA/cm², and parameter spread < 1-2% over the chip, more complete CAD tools, more emphasis on architecture suitable for RSFQ circuits, professional (rather than university-based) design teams, hybrid Josephson-CMOS memory, interconnect switches for the many processor and memory chips, high-current power supplies avoiding magnetic flux generation, *i.e.*, a radical solution to flux trapping and BER limitation, and, finally, adequate solutions to multi-chip packaging and interfacing with higher-temperature circuitry.

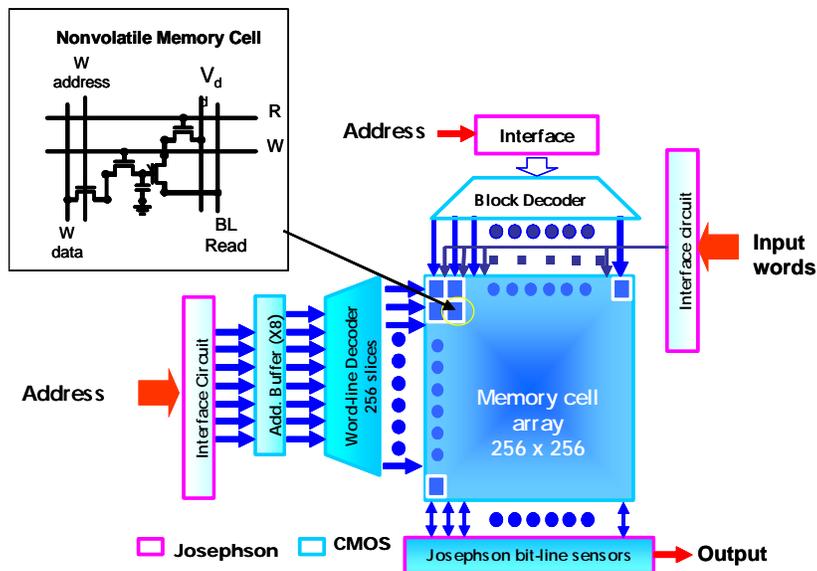


Fig. 2. Block diagram and nonvolatile cell of the hybrid memory, including reading and writing. [11].

IV. FLUXONICS AND SUPERCONDUCTING ELECTRONICS IN EUROPE

[Horst Rogalla](#) (University of Twente, the Netherlands) characterizes briefly the European project structures and the approaches to continuing effort in the field, which evolved in Europe without significant funding concentrated on major technological goals comparable to the past HTMT petaflop computing project in the US or to major Japanese government-sponsored programs [12]. Author's comments encompass also to some extent electronics other than digital, and even quantum computing is mentioned. The Fluxonics network society is the European solution to the foundry problem (thus far with the junction tunneling density still at 1 kA/cm^2 , see Forum paper [RN4](#)).

Highlighted are selected examples of more successful SDE projects, which have been performed in Europe, such as the low- T_c Digital Signal Processor of Chalmers University (the topic of the next section), and very small high- T_c circuits such as a σ - δ (sigma-delta) modulator, and the unfinished hybrid second-order modulator, *etc.* (subject of the past SUPER-ADC EC project), which could be practical even with the limited control of junction parameters and spreads [13]. Figure 3 shows the block diagram of the 2nd order σ - δ modulator; although adversities prevented its completion, it remains a goal worthy of industrial implementation. Figure 4 shows the photo of the pulse stretcher chip containing 16 junctions. Its function is to stretch output pulses for amplification by a broadband cooled InP amplifier.

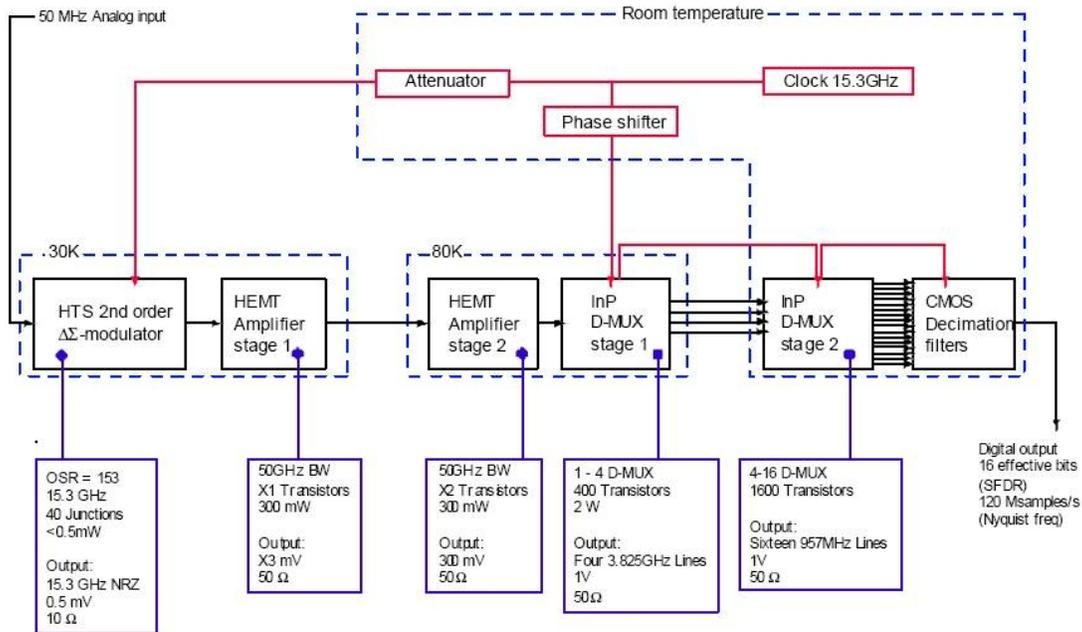


Fig. 3. The block diagram of the 2nd order σ - δ ADC, subject of the past SUPER-ADC EC project.

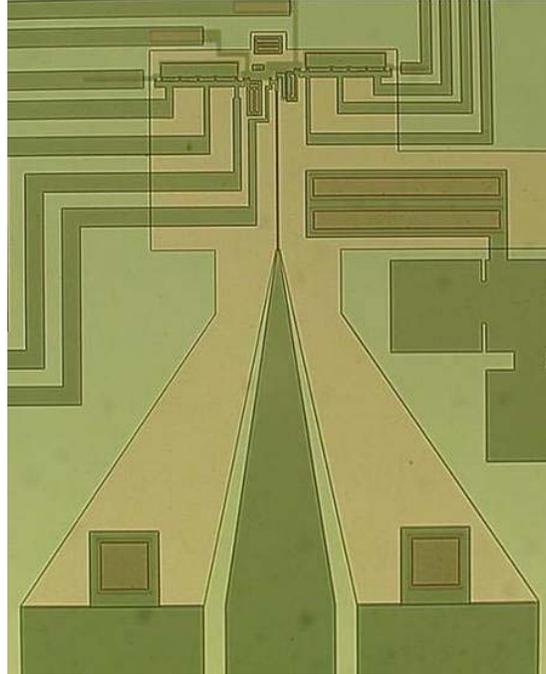


Fig. 5. Photo of the high- T_c pulse stretcher of the 2nd order σ - δ modulator.

The author emphasizes also the beneficial effect of European networks (such as the past SCENET and Fluxonics) on the development and availability of European cryocoolers suitable for SDE. For cooling of very small digital circuits utilizing high- T_c junctions, he advocates implementation of miniature micro-machined Joule-Thomson cryocoolers with sorption compressors, which are under development at Twente in cooperation with the European Space Agency and should provide cooling at about 40 kelvin up to the mW range, suitable for small high- T_c circuits [14].

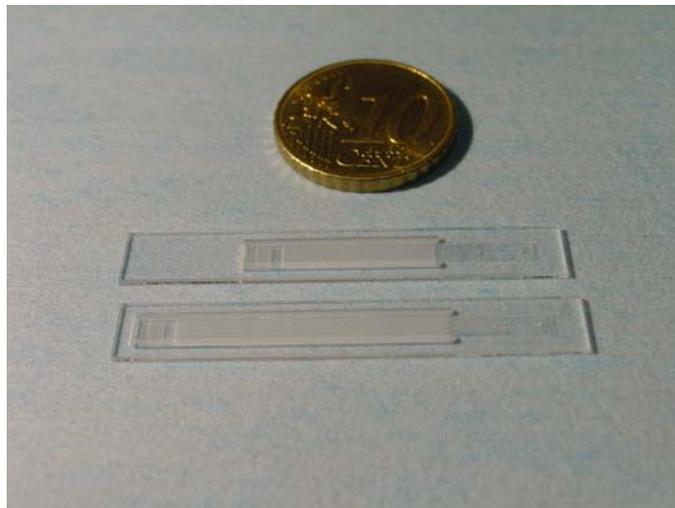


Fig. 5. Two microcooler cold stages fabricated at Twente.

Small high- T_c digital circuits would be used with cold semiconductor electronics as shown in Figure 3. The cold stage of a cryocooler for the cooling of this cold semiconductor electronics to, *e.g.*, 80K would be a suitable platform for a microcooler that could reach 40K needed for the HTS circuit. It would perfectly fit in size and would easily give the necessary cooling power for the cooling of both the HTS circuit and its connections to an 80K stage. An industrial spin-off company has been organized to further pursue the development and to fabricate and market microcoolers [15].

The author's wish list is qualitatively similar to that of Van Duzer (Section IV) and includes goals for the VLSI integration level, enhanced speed and clock rates, hybrid technologies, improved interfaces to room-temperature devices and cryo-packaging.

V. RSFQ BASEBAND DIGITAL SIGNAL PROCESSING

[Anna Herr](#) (Chalmers University of Technology) outlines progress in the development of the RSFQ Digital Signal Processor (DSP) for baseband processing in modern telecommunication systems [16]. The RSFQ DSPs open a very rich application niche where superconducting circuits do not face competition from conventional approaches. The performance gain in the telecommunication systems is so significant, that one would expect quite a large commercial market for the RSFQ DSP once there is proof of existence in the form of the first prototype.

Due to the necessity of cooling to 4 kelvin, application of RSFQ technology is only reasonable for tasks that are impossible or ineffective using semiconductors. For DSPs this points to problems that cannot be effectively parallelized. The general class of DSP problems that falls into this category is *adaptive filtering*. The applications of adaptive filters are numerous and include system identification, channel equalization, and signal prediction. Perhaps the most strongly motivated application for adaptive filtering is interference cancellation in modern wireless communication systems. Signal detection in an interference-limited system is exactly where currently existing cellular wireless networks show a disparity between what is theoretically possible and what is technically realizable using conventional technology. It is important to note that the adaptive filtering solves the central problem of signal detection that simply cannot be addressed by other system improvements such as signal coding or advanced receiver hardware.

All adaptive algorithms are recursive and the main problem with practical implementation of the recursive algorithms in telecommunication is the required computational complexity and short latency. Ultra-fast switching speed of superconducting digital circuits makes possible the realization of DSPs with performance unattainable by any other technology. Based on RSFQ logic, these integrated circuits are capable of delivering high computation capacity up to 30 GOPS on a single processor and very short latency of 0.1 ns. Even with the moderate integration density available in today's fabrication technology, the RSFQ DSPs can execute complex recursive algorithms independent of the communication standard, for both uplink and downlink.

The article presents the current (2007) status of the development of the RSFQ baseband DSP at Chalmers. The chosen architecture of the RSFQ DSP is scalable in various ways: with respect to memory, bit-precision and speed. Component design, test results, and future development of the complete systems including cryopackaging and

CMOS interface are reviewed. Figure 6 is a photograph of the chip of the main component of the DSP: the 4x4 two's complement parallel multiplier comprising 2800 Josephson junctions. It was fabricated at HYPRES using the 4.5 kA/cm² process. Paper [ST36](#) contains a short up-to-date description of the project ongoing at Chalmers.

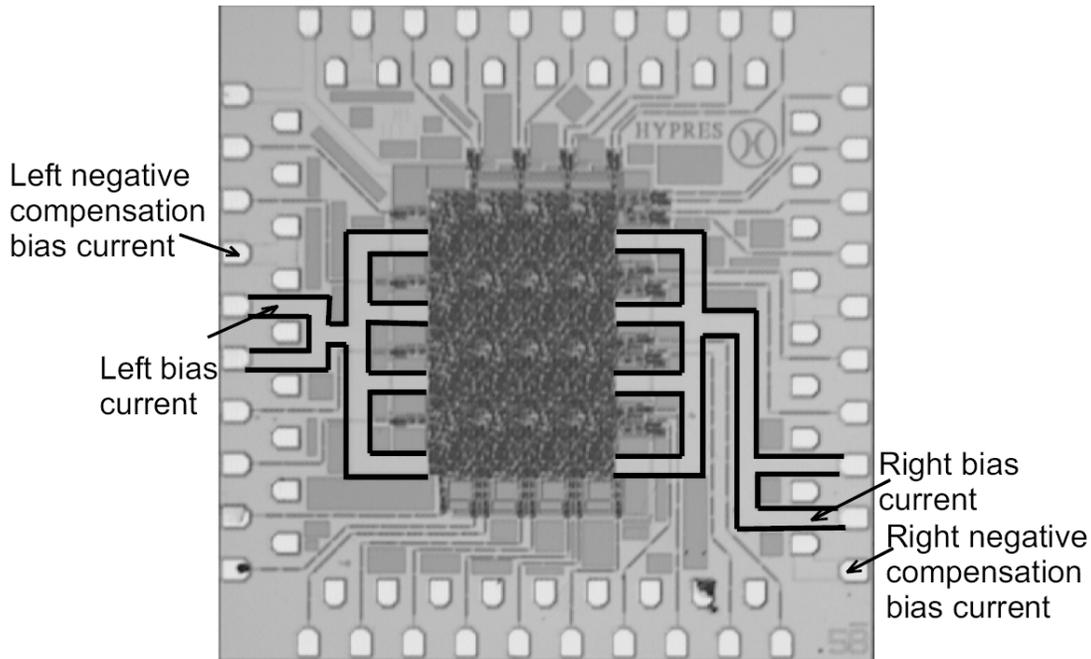


Fig. 6. Photo of the main component of the RSFQ DSP developed at Chalmers: 4x4 two's complement parallel multiplier. There are 2800 Josephson junctions on the chip [17].

VI. SUPERCONDUCTOR DIGITAL-RF RECEIVER SYSTEMS

[Oleg Mukhanov](#) *et al.* (HYPRES, Inc.) outline the development and demonstrations of complete digital receiver prototype systems, implementing Digital-RF architecture capable of directly digitizing wide-band RF signals from kHz to GHz [18]. The heart of these systems is a low-temperature superconductor integrated circuit chip (All Digital Receiver, ADR), consisting of either low-pass or band-pass ADC (analog to digital converter) modulator and digital channelizer processors. These ADR systems were assembled following the hybrid-technology-hybrid-temperature (ht²) system integration approach.

The authors integrated digital receiver low-temperature superconductor chips with commercial 4 kelvin cryocoolers (Sumitomo), and equipped them with room-temperature interface electronics controlled by graphical user interface. Using one of these ADR systems, an X-band ADR (XADR), live operation in communicating with the XTAR satellite was demonstrated. The XADR chip has been fabricated using the HYPRES 4.5 kA/cm² Nb-AlO_x-Nb process, contains ~11000 Josephson junctions and operates at ~30

GHz while packaged on a cryocooler. This is the fastest complex digital RSFQ IC fully operational in relevant application environment.

The ADR was integrated with conventional digital modems and successfully passed data and video. Figure 7 presents a composite block diagram of this experiment, which demonstrated the relative maturity of superconductor Digital-RF technology. However, such Digital-RF receiver demonstrations are just initial steps toward an All-Digital-RF Transceiver (ADT) for future communications systems. The overall goal of the ADT is to provide direct RF digitization of the whole bandwidth for all incoming signal carriers from the antenna and consolidate all digital-RF distributions from the antenna into a single all-digital software-defined platform from RF to baseband. In terms of increased capability, this will allow one to have programmable and flexible multi-band multi-mode communications across multiple RF sources simultaneously. In terms of increased performance, this will allow one to have greater gain over noise temperature improvement on the receive-side and greater power efficiency on the transmit side, due to the intrinsically low noise temperature and direct digital-RF processing using superconducting digital circuits. In terms of cost, this should eliminate significant amount of legacy equipment, such as intermediate frequency (IF) cabling, analog RF switch panels, analog IF up/down converters, and analog IF modems.

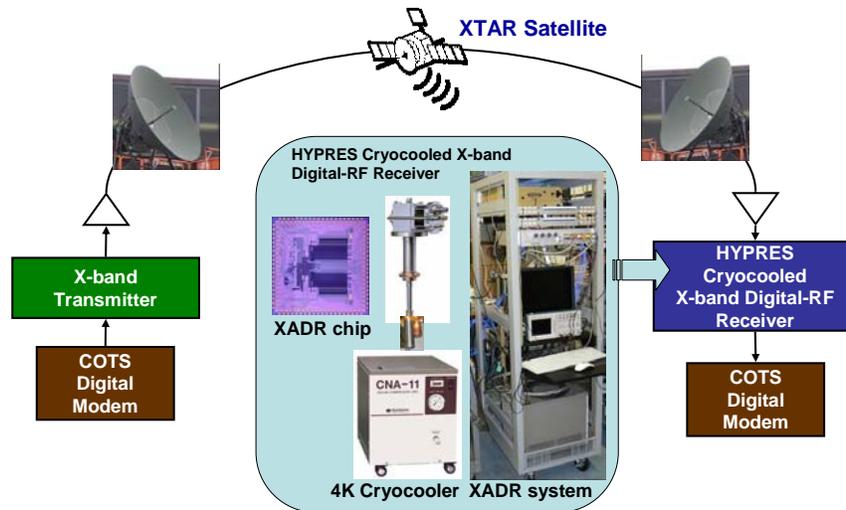


Fig. 7. The Cryocooled X-band All-Digital Receiver (XADR) system demonstration with live XTAR satellite. Digital data including video were transmitted over satellite and received by HYPRES XADR system by directly digitizing X-band (7.6 GHz) satellite downlink signal with high sampling rate clock. The HYPRES system was integrated with commercial digital modems, transmitter and dish antenna.

VII. CONCLUSIONS

These conclusions represent the consensus of all authors. The general arguments for SDE remain: (1) lower power consumption on chip - by three orders of magnitude, and (2) data and signal processing rates between 10 and 100 GHz, an order of magnitude

higher than those of conventional technology. At present, only the Nb/Al₂O₃/Nb logic circuit technology, which requires cooling to around 4 kelvin, is suitable for fabrication of SFQ/RSFQ circuits with complexity up to several thousand gates per chip. Advanced processing technology will allow more complex circuits on the chips. Still larger circuits must use the multi/chip module (MCM) technique. High- T_c technology, permitting one to operate at 30 to 40 kelvin is presently not usable for SFQ fabrication, except for very small circuits with junction counts below 50 or so, such as samplers. Only technological breakthroughs and the infusion of sizable and stable financing could change this situation and enable true VLSI on chip, at least in low- T_c technology.

Hybrid technologies, *e.g.*, involving CMOS, should be pursued as this approach might alleviate the memory problem. Further work is needed on inter-chip communication, on high current delivery to the chips without flux trapping, on the related issue of magnetic shielding, on two-way hybrid interfaces with room temperature circuitry, and on integration with suitable 4 kelvin cryocoolers, which also need optimization. Architectures most suitable for SFQ circuitry should be further explored.

Currently, low-power signal and data processors and switches with speed equivalent to 20 to 40 GHz clock frequency appear realistic. This technology status makes possible demonstrations and various niche applications in (predominantly military) communications, and perhaps also in signal processing and switching for commercial wireless networks. Were it possible to penetrate the commercial wireless communication community, a sizable niche market could develop. Massive serial computing and data switching appears possible in principle, but would require a dramatic increase in the level of resources, both manpower and funding, compared to what this technology enjoyed in the past. This would lead to the creation of the necessary professional infrastructure and thus to the removal of existing technological obstacles.

REFERENCES

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- [1] Guest Associate Editors were: M. Maezawa (AIST), Y. Mizugaki (Univ. of Electro-Communication), H. Myouren (Saitama Univ.), K. Saito (Hitachi, Ltd.) and S. Yorozu (NEC).
 - [2] [M. Nisenoff](#), "Bringing Superconductor Digital Technology to the Market Place", *IEICE Trans. Electron.* **91E-C**, 252-259 (2008).
 - [3] [T. Van Duzer](#), "Superconductor Digital Electronics Past, Present and Future", *IEICE Trans. Electron.* **91E-C**, 260-271 (2008).
 - [4] Special Issue on Josephson Computer Technology, *IBM J. Res. Dev.* **24**, No. 2 (1980).
 - [5] K.K. Likharev, O.A. Mukhanov, V.K. Semenov, "Resistive single flux quantum logic for the Josephson-junction technology", in *SQUID '85*, H.D. Hahlbohm and H. Lübbig, eds., W. de Gruyter, Berlin 1985, pp. 1103-1108.
 - [6] K.K. Likharev, V.K. Semenov, "RSFQ logic/memory family: a new Josephson junction technology for sub-terahertz clock frequency digital systems", *IEEE Trans. Appl. Supercond.* **1**, 3/28 (1991).
 - [7] Superconducting Technology Assessment, NSA Office of Corporate Assessment, August 2005; <http://www.nitrd.gov/pubs/nsa/sta.pdf>.
 - [8] P. Bunyk, M. Leung, J. Spargo, M. Dorojevets, "FLUX/1 RSFQ microprocessor: physical design and test results", *IEEE Trans. Appl. Supercond.* **13**, 433-436 (2003).
 - [9] F. Bedard, "128 x 128 superconducting crossbar switch, presented at the Intl. Workshop on Low-temperature Superconducting Electronics", Sept. 1996 (unpublished).
 - [10] U. Ghoshal, H. Kroger, T. Van Duzer, "Superconductor/semiconductor memories", *IEEE Trans. Appl. Supercond.* **3**, 2315-2318 (1993).
 - [11] T. Van Duzer, Private communication, 7/7/08.

- [12] [H. Rogalla](#), "Fluxonics and superconducting electronics in Europe", *IEICE Trans. Electron.* **91E-C**, 272-279 (2008).
- [13] A. Roussy, S. Karthikeyan, I. Oomen, T. Ortlepp, E. Sujiono, A. Brinkman, H. Rogalla, "HTS pulse-stretcher and second-order modulator: design and first results", *IEEE Trans. Appl. Supercond.* **15**, 457-460 (2005).
- [14] P.P.P.M.Lerou, G.C.F. Venhorst, C. Berends, T.T. Veenstra, M. Blom, J.F. Burger, H.J.M.ter Brake, H. Rogalla, "Fabrication of a micro cryogenic cold stage using MEMS-technology", *Journal of Micromechanics and Microengineering*, **16**, 1919-1925 (2006).
- [15] Kryoz Technologies B.V., Drienerlolaan 5, Gebouw Hogekamp, 7522 NB Enschede, The Netherlands, www.kryoz.com and/or www.kryoz.nl.
- [16] [A.Y. Herr](#), "RSFQ baseband digital signal processing", *IEICE Trans. Electron.* **91E-C**, 293-305 (2008).
- [17] I. Kataeva, H. Engseth, A. Kidyarova-Shevchenko, "New design of an RSFQ parallel multiply-accumulate unit", *Supercond. Sci. Technol.* **19**, S381-S386 (2006).
- [18] [O.A. Mukhanov](#), D. Kirichenko, I.V. Vernik, T.V. Filippov, A. Kirichenko, R. Webber, V. Dotsenko, A. Talalaevskii, J.C. Tang, A. Sahu, P. Schevchenko, R. Miller, S.B. Kaplan, S. Sarwana, D. Gupta, "Superconductor digital-RF receiver systems", *IEICE Trans. Electron.* **91E-C**, 293-305 (2008).