A Robust and Tree-Free Hybrid Clocking Technique for RSFQ Circuits – CSR Application

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***Abstract*— RSFQ technology promises to achieve the ultra-low power and high-speed computing needed for future exascale supercomputing systems. One of the biggest challenges impeding the application of this technology, however, is the ultra-high-speed clocking of large scale RSFQ circuits. The clocking complexity is aggravated by algorithmic loops and generic complex pipelines, whose presence is inevitable in large scale systems. This paper presents a new clocking technique, comprised of synchronized hybrid clock loops, whose frequency is intrinsically determined by the clock architecture. This tree-free scheme reduces the area, power, and complexities associated with traditional clock distribution networks. A SystemVerilog model of the architecture is built to quantify the benefits and prove the feasibility of the proposed scheme. As an example, for a 32-gates circular shift register (CSR), under a model of moderate local and global variations, our experimental results show up to 93% yield improvement at the same cycle time compared to zero-skew tree clocking.**

***Keywords (Index Terms)* — RSFQ Clocking, RSFQ timing, circular shift registers, hybrid clocking, clock distribution networks.**

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