Lowering Latency in High-Speed Gate-Level-Pipelined Single Flux Quantum Datapath Using Interleaved Register File

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***Abstract*—We successfully demonstrate the 50-GHz operation of a microprocessor datapath based on single-flux-quantum logic with a gate-level pipeline structure. The microprocessor datapath features a register file (RF), an arithmetic logic unit (ALU), and a long feedback loop that connects these components. Interleaved data-processing is introduced in the RF so that the operating frequency of the RF is half that of the ALU. This makes the timing constraints eased; thus, we can reduce the number of pipeline stages used for timing adjustments. We designed a 4-bit datapath using the proposed technique, targeting 50-GHz operation. Compared to the conventional datapath, the total number of pipeline stages and the latency decreased from 49 to 24 and from 980 to 760 ps, respectively. We fabricated test chips using the AIST Nb 9-layer 10-kA/cm^2 process, and performed successful on-chip high-speed tests. In addition, our preliminary experiments suggest that we can expect 1.6-fold higher throughput at an 80-GHz clock frequency, at the cost of a 10% increase in latency.**

***Keywords (Index Terms)*—Bit-parallel processing, gate-level-pipeline, microprocessor, single-flux-quantum logic**

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