60-GHz Single Flux Quantum Pulse Transfer Circuit for Serial Biasing

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***Abstract*—Serial Biasing (SB) is a technique to reduce the total DC bias current of Rapid Single Flux Quantum (RSFQ) circuits by partitioning a design into several islands with isolated grounds and sequential biasing. In this paper we focus on the design of a driver-receiver pair (DRP) to transfer pulses between islands that are galvanically isolated for pulse streams. We discuss both DRP itself and the structure for its testing, that comprises several DRPs connected in series, on-chip pseudo random binary sequence (PRBS) generator for circuit stimulation, and HF output interface. We use the layout of DRPs' chain as an example to illustrate the advantage of the grapevine (GV) approach, introduced earlier, to manage the bias current flowing into and out of an island. The GV current management technique is analyzed by both electromagnetic simulations and measurement, compared, and contrasted with the so-called 'straightforward' (SF) approach. The maximum operational frequency for SF test structure was 10 GHz with zero margins for the SB current. Measurements of the GV structure at 10 GHz demonstrated BER of 10-12 with ±5.8% margins for SB current. We observed the correct operation of the 5-island DRP chain up to 60 GHz using the grapevine approach for SB current management. All chips were fabricated at MIT Lincoln Laboratory using SFQ5ee fab node.**

***Keywords (Index Terms)*—RSFQ, serial biasing, current recycling, grapevine**

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