Low-Cost Fan-Out with SFQ Cell Labeling

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***Abstract*—Superconductor electronics (SCE) promise computer systems with orders of magnitude higher speeds and lower energy consumption than their complementary metal-oxide semiconductor (CMOS) counterpart. At the same time, the scalability and resource utilization of superconducting systems are major concerns. Some of these concerns come from device-level challenges and the gap between SCE and CMOS technology nodes, and others come from the way Josephson Junctions (JJs) are used. Towards this end, we notice that a considerable fraction of hardware resources are not involved in logic operations, but rather are used for fan-out and buffering purposes. In this paper, we ask if there is a way to reduce these overheads; propose the use of JJs at the cell boundaries for improved fan-out; and establish a set of rules to discretize critical currents in a way that is conducive to this reassignment. Finally, we demonstrate the accomplished gains through detailed analog simulations and modeling analyses. Our experiments indicate that the introduced method leads to a 48% savings in the JJ count in a tree with a fan-out of 1024, as well as an average of 43% of the JJ count for signal splitting and 32% for clock fan-out in ISCAS'85 benchmarks.**

***Keywords (Index Terms)*—Superconductor electronics, SFQ, design abstraction, design methodology**

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