In-situ Fabrication of Topological-Superconducting Hybrids

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***Abstract*—Majorana platforms comprised of networks of quasi one-dimensional (1D) topological insulator (TI) nanostructures in proximity to s-wave superconductors might open the door towards topological quantum computation. To assure a high quality of such platforms, fabrication under UHV conditions is mandatory. In this work, we introduce two in-situ techniques, which when combined form the key to scalable Majorana platform fabrication. 1D TI nanostructures can be realized by "selective area growth". Therefore, a thin layer stack of Si_3N_4 and SiO_2 on top of a Si (111) surface was patterned by electron beam lithography and reactive ion etching. Topological insulator (TI) thin films grew selectively in as defined trenches on top of the exposed Si (111) surfaces via molecular beam epitaxy. Thereby, later fabrication processes for mesa definition under ambient conditions have been avoided. "Stencil lithography" on the other hand assures clean and highly transparent interfaces in between TI and superconductive thin films. We established a process, which allows the fabrication of Josephson junctions via stencil lithography under UHV conditions, again by means of molecular beam epitaxy. Our junctions show large I_CR_N products and signatures, which indicate transport mediated by gapless Andreev bound states, so called Majorana bound states.**

Keywords—Topological Insulators; Majorana Zero Modes; Stencil Lithography; Selective Area Growth

I. Introduction

Majorana Zero Modes (MZMs) are expected to obey non-Abelian exchange statistics and therefore promise to facilitate fault-tolerant quantum computation [1,2]. These exotic Zero Modes were predicted to exist in superconductors (SC) with partly p-wave pairing-potential. Such superconducting p-wave correlations are induced in topological insulator surface states by the proximity effect of a conventional s-wave superconductor.

Proposals suggest networks of 1D TI nanostructures or wires in proximity to superconductors for realizing topological quantum bits (qubits) [3]. Disadvantageously, the surfaces of topological insulators tend to oxidize once exposed to ambient conditions. To assure the preservation of the pristine Dirac surface states, capping layers of different materials have efficiently been used [4]. One way to provide a protective passivation layer is to deposit 2 nm of Al on top of the thin film right after the growth of the TI [5]. This thin Al-layer will oxidize subsequently and protect the surface of the TI. For the realization of nm-sized ribbons the structures need to be defined before TI thin film deposition. Within this work, we are presenting a method how to selectively grow such nanostructures in-situ, before deposition of the additional capping layer. The method we are introducing is highly scalable and allows to grow arrays of such nanostructures of any lateral geometry and precisely aligned to each other.

A problem related to the in-situ Al-capping is the high stability of the native Al-oxide (AlO_x). Removing the AlO_x and other hard-capping layers thoroughly turned out to be challenging [6]. Residual oxides at the interface or damage to the TI thin film during removal of the capping layer usually result in low interface transparencies. By defining and fabricating superconductive contacts before deposition of a global dielectric, one could avoid the removal of the capping layer. A promising way to define contacts in-situ is stencil lithography [7]. In the second part of this work, we are presenting first results of superconductive Nb grown on top of our TI thin films via stencil lithography. Combining this method and the technique of selective area growth paves the way to fabricate desired topological insulator-superconductor hybrids of high quality and scalability.

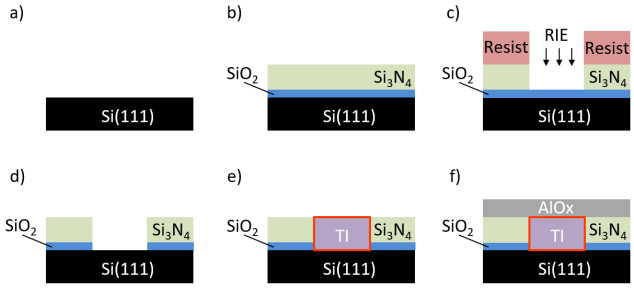

Fig. 1: Substrate fabrication and selective growth: a) Clean Si. b) SiO_2 and Si_3N_4 deposition. c) Nano-patterning (EBL and RIE). d) HF dip. e) Selective TI growth. f) In-situ Al-capping and oxidation at atmosphere.

II. Selective Area Growth

In a first step the upper 6 nm of a cleaned Si (111) substrate (Fig. 1a) have been thermally oxidized. Then, a 25 nm thick layer Si_3N_4 has been deposited (Fig. 1b). After defining

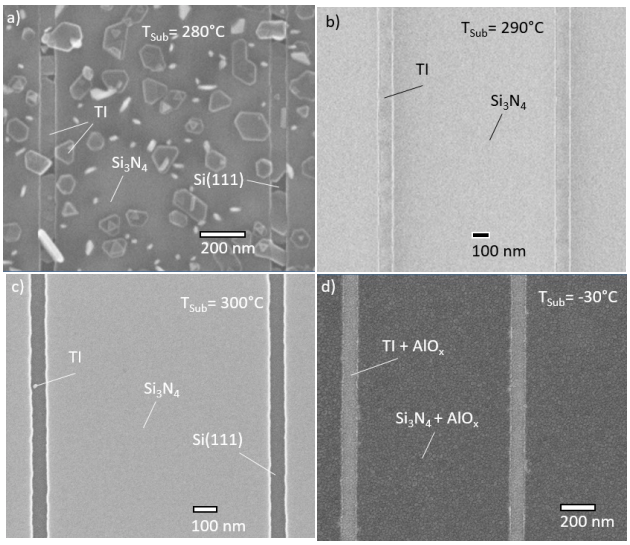

Fig. 2: Selective area growth of topological insulators. a) T_{Sub} = 280 °C: TI grows in Si trenches and on top of Si_3N_4. b) T_{Sub} = 290 °C: TI growth selectively only on Si. c) T_{Sub} = 300 °C: TI growth nowhere. d) Al capping deposited on top of filled trenches at T_{Sub} = −30 °C.

rectangular structures with widths down to 50 nm via standard electron beam lithography (EBL), the trenches were transferred into the Si_3N_4 layer via reactive ion etching (RIE) (Fig. 1c). A final dip in diluted HF solution (1%) for 2:15 minutes, removes the 6 nm of SiO_2 on top of the Si (111) surface inside the defined trenches and passivates the Si((111) surface with hydrogen atoms for ex-situ transport to the MBE system (Fig. 1d).

After removing the protective hydrogen passivation by heating the substrate to 700 °C for 10 min. in the growth chamber, the substrate temperature (T_{Sub}) was set to its growth temperature. Before starting the self-regulated growth of $(Bi_{1-x}Sb_x)_2Te_3$ thin films within the nano-trenches defined, the surface is flushed with Te to saturate the Si dangling bonds. If the growth temperature is set correctly (Fig. 2b), the topological insulator thin film only grows on top of the exposed Si (111) surface and not on Si_3N_4. The selectivity of the TI growth on the silicon surface is only given in a small temperature window below $\Delta T < 20$ °C. If the temperature is too high, nucleation does not take place and TI thin films do not grow on the Si (111) surface nor on Si_3N_4. At T_{Sub} = 300 °C only a single small flake inside one trench on top of Si (111) is observed (Fig. 2c). In case T_{Sub} is too low, the TI will grow inside the trenches, but flakes will grow on top of the Si_3N_4 as well (Fig. 2a). For a substrate temperature of 290 °C we obtain a clean Si_3N_4 and filled trenches.

If the growth is timed right, the Si_3N_4 trenches can be filled to the desired height. While Si and Si_3N_4 protect the bottom and side facets of the nanostructures, respectively, the upper surface is exposed to the vacuum (Fig. 1e). Before taking the sample to ambient conditions, one can deposit 2 nm of Al (Fig. 2d) for the desired AlO_x capping layer. It is known, that these 2 nm will oxidize natively, when taking the sample to air. Alternatively, one can sputter deposit stoichiometric Al_2O_3. In this way, all six surfaces of the selectively grown topological

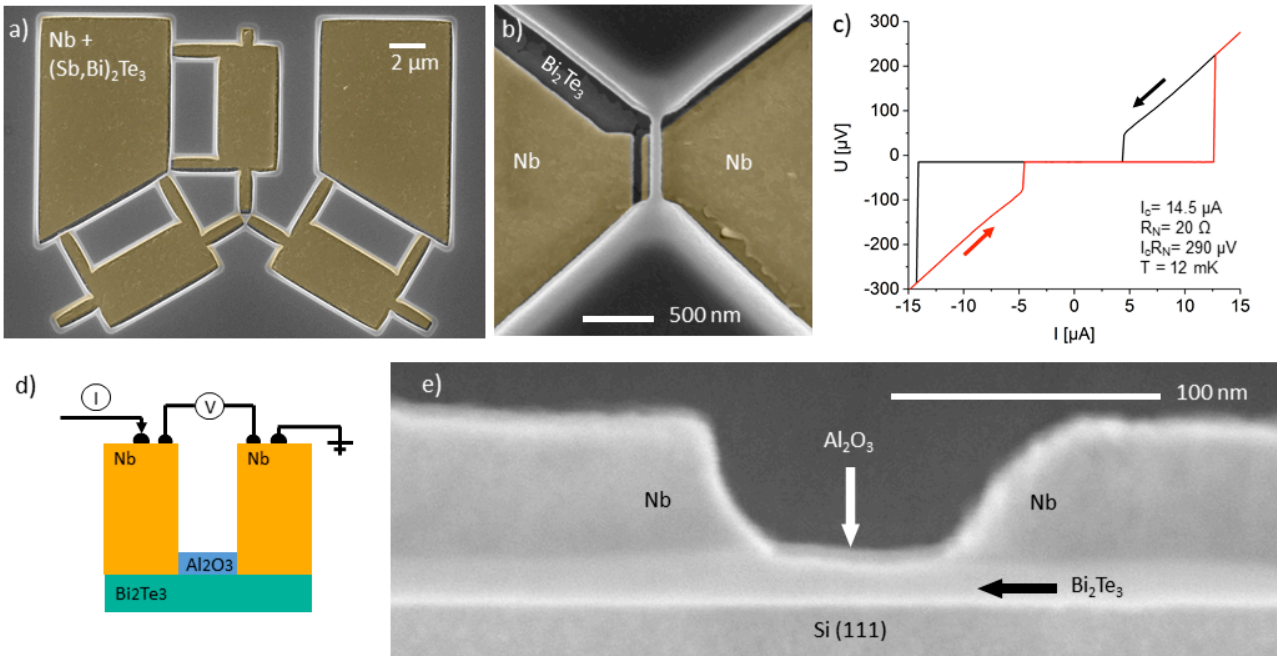

Fig. 3: Stencil Lithography. a) Structured superconductive Nb thin film (golden) in the form of a tri-junction with attached SQUIDs [1]. b) Grown Josephson junction (mask still attached to the substrate). c) I-V curve of an as grown JJ. d) 4 point measurement setup. e) Lamella prepared with focused ion beam: Cross section of as grown JJ with Nb contacts on top of Bi_2Te_3 TI thin film with Al_2O_3 capping layer.

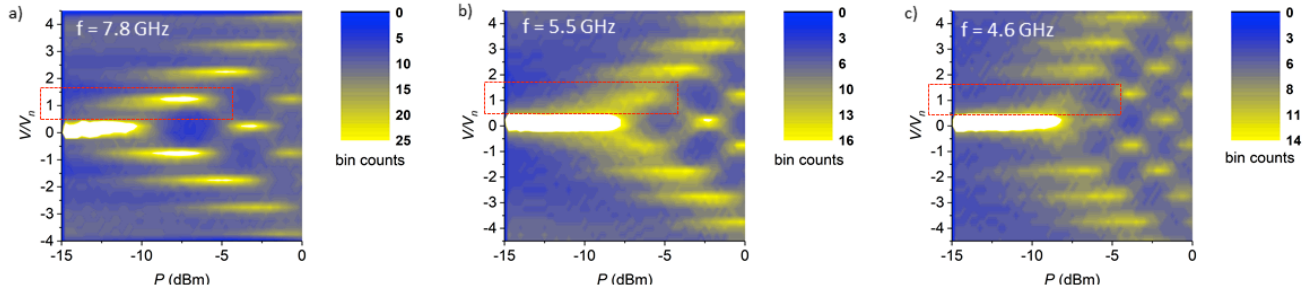

Fig. 4: Shapiro step measurements for three frequencies at 1.5 K: a) For 7.8 GHz all steps are visible. b) First step is attenuated at f = 5.5 GHz. c) Full suppression of the first step for f = 4.6 GHz, indicating a 4π-periodic contribution. The location of the first step is indicated with a red box in each image.

insulator nanostructures are protected from degradation (Fig. 1f). Selective area growth makes it possible to define any lateral geometry of the mesa, without the need of ex-situ mesa fabrication.

III. Stencil Lithography

Instead of a global surface passivation, it is also possible to first use stencil lithography to define superconductive contacts/islands of any shape, still in-situ [8]. In Fig. 3a a superconductive tri-junction with attached SQUIDs is shown. The hybrid device is comprised of a structured Nb thin film on top of $(Bi_{0.06}Sb_{0.94})_2Te_3$. Note that the stencil mask used is still in contact with the substrate. After the deposition of superconductive contacts the whole sample can be capped additionally with 2 nm of Al or a dielectric thin film, to assure that the delicate TI surface is either covered by superconductors or a protective capping layer. The shapes of the superconducting islands shown in Fig. 3a are inspired from [1]. Such superconducting islands have been theoretically proposed for demonstrating braiding experiments with Majorana Zero Modes.

We also fabricated single Josephson Junctions (JJs) on Bi_2Te_3 3D TI thin film with Nb contacts via stencil lithography (Fig. 3b) and performed four point measurements at 12 mK (Fig. 3c). In these transport experiments, we observed high critical currents, up to 14.5 µA, and I_CR_N products of the order of 290 µV. These values are about one order of magnitude higher compared to our previous results on ex-situ fabricated JJs.

Once the junctions are irradiated with an rf-signal, integer Shapiro steps of constant voltage height appear within the I-V curve. For high quality 2D and 3D topological JJs missing Shapiro steps were reported in HgTe [9]. Vanishing odd Shapiro steps are attributed to transport mediated across the junction by a pair of gapless Andreev bound states, so called Majorana bound states.

We also observe the first Shapiro step disappearing in our junctions as soon as we approach the lower GHz regime (Fig. 4). Although, Shapiro step measurements have been carried out on ex-situ fabricated Bi_2Te_3 JJs before, a missing step was never reported.

We attribute the sharp and clean interface in between SC and TI film (Fig. 3e) in combination with the in-situ capped weak link for the high quality of our junction. More information about the stencil technique and the 4π-periodic supercurrent are presented elsewhere [10].

The method of stencil lithography, presented here, allows fabricating devices with a large throughput and a high interface quality. We report on the first observation of a 4π-periodic contribution to a Josephson current in Bi-based topological insulator thin films. These findings emphasize to make use of in-situ techniques to fabricate more complex devices to further investigate Majorana physics in SC-TI hybrids. Combining stencil lithography with the technique of selective area growth allows the in-situ fabrication of very complex hybrid structures, which—due to their scalability—might become highly interesting for future topological quantum computing applications.

IV. Conclusion

In the first part we showed how to fabricate in-situ capped nm-scaled mesa structures comprised of topological insulator thin films. The process is highly scalable and allows for well-aligned networks of nanostructures. Since exposure of the TI to ambient conditions should be avoided, we established another technique that allows deposition of superconductive contacts in-situ via stencil lithography. Nb-contacts fabricated by this method provide highly transparent interfaces and first signatures of 4π-periodic transport in as grown Josephson devices. Combining both methods paves the way to fabricate complex hybrid devices for topological quantum computation.

Acknowledgment

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