A Cooling Platform Powered by Superconducting Tunnel Junctions

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June 30, 2015 (STH32, HP97). Refrigeration below 1 kelvin belongs traditionally to the domain of macroscopic machines, such as adiabatic demagnetization or ^{3}He-^{4}He dilution cryostats. Although being reliable and universal, these systems are often bulky and complicated to operate. Alternatively, one can employ the cooling effect in a Superconductor - Insulator - Normal metal - Insulator - Superconductor (SINIS) junction when such a contact is biased near the superconducting gap. Powered by SINIS coolers, a nonconducting platform can cool mesoscopic devices to their working temperature or it can ultimately replace a dilution unit. This approach offers a simple, light weight cooling solution, especially for spaceborne applications [1].

There are many challenges that hinder an uncompromised demonstration of such a device. First, the SINIS cooler under-performs its theoretical prediction, mainly due to the excessive number of quasiparticles injected from superconducting leads. On the other hand, those devices that would perform well, lack a practical power to handle external loads. Second, when the device dimensions become comparable to the phonon wavelength, a few μm at low temperatures, size effects modify thermal transport properties, especially at the boundary of materials. It becomes increasingly difficult to precisely engineer the thermal transport, especially in the sub-kelvin temperature regime. As a result, one often needs to suppress the thermal conductivity between the cold platform and its environment as effectively as possible. The platform of choice is an amorphous silicon nitride (SiN) membrane, where three dimensional phonons do not exist. This two dimensional structure is then typically perforated so that the center part is suspended only by thin legs. It results in a fragile structure and further manipulation is next to impossible.

Recently, such an electron cooler was developed with a well thermalized superconductor using photolithography and wet etching [2]. At 300 mK, this device has 1 nW cooling power, enough to handle an external load, yet performs outstandingly over a wide range of temperature [3]. Four coolers are placed at corners of a 1 mm $\times$ 1 mm $\times$ 100 nm SiN membrane, see Fig. 1a. The cooled normal metal is thermally connected to the center of the membrane using Cu a cold finger made in a separate lithography step. It is designed so that there is one main cold finger, one middle cold finger, and two outer cold fingers. This onion-like design allows outer cold fingers to precool the inside area and at the same time prevents the external heat load. The inner cold finger, now precooled to a temperature lower than the bath, can focus on cooling just a small part of the membrane. The whole device is then covered by 25 nm of AlOx using atomic layer deposition. This passive layer isolates the cooler electrically from any structure patterned on top of it [4]. Performance of the device is shown in Fig. 1c when three outer coolers are set to their optimum bias points. In general, the chip is always overheated, and the membrane is effectively cooled with extra help from the auxiliary coolers. At optimum cooling, phonon temperature on the membrane reaches 150 mK down from 250 mK, where the latter is an achievable base temperature of a ^{3}He cryostat.

This practical platform is suitable for a wide range of applications. Most importantly, it is

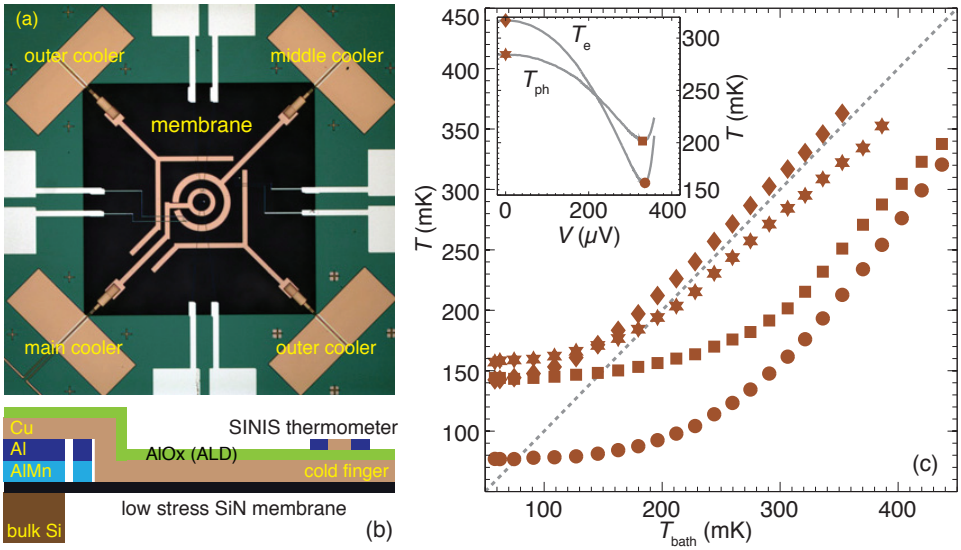

Fig. 1. (a) Layout of the cooling platform equipped with four SINIS coolers at corners of the low stress SiN membrane and an onion-like cold finger design. (b) Cross-sectional diagram of the device. (c) Temperatures at different parts of the device as a function of bath temperature when all outer coolers are biased optimally. Diamonds show the temperature of the main cooler at zero bias. Stars show the phonon temperature at the center of the membrane when the main cooler is at zero bias. Squares represent the main result of this work, the lowest phonon temperature on the membrane, and circles are the lowest electron temperature of the main cooler. The dashed line yields $T = T_{\mathrm{bath}}$. The inset shows data at 305 mK bath temperature as a function of bias on the main cooler.

not perforated. A robust SiN membrane with excellent mechanical properties would survive further integration with other devices. For example, fabrication of a kinetic inductance device or a qubit on it would be quite straightforward following the demonstrated fabrication scheme. Moreover, the whole platform is passivated with alumina, isolating the foreseen cooled device on top. The passivated alumina layer also allows a free design of the cold finger layout as required by different applications. These two advances transform the SiN membrane into a robust and versatile platform. Last but not least, the cooler has high power and can thus accommodate dissipative devices on top. This platform would provide a phonon bath of 150 mK when attached to a ^{3}He adsorption cryostat.

To summarize, a standard commercial SiN membrane is transformed into a cooling platform by integrating it with powerful SINIS refrigerators. Phonons at the center of the membrane reach 150 mK from 250 mK starting temperature, the base temperature of a ^{3}He cryostat. This passivated, unperforated platform is compatible with a wide range of requirements set by practical implementations.

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