

Advanced Fabrication Processes for Superconducting Very Large Scale Integrated Circuits

Sergey K. Tolpygo, Vladimir Bolkhovsky, T.J. Weir, Alex Wynn, D.E. Oates, L.M. Johnson,
and M.A. Gouker

Lincoln Laboratory, Massachusetts Institute of Technology Lexington, MA 02420, USA

Email: sergey.tolpygo@ll.mit.edu

Abstract— We review the salient features of two advanced nodes of an 8-Nb-layer fully planarized process developed recently at MIT Lincoln Laboratory for fabricating Single Flux Quantum (SFQ) digital circuits with very large scale integration (VLSI) on 200-mm wafers: the SFQ4ee and SFQ5ee nodes, where “ee” denotes the process is tuned for energy efficient SFQ circuits. The former has eight superconducting layers with 0.5 μm minimum feature size and a 2 Ω/sq Mo layer for circuit resistors. The latter has nine superconducting layers: eight Nb wiring layers with the minimum feature size of 350 nm and a thin superconducting MoN_x layer ($T_c \sim 7.5$ K) with high kinetic inductance (about 8 pH/sq) for forming compact inductors. A nonsuperconducting ($T_c < 2$ K) MoN_x layer with lower nitrogen content is used for 6 Ω/sq planar resistors for shunting and biasing of Josephson junctions (JJ). Another resistive layer is added to form interlayer, sandwich-type resistors of m Ω range for releasing unwanted flux quanta from superconducting loops of logic cells. Both process nodes use Au/Pt/Ti contact metallization for chip packaging. The technology utilizes one layer of Nb/ AlO_x -Al/Nb JJs with critical current density, J_c of 100 $\mu\text{A}/\mu\text{m}^2$ and minimum diameter of 700 nm. Circuit patterns are defined by 248-nm photolithography and high density plasma etching. All circuit layers are fully planarized using chemical mechanical planarization (CMP) of SiO_2 interlayer dielectric. The following results and topics are presented and discussed: JJ fabrication, the effect of surface topography under the JJs on their properties and repeatability, I_c and J_c targeting, effect of hydrogen dissolved in Nb, circuit inductors, MoN_x properties for the resistor layer and for high kinetic inductance layer, technology of m Ω -range resistors.

This work was sponsored by the IARPA under Air Force Contract FA872105C0002. Opinions, interpretations, conclusions, and recommendations are those of the authors and not necessarily endorsed by the United States Government.

Keywords (Index Terms)— Josephson junctions, kinetic inductance, MoN_x , Nb/ AlO_x /Nb Josephson junctions, ERSFQ, RSFQ, RQL, SFQ digital circuits, superconductor integrated circuits.