30-GHz Operation of Datapath for Bit-Parallel, Gate-Level-Pipelined Rapid Single-Flux-Quantum Microprocessors

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***Abstract*—We report high-speed operation of the datapath test circuits that were designed for high-throughput rapid single-flux-quantum (RSFQ) microprocessors. After we demonstrated several RSFQ microprocessors called CORE1 based on simple, bit-serial architectures, we started development of advanced microprocessors based on bit-parallel processing by co-design in device/circuit/architecture levels. Our quantitative exploration of computer architecture targeting bit-parallel RSFQ microprocessors revealed that gate-level-pipelining with fine-grained multithreading would be a promising approach [1], and we successfully demonstrated 56-GHz operation of a bit-parallel, gate-level-pipelined arithmetic logic unit (ALU) up to 56 GHz [2]. In this work, we designed the datapath of the bit-parallel microprocessors which has more complex interconnections. The datapath is composed of the gate-level-pipelined ALU and a ring-structure register file that supports fine-grained multithreading. Data stored in the register file are read out, processed in the ALU, and then written back to the register file. The challenge in the design is realization of high-frequency pipeline operation with a large number of feedback loop paths.**

We designed the datapath, where we can execute 12-thread, 4-bit register-to-register operation such as addition, subtraction, and comparison among four registers in each thread to show the feasibility. The target clock frequency is 30 GHz, i.e., the expected throughput is 3×10^{10} operations per second. We overlapped the ALU and register file in the layout design to shorten feedback loop paths and hybridize concurrent- and counter-flow clocking to minimize clock skew in the loops to achieve high-frequency operation. We fabricated the test circuits using the AIST Nb 9-layer, 10-kA/cm^2 process. We integrated 9600 Josephson junctions on a 3.42×2.37 mm^2 area, including peripheral circuit components for on-chip high-speed testing. The circuits were designed with the conventional RSFQ cell library, and the estimated power consumption is 2.51 mW at the designed point. We have confirmed several successful gate-level-pipelined operations at high clock frequencies up to 31 GHz. The first tape-out of the prototype microprocessor including the designed datapath was submitted on January 2018, and fabrication and testing is ongoing.

[1] K. Ishida et al, "Exploring Design Space of a Single-flux-quantum Microprocessor," *IPSJ Journal*, vol. 58, pp. 629–643, 2017.
[2] M. Tanaka et al, "High-throughput bit-parallel arithmetic logic unit using rapid single-flux-quantum logic," ISEC 2018, Sorrento, Italy, 2018.

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***Keywords (Index Terms)*— Datapath. RSFQ microprocessors, throughput-oriented microprocessors, CORE1, ALU.**

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