Reversible Fluxon Logic for Future Computing

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***Abstract*—Today's industrial digital logic gates are reaching a technological limit and meanwhile, superconducting circuits produce fundamentally different technologies for the future of digital computing. The standard logic is irreversible and yet superconducting circuits allow digital reversible logic with a much higher energy efficiency per gate operation. Previous reversible gate circuits were "adiabatic," meaning that they used adiabatic-clocking waveforms for their operation power. However, we are studying logic starting from a ballistic model, where fluxons enable gates using only energy from their inertia. Our fluxons are defined in Long Josephson Junctions (LJJs) and may travel ballistically, similar to a particle with negligible damping. Once a fluxon's energy approaches close enough to the gate, a resonance is induced at the gate and the fluxon loses its definite topology. Gates are comprised of the (few Josephson-penetration-depth long) ends of LJJs and a connecting circuit interface. Only after the resonance does a fluxon get formed and yield the gate result without external power: a fluxon for bit-state 0 or an antifluxon for bit-state 1. Through earlier analysis of the numerically discovered phenomena we find that dynamics can be described with fluxon- and antifluxon-like excitations at the ends of LJJs within the gate. The bit-switching action in our gates is resonant indicating fundamentally different dynamics than the classic model of adiabatic reversible circuits. Our ballistic Reversible Fluxon Logic (RFL) gates have no added damping and calculated energy efficiencies of over 97%. Thus in our dynamical process the "bit energy" is preserved. However, irreversible logic completely dissipates this at each operation (e.g., charging energy in CMOS or SFQ energy in irreversible SFQ logic). An RFL gate can achieve a fast gate operation since its resonance is only few JJ plasma periods. We also describe the CNOT in our technology. It is enabled by a couple of vital gates: A IDSN logic gate, similar to our other ballistic gates, and a Store-aNd-Launch (SNL) timing gate to ensure proper synchronization of the bits. The latter allows bit storage followed by launching of a data fluxon using an adiabatic pulse from a clock fluxon with lower energy than the data fluxon for good CNOT efficiency.**

I. Introduction

The technology roadmap for semiconducting logic is changing, in part due to the inability to scale down gate dimensions much further. For a long while scaling allowed CMOS logic gates to achieve smaller energy costs due to a corresponding lower gate capacitance. Between gates the charging energy or bit energy is completely dissipated for each bit switching. This energy greatly exceeds the minimum energy cost, $\log_e(2)k_BT$, from bit erasure, and well known to be present in gates with irreversible (non-one to one) operations. Reversible computing avoids this information energy limit, and this was understood by Bennett when he developed a mathematical model of a reversible computer [1]. By 1982, Likharev had analyzed how to achieve reversible computing in a superconducting circuit, using an adiabatically applied (clock) field [2]. Research has recently expanded beyond this early pioneering work, creating demonstrations of reversible digital logic circuits using Quantum Flux Parametron (QFP) [3] and N-SQUID [4] circuits. They both use adiabatic clock fields which made them comparable to Likharev's original proposal of adiabatically steering the state evolution with potential energy [2]. The predicted result is that the switching energies are proportional to the inverse of the gate time, and theoretically that this can lowered indefinitely towards zero.

A lesser-known energy conservative method for computing was described as "ballistic reversible" gates and used inertia-powered billiard balls [5]. This physical model is distinct from Likharev's adiabatic model since inertia rather than external fields power the logic gate. Optical experiments with solitary waves have been conducted as a scientific investigation of ballistic reversible gates which result in time-delays or path switching [6].

Here we describe ballistic logic gates using simulated circuits. Our logic gates, named Reversible Fluxon Logic (RFL), use fluxons which are flux solitons in gates without external power [7]. Fortunately this allows for efficiency that is greater than 97% per logic gate. In Table I we compare different gate technologies. The first column describes the bit energy in CMOS – the well known charging energy from the capacitance C and a drain or bias voltage V. The second column describes how irreversible SFQ (e.g., RSFQ, ERSFQ, RQL) logic dynamically operates with a energy cost of $\sim I_c\Phi_0$ for a particular JJ that is switching and has critical

Logic Gate Property	CMOS	Irreversible SFQ	Adiabatic Rev. SFQ	Ballistic Rev. Logic in RFL
Bit Energy (E_B)	$CV^2/2$ = charging energy	$I_c\Phi_0$ = switching energy	$\lesssim I_c\Phi_0$ = time-dependent E_B	$8I_c\Phi_0\lambda_J/(2\pi a)$ = E_B (for v=0); E increases as $1/\sqrt{1-v^2/c^2}$
Energy cost per switching element	$CV^2/2$ per gate	$\lesssim I_c\Phi_0$ per JJ	$\ll I_c\Phi_0$	<< E_B (cost seen as lower v)
Power source in logic gate	voltage bias V	current bias $I \lesssim I_c$	multi-phase current bias	none (v restored elsewhere)

Table I
THIS TABLE COMPARES THE BIT ENERGY AND ENERGY COST OF DIFFERENT LOGIC GATE TECHNOLOGIES. THE DIFFERENCE IN REVERSIBLE LOGIC RELATIVE TO IRREVERSIBLE LOGIC IS THAT THE BIT ENERGY IS PRESERVED TO A LARGE EXTENT. IN RFL GATES THE BIT ENERGY IS PRESERVED WELL FOR MODERATE VELOCITY v. ADDITIONALLY, AN INCOMING FLUXON RESULTS IN AN OUTGOING FLUXON, WITH NO EXTERNAL POWER APPLIED WITHIN THE GATE (ASSUMING REQUIREMENTS FROM NUMERICAL SIMULATIONS ARE MET).

current I_c. The bit energies in logic, $\gg k_BT$, generally meet stability requirements such that an internal potential barriers distinguishes states and are immune to thermal excitations $\sim k_BT$. As a result, a typical value of $\sim I_c\Phi_0$ must be dissipated for each JJ that switches phase in these irreversible gates.

In contrast, reversible logic can preserve some bit energy. An adiabatic reversible gate, as analyzed by Likharev [2], can lower dissipation inversely with clock period, due to the way less energy is consumed in powering the dynamics. We are studying ballistic fluxons in LJJ connecting to logic gates, where the rest or potential energy of a fluxon (bit) in a LJJ is fixed at $8I_c\Phi_0\lambda_J/(2\pi a)$. Here we have chosen a discrete model of lattice constant a for simulations, but we are also near the continuous limit of the LJJ, where fluxons have no known fundamental limits for loss meaning that the fluxon does not slow significantly in our usage (over distances of $\sim 10\lambda_J$). Here the Josephson penetration depth is large $\lambda_J \simeq 3a \gg a$; it sets the length of phase gradients about the fluxon as well as the near the ends of LJJs. The bit energy can be adjusted for the application, similar to other superconducting technology. The ballistic dynamics in our simulations show potential energy is conserved after the gates, meaning that for each fluxon into the gate we will get a fluxon out. However, we have two distinct features in our ballistic gates relative to the classic billiard-ball model: 1) flux polarity changes rather than having path changes that are found in the classic model of ballistic gates and 2) resonance in the gate for the switching is necessary here but not in the adiabatic reversible gate type. Another group studies reversible ballistic logic [10] and recently studied a one-LJJ circuit for fluxons with internal state memory [11]. One distinction of our fluxon logic is the use of shunt capacitors on LJJ ends, added to the JJs within gates; we find this allows a resonance to enable high-efficiency forward-scattering gates.

II. KICKING OFF A BALLISTIC REVERSIBLE LOGIC

We initially study a 1-bit gate structure to develop a circuit-based method to switch the bit state in a ballistic logic gate. The flux polarity here corresponds to the bit state, such that a polarity change corresponds to a bit switch. The structure for a general 1-bit gate is shown in Figure 1 a). Specifically it is the NOT gate, which is defined by particular parameters in the structure that allow change of the polarity of the fluxon: from fluxon to antifluxon or vise versa. The structure consists of two LJJs and a circuit interface with 3 JJs which connects them. The 3 JJs of the interface are substantially different than the JJs of the discrete LJJ in that they have tuned values including large added (shunt) capacitances to allow a resonance used for bit switching. Without these capacitances, an incoming fluxon would not be able to excite the necessary large (non perturbative) resonance.

After an initial *kick* (launch) from something else, a fluxon is incident with some velocity towards the NOT gate. As it arrives, the fluxon changes into an interface oscillation involving the LJJs. Only later does the oscillation emit an antifluxon in the other LJJ. This structure does not require any twists of the planar LJJ structure to switch polarity. Rather, the fluxon polarity is converted in the NOT gate due to the resonance. The topology of a fluxon break down near the interface relative to ordinary SFQ because the gate contains a JJ for phase slipping, one which is not intended to store a flux quantum, and this allows the oscillation toward a new state. In fact, in the adiabatic limit (for substantially small fluxon velocity) the flux quantum will be lost in the gate rather than be stored (though a 2π phase winding will remain at the interface). This distinguishes this logic from other SFQ logic types (irreversible or reversible). The gate parameters must be set in the NOT gate and other logic gates for the proper free dynamics with a defined range of input velocities.

If the parameters are defined specifically different, resonant oscillations will be different and the polarity and fluxon can be forward emitted after oscillations with no change in polarity. We define this as an IDentity gate. Of course other parameters will produce less useful dynamics (energy annihilation or fluxon reflection). There are simpler structures for fluxon scattering which use a "defect" within a LJJ. These studies include resonant chaotic scattering at point defects [8] and fluxon scattering at a qubit-induced potential [9]. However, these previously known scattering types do not allow polarity change. The interface scattering used in RFL gates is non-perturbative, where a fluxon breaks up and loses its identity at the interface.

To analyze these complex dynamics we have developed a reduced coordinate model [7]. The solution uses a superposition of a fluxon and mirror antifluxon in each LJJ. With it we are able to reduce the many degrees of freedom (3 interface JJs plus the many JJs that approximate the LJJs) to only 2 degrees of freedom. This assumption is justified by quantitative agreement between the analyzed dynamics and that from full numerics (See Ref. [7] for details).

A two-bit gate is an important practical gate in RFL, and extends the use of resonant dynamics in the fundamental 1-bit gates. As we will discuss below, it allows ballistic gates with conditional polarity inversion – action on one bit depends on the polarity of the other. From Fig. 1b) we can see that the 2-bit gate generally has 4 LJJ "fluxon waveguides" and 7

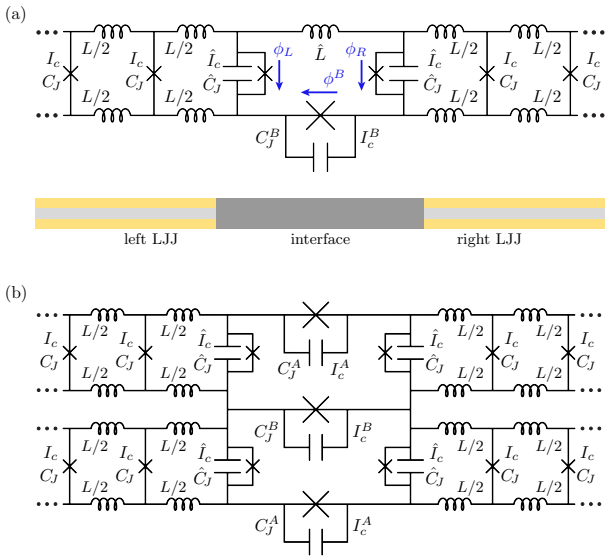


Figure 1. **RFL Gate Structures. Upper Panel)** Schematic for a one-bit RFL gate consisting of a interface cell (with JJs : N_I, $N_{I+1}$and the central I_C^B) and two LJJs (to the left and right). To be considered as ballistic RFL gates, they must exhibit specific reversible resonant dynamics with free incident fluxons. These dynamics are found to be enabled by large shunt capacitances in the interface JJs, in addition to specific values for the interface parameters. The x-scale indicates JJ positions for a possible unit cell size a, is much smaller than the Josephson penetration depth λ_J . **Middle Panel)** a representation of the gate, which emphasizes the nature of the gates to work with LJJs, since the dynamics in the discrete LJJs is similar to the continuous limit. **Lower Panel)** Schematic for two-bit RFL gates consisting of 7 JJs in a circuit interface and 4 LJJs. These allow gates with reversible dynamics similar to 1-bit gates, but also allow the added feature of input-dependent (conditional) polarity changes.

JJs in the gate interface. We always numerically compute the dynamics of the gates, and this generally requires optimization of the interface parameters. However, we have found that the parameter margins suggest that the gates can be realized (see Ref. [7]).

One set of dynamics for the NOT gate is shown in Figure 2. In the (a) panels one can see the JJ phases of the left (typical input) and right (typical output) LJJ at particular times. Figure 2 (b) corresponds to continuous false-color display of phase dynamics in time (relative to panels (a)). In panel (a1) a fluxon (2π to 0 winding in phase vs. position) is seen at a time that it is approaching the interface from the left. The fluxon is still located in the bulk of the input LJJ and has not yet substantially excited the interface JJs. In panel (a2) the fluxon excitation has clearly induced excitations on each side of the central JJ of the interface. Left of the interface there is a uniform 2π-phase established, related to the "wake" of the incident fluxon (with no potential energy at this time). To the right side of the interface there is a fluxon-type excitation in that there is a negative slope in phase vs. position. We see later in panel (a3) that the left (right) LJJ end has a antifluxon-like (fluxon-like) excitation. At a later time shown in (a4), we see that both LJJs ends have an antifluxon-like excitation. By this time there is a total phase difference in the central JJ that has grown to $\sim 3\pi$ (see panel c). By the time of panel (a5), an antifluxon has exited the interface to the right, and the total phase difference in the central JJ is 4π (see also panel c). The dynamics can be seen as a resonance

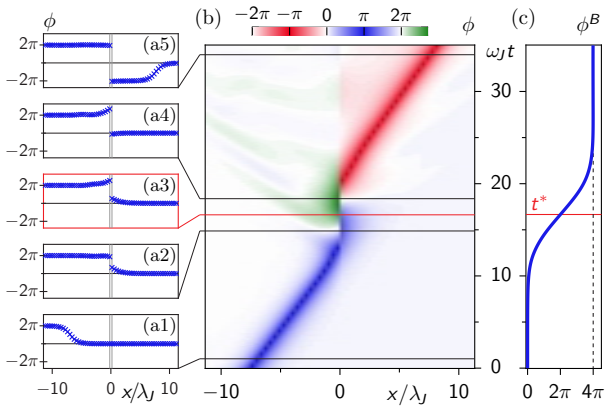


Figure 2. **RFL NOT Gate dynamics. a1-a5)** JJ phase ϕ_i versus position at subsequent times **a1)** input fluxon incident on gate with no other excitations **a2-a4)** intermediate logic gate resonance which uses the interface circuit and evanescent fields into 2 LJJs **a5)** antifluxon that has exited the gate. **b)** dynamics of JJs ϕ_i versus time showing constant fluxon velocity v away from gate interface. **c)** dynamics of the central JJ ϕ^B showing its adiabatic transition in phase by 4π.

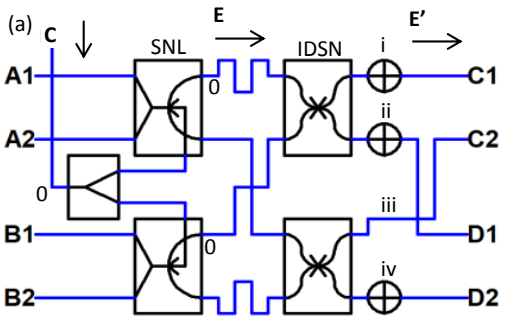
that appears as 2 "bounces," (see panel (b); for a reference on bounces see ref. [8]). The bounces are seen from maximally extending evanescent waves in color: at the time of panel a2 (a4) we see a π (3π) phase excitation decaying to the right (left) of the interface. The way in which these phases use wave-like dynamics is unusual in SFQ logic, but is natural to our RFL, since it uses a resonance to exchange energy through evanescent fields, from one side of the gate interface to the other.

III. The CNOT Gate in RFL

Some of our 2-bit gates can be performed with the power of two synchronous fluxons (Fig. 1), including the NSWAP [7] and IDSN [12]. Other hardware is planned to create the needed timing and fluxon routing. Together this can allow more complex gates, such as the CNOT gate shown in Figure 3 [12]. This gate consists of two Store-and-Launch (SNL) *clock* gates, two IDSN *logic* gates (that are ballistic), and other components.

The SNL gates allow for fluxon synchronization as part of the CNOT gate, and SNL details will be given in the next section. In operation of our CNOT, one bit state A arrives from the left as (A1 or A2) and likewise a bit state B on either B1 or B2. The bit state is then stored as a stored flux in the SNL. Later an incoming *clock* fluxon arrives along the C LJJ and, using a known t-branch, splits into two half-energy fluxons with the velocity nominally unaltered. They then continue unimpeded, and each impinge on an SNL gate. Each of these clock fluxons now cause a data fluxon to launch on a right-side LJJ, depending on the stored flux state. If the bit state is 0 (1), a fluxon (antifluxon) will be launched into the upper-right (lower-right) LJJ. These fluxons travel towards the IDSNs such that any bit state 0 will arrive at the upper IDSN and any bit state 1 will arrive at the lower IDSN.

The IDSN gates have a the structure of Fig. 1b and can operate with either one input fluxon of any polarity or two input fluxons of the same polarity. In the latter case, the



(b)

A B	A⊕B	path to	C=A⊕B	D=A
0 0	0	C1 D1	0	0
0 1	1	C1 D2	1	0
1 0	1	C2 D1	1	1
1 1	0	C2 D2	0	1

Figure 3. a) The CNOT schematic consisting of i) two (ballistic) IDSN gates, ii) two Store-aNd-Launch (SNL) gates, LJJs as wiring (blue), and other components. A low-energy clock fluxon arrives along C to power the timing of the gate. b) A table showing the action of the CNOT for different input on A and B. One bit 0 (bit 1) as a fluxon (antifluxon) approaches the SNL from the left. The "path to" column indicates which the LJJ the the path of the bit. The XOR result of the CNOT is bit C and the copy of A appears as bit D.

Upper In	Lower In	Upper Out	Lower Out
-	-	-	-
0(F)	-	0	-
-	0	-	0
1(AF)	-	1	-
-	1	-	1
0	0	1	1
1	1	0	0

Table II
THE IDSN GATE LOGIC TABLE DESCRIBES THE ACTION FOR NULL INPUT (-), INPUT FLUXONS (0), AND INPUT ANTIFLUXONS (1), ASSUMING THE FLUXON INPUT VELOCITY LIES IN THE ACCEPTABLE RANGE. THE IDSN GATE STRUCTURE IS SHOWN IN FIG. 1B. AN INCOMING FLUXON ON THE UPPER (LOWER) LEFT LJJ WILL BE SCATTERED TO THE UPPER (LOWER) RIGHT LJJ. THE ACTION OF THE IDSN GATE IS SUMMARIZED AS "IDENTITY, EXCEPT SAME-POLARITY YIELDS NOT."

two data fluxons will arrive at a IDSN synchronously. The fluxons then satisfy the possibilities for an IDSN operation according to Table II: 1) one-input fluxon will undergo the IDSN gate, that is 1) the *IDentity* (unchanged bit) operation for one bit on upper or lower LJJs and 2) for two fluxons arriving synchronously with the *Same* polarity the *Not* operation. The fluxons are output on the upper (lower) right LJJ if they enter on the upper (lower) left LJJ. Next, some of the fluxons pass through a NOT gate, indicated by a $\oplus$. The output bits C and D arrive at either C1 or C2 for bit C and either D1 or D2 for bit D. The resulting bits can each be stored in another SNL for subsequent processing if desired.

IV. THE STORE AND LAUNCH (SNL) GATE

The SNL is a gate that stores the bit state of an input fluxon and then launches a fluxon on a path depending on the bit state. The IDSN gate above is a core gate to RFL because it has near unity efficiency. Thus the SNL is "only" a *clocking* gate that enables the near-unit-efficiency ballistic gates by providing timing and synchronization. Recall that in the above CNOT schematic, the ballistic IDSN gate receives the appropriate fluxons launched from SNL gates. We previously introduced a SNL gate schematic with one-input in Ref. [12]. We now report on the SNL, Fig. 4, for the CNOT gate which has the required two-input LJJs.

This gate has been simulated for a range of parameters and input fluxon velocities. Logical reversibility in our *ballistic* logic gates are accomplished with the requirement of left-right physical symmetry of the corresponding gate circuit. In contrast, the SNL is designed to always launch bits to the right so there is no required left-right symmetry. This new SNL holds a bit state as a circulating current using a central loop with JJs containing phases $\phi^U_{N_l}, \phi^U_{N_l+1}, \phi^L_{N_l}, \phi^L_{N_l+1}$. A clockwise current is stored for bit state 0 (flowing cyclically through JJ phases $\phi^U_{N_l}, \phi^U_{N_l+1}, \phi^L_{N_l+1}, \phi^L_{N_l}, \phi^U_{N_l}, ...$) and a counterclockwise current is stored for bit state 1. These bits previously were *data* fluxons in the bulk of the LJJ, but the SFQ changed of course after it approached as a fluxon towards the SNL from the left. Accordingly, the circulating current magnitude changed but the direction of current circulation (CW or CCW) was preserved.

Again, the SNL can store a bit unlike our ballistic gates. When the SNL gate stores flux, it stores much of the potential energy of the incident fluxon. Some energy from the incident fluxon is lost in damping resistors, however, a large fraction of the rest energy from the fluxon can be stored in JJs. The JJs in the SNL, including adjacent JJs of the input and output LJJs, are optimized (for a given clock fluxon energy and input-data fluxon energy range) to enable an efficient conversion of the clock-fluxon energy into kinetic energy of the launched fluxon. The kinetic energy of data fluxons in typical simulations are only 20% of the total fluxon energy, so this sets an approximate energy scale for the energy required (in principle it could be lower or higher than this amount).

The SNL is designed with tuned parameters such that when a clock fluxon arrives through the clock LJJ, the ouput fluxon velocity is made to be maximum for a range of input velocities. The clock fluxon contains a small energy relative to the data fluxon, such as one half the value, to launch the stored energy as a fluxon. This is an advantage in energy conservation relative to irreversible SFQ gates which would dissipate all the bit energy in switching the bit state. The routing function of the gate is accomplished by the way in which an incoming clock fluxon will cause opposite current and phases change in $\phi^U_{N_l+1}$ and $\phi^L_{N_l+1}$. Note also that the currents induced by the clock fluxon pass similarly through 2 resistors such that the input side JJs with phases $\phi^U_{N_l}$ and $\phi^L_{N_l}$ experience a negligible current pulse. On the right-hand-side, the Lorentz force will induce flux to steer flux towards the appropriate lower or upper

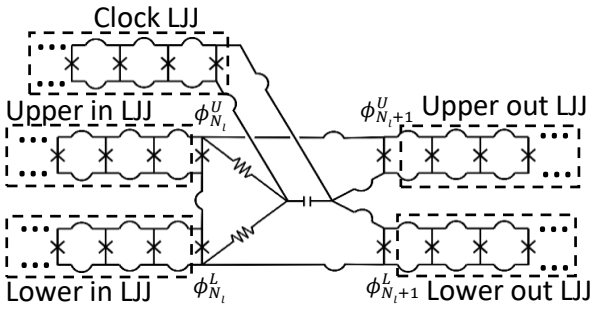


Figure 4. The Store aNd Launch (SNL) gate with 2 possible inputs and 2 possible outputs, all for one bit. These 4 data lines are LJJs. This clocking gate is not meant to be reversible unlike the ballistic logic gates; wiring to the clock LJJ breaks left-right symmetry. After bit storage, a clock LJJ can carry a low-energy clock fluxon relative to the data fluxons. The clock fluxon will cause a stored bit state 0 (1) to be launched as a fluxon (an antifluxon) out of the upper (lower) output.

output LJJ (through the JJ with $\phi^U_{N_l+1}$ or $\phi^L_{N_l+1}$). Due to the nature of the clock fluxon on the LJJ, a single JJ does not "switch" nonadiabatically, but rather the clock fluxon provides an adiabatic waveform to launch the data fluxon.

V. Conclusion

Reversible digital gates are important to the future development of computing because they can demonstrate much higher energy efficiency than the typical irreversible ones, including industry standardized CMOS gates. Recently demonstrated superconducting gates are physically similar to the adiabatic reversible model of Likharev, however, we are developing gates with a ballistic reversible model. The ballistic reversible gates in our RFL exploit a resonant process at special circuit interfaces to achieve a conditional polarity change of a fluxon. Fluxons are both the bits and the sole power source for ballistic gates. This can be physically understood in terms of fundamental 1-bit gates such as the NOT gate that we described. The advantage of our logic over irreversible logic is easily seen as full conservation of the rest (potential) energy of fluxons in logic operations. The 2-bit gate structure is more complicated than the 1-bit gate structure and uses 4 LJJs and an interface with 7 JJs. It allows gates such as the NSWAP and the IDSN.

To build up useful computations one needs other gates to generally support RFL gates. This can be seen in the execution of a CNOT gate. The CNOT uses 2 Store-aNd-Launch (SNL) gates to store bit states. This gate initially stores a bit, but later can route it (as a fluxon) towards an IDSN logic gate, using power only from a low-energy clock fluxon. To provide synchronization, a clock fluxon launches two data fluxons after bit storage, one from each SNL.

The SNL gate uses damping resistors unlike ballistic RFL gates which have none. This is needed because the SNL stores the incoming fluxon as a static circulating current. Note that the SNL does not use a DC bias like irreversible SFQ logic gates. This gate is efficient by irreversible SFQ standards because the gate will only dissipate a small fraction of the "bit energy" to launch the data fluxon.

This work indicates that reversible computing should be thought of more broadly than the classic adiabatic model of Likharev. In general the use of resonance in unpowered gates seems very convenient and also auxiliary structures to support these ballistic gates seems practical. There are many directions to progress this work, including work on the readout of a qubit with a classically reversible gate. We look forward to a future in superconducting circuits where the diversity of digital-reversible gates has reached the current diversity of quantum-reversible gates.

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