Design and Implementation of an SFQ-based Single-chip FFT Processor

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***Abstract*—We have been working on the development of a high-speed FFT processor using single-flux-quantum (SFQ) logic circuits. In our previous studies, we designed and demonstrated a 4-bit butterfly processor, a data-shuffling circuit, and a twiddle factor ROM for 4-bit 8-point FFT using the AIST 10 kA/cm^2 Nb advanced process 2 (ADP2) at maximum frequencies of 51.6 GHz, 59.5 GHz, and 51.5 GHz, respectively. In this study, to complete the FFT processor design, we designed and demonstrated residual component circuits called a rounding circuit and a data buffer at a target frequency of 50 GHz. We also designed and experimentally confirmed the operation of an SFQ-based single-chip FFT processor integrating all the component circuits.**

***Keywords (Index Terms)*—butterfly processing circuit, FFT, RSFQ, superconducting devices, SFQ circuit, Josephson integrated circuit.**

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