AC-Biased Shift Registers as Fabrication Process Benchmark Circuits and Flux Trapping Diagnostic Tool

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***Abstract*—We develop an ac-biased shift register introduced in our previous work (V.K. Semenov *et al*., *IEEE Trans. Appl. Supercond*., vol. 25, no. 3, 1301507, June 2015) into a benchmark circuit for evaluation of superconductor electronics fabrication technology. The developed testing technique allows for extracting margins of all individual cells in the shift register, which in turn makes it possible to estimate statistical distribution of Josephson junctions in the circuit. We applied this approach to successfully test registers having 8, 16, 36, and 202 thousand cells and, respectively, about 33, 65, 144, and 809 thousand Josephson junctions (JJs). The circuits were fabricated at MIT Lincoln Laboratory, using a fully planarized process, 0.4 μm inductor linewidth and $1.33 \cdot 10^6$ cm^{-2} junction density. They are presently the largest operational superconducting SFQ circuits ever made. The developed technique distinguishes between "hard" defects (fabrication-related) and "soft" defects (measurement-related) and locates them in the circuit. The "soft" defects are specific to superconducting circuits and caused by magnetic flux trapping either inside the active cells or in the dedicated flux-trapping moats near the cells. The number and distribution of "soft" defects depend on the ambient magnetic field and vary with thermal cycling even if done in the same magnetic environment.**

***Keywords (Index Terms)*— Flux trapping, Josephson junctions, RQL, RSFQ, SFQ digital circuits, SFQ VLSI, superconducting digital circuits, superconductor electronics**.

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