Impact of Recent Advancement in Cryogenic Circuit Technology

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***Abstract*—A new generation of cryogenic circuit technology is significantly advanced, combining superconductor with novel, various materials and physics such as ferromagnetism and thermal assistance. The extremely energy-efficient, high-density logic families, large-capacity memory, and effective power supplying will be promising for the single-flux-quantum-based digital circuits to be applied in practical use, especially in high-performance computing applications. In this paper, we discuss the impact of recent advancement in the cryogenic circuit technology. We also report recent progress of microprocessor development in Japan.**

Keywords—energy-efficiency; high-performance computing; microprocessors; nano-structured device; single-flux-quantum logic; superconductor spintronics, thermal-assisted device

I. Introduction

The idea to use superconductor switching devices in digital circuits toward computing applications originates from the cryotron in 1950s [1]. Subsequently, the trend of superconductor digital circuits has been drastically changed every two decades. We assume that the cryotron can be regarded as the "zeroth generation" of superconductor digital circuits, in terms of non-use of Josephson junctions. The first and second generations will be the latching logic and single-flux-quantum (SFQ) logic [2], where voltage levels and magnetic flux quanta are used for representing binary information, respectively.

The advantage of superconductor digital circuits is ultrafast operation and ultralow power consumption. Until the second generation, operation speeds were mainly prioritized. As information and communication technology (ICT) have advanced, however, energy efficiency became a keyword because of excessive increase of energy use in large-scale computing systems, such as data centers and supercomputers. That motivated invention of energy-efficient logic families, the third generation, of superconductor digital circuits.

The third-generation circuits also feature the combination of novel, different types of materials and physics. It had been well known that contamination of ferromagnetic materials into superconductor results in serious degradation of superconductivity, and introduction of magnetic materials was regarded as taboo. After the progress in fabrication process technology, the fusion of superconductor and magnetic materials has led to a new area, called superconductor spintronics. In addition, superconductor devices based on nanotechnology made a great impact. Particularly, a nanocryotron (nTron) [3] is a game-changing device because it can generate voltage of as high as ~1 V with reasonable switching speed and power consumption, while a single Josephson junction generates only a couple of millivolts.

Here we discuss the following topics in the recent advance of SFQ-based circuit technology: (i) energy-efficient circuitry suitable for further integration, (ii) large capacity memory, and (iii) effective power supply. We also report the recent progress in our development of SFQ microprocessors toward high-performance computing.

II. Recent Advancement in Third-Generation Citcuits

A. Energy-Efficient Circuitry Suitable for Further Integration

The conventional SFQ (second-generation) circuits are driven with dc constant currents supplied through large bias resistors, and thus the static power consumption at the bias resistors were large. The solution in the third-generation circuits are roughly categorized into two groups: reducing bias voltages or introduction of ac powered circuitries. In former group, a simple approach is use of small resistors with large inductance to keep constant currents [4, 5] or without extra inductance in exchange for changing driving mode to low-voltage, constant-voltage, called LV-RSFQ [6]. These result in reduction of power consumption at bias resistors. Another advanced approach is to use Josephson junctions as current limiters in substitute for resistors [7, 8]. In this approach, the power consumption of circuits are only dynamic power consumption, which is approximately equal to $I_c\Phi_0$ per Josephson junction per one switch (where I_c is the average critical current and Φ_0 is magnetic flux quantum), while large inductances are required to smoothing bias currents. The latter group includes RQL [9], AQFP [10], and nSQUID [11]. The dynamic power of RQL is comparable with $I_c\Phi_0$, while many logic gates can be built with fewer number of Josephson junctions compared with conventional RSFQ. AQFP and nSQUID consumes much smaller dynamic power. In these logic families, the ultimately low power dissipation even below the thermodynamic limit can be achieved in physically and logically reversible circuits.

Density is an important metric for integrated circuits. Use of shunt-resistor-free Josephson junctions should be attractive in terms of increasing integration density. Recently, we reported that shift-registers composed of shunt-resistor-free junctions

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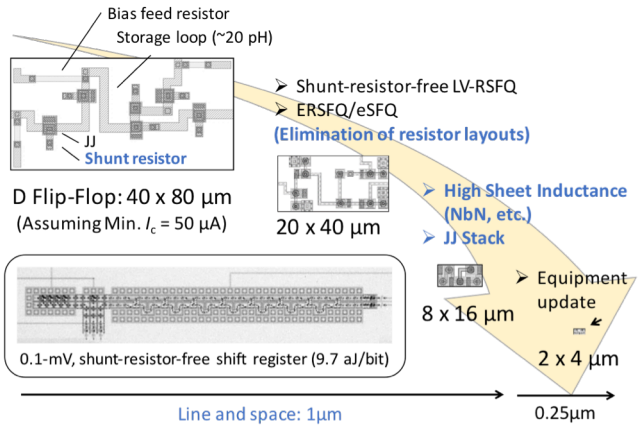


Fig. 1 Approach to further integration. Microphotograph of shunt-resistor-free shift-register is shown in inset.

experimentally showed better performance, especially with higher critical density, 10-kA/cm^2 process in LV-RSFQ [12], as well as in AQFP [13] (microphotograph is shown in Fig. 1 inset). At lower driving voltage, small bias resistors act as shunt resistors, and lightly dumped junctions can switch faster, resulting in better energy efficiency by ~10%. A shunt-free junction with a small bias-feeding resistor can achieve extremely small footprint, if we form vertically stacked two Josephson junctions with a normal layer stacked vertically on the top electrode.

Reduction of sheet inductance will be also a serious problem in further integration with fine patterns. Dc-biased logic families without mutual coupling have advantage that kinetic inductance can be used to obtain higher sheet inductance. Fig. 1 shows the possible approach and expected effects toward further integration. Without layouts for shunt resistors, size of logic gates will be reduced half. Stacking of a couple of Josephson junctions [14] and introduction of large sheet inductance material such as NbN will result in 1/25 reduction in occupied area within the conventional lithography.

B. Large Capacity Memory

Nanocryotron (nTron) has a potential to drive CMOS circuits directly with short delay because of their high-impedance characteristic in a kilo-ohm range. The nTrons will achieve small power dissipation compared with combination of Josephson junction stacks and CMOS differential amplifiers used in the conventional hybrid memory. We proposed Josephson-CMOS-nTron hybrid memory [15]. The concept is based on dynamic random access memory (DRAM), composed of address decoders based on the energy-efficient SFQ logic, nTron line drivers, a CMOS memory cell array, and Josephson current sensors. Our estimates predicted that the power consumption of the 64-kb Josephson-CMOS hybrid memory in a read/write operation and read access time would be approximately 1/12 of the conventional Josephson-CMOS hybrid memory.

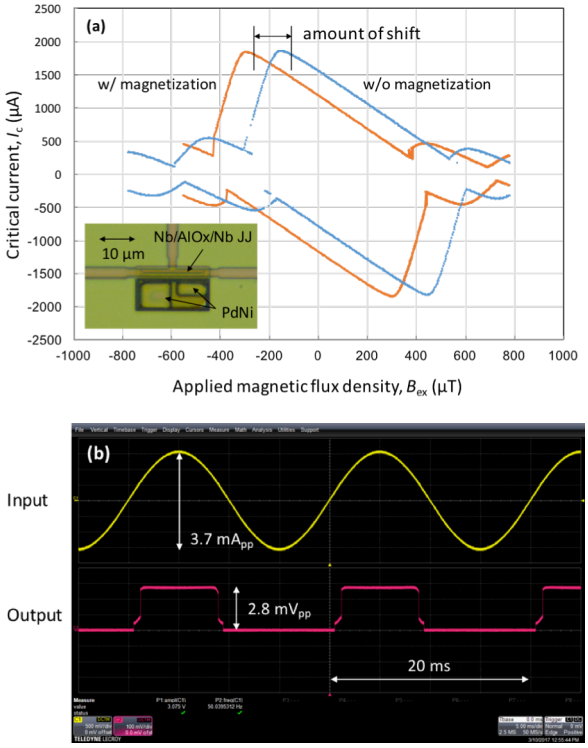


Fig. 2 Superconductor rectifier using ferromagnetic patterns: (a) microphotograph (inset) and (b) asynchronous I_c modulation.

C. Effective Power Supply

AC power supply is effective in cryogenic system, because impedance matching to very small input impedance of SFQ circuits is possible using transformers.

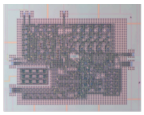
Recently ac/dc converter for cryogenic circuits has been invented [16], so that power can be distributed effectively even in the dc-powered SFQ circuits. Fig. 2 shows demonstration of half-wave rectification, where ac input currents were converted into a voltage output signal in the positive direction, from which we can obtain dc voltage in the order of millivolts by averaging.

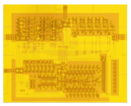
III. Microprocessor Development

High-performance computing is one of the ultimate applications of SFQ circuits. The United States currently supports development of SFQ-based supercomputers, as known as the Cryogenic Computing Complexity (C3) project [17]. In Japan, we have been developing SFQ microprocessors for 15 years. Nagoya University and Yokohama National University demonstrated 15-GHz operation of the bit-serial microprocessor called CORE1α in 2003 [18] using a Nb 4-layer, 2.5 kA/cm^2 process.

After the introduction of third generation circuits, we demonstrated microprocessors based on CORE1α with the low-voltage driving technique (LV-RSFQ) [6]. In 2015, Nagoya University and AIST has developed and successfully demonstrated a 100-GHz microprocessor, called CORE100 based on the 20-kA/cm^2 process [19]. In general, there is a trade-off between operating speed and power consumption, and

TABLE I PERFORMANCE COMPARISON





	Standard RSFQ	LV-RSFQ	Mixed-voltage RSFQ
Technology	ISTEC 2.5-kA/cm^2	AIST 10-kA/cm^2 ADP	AIST 20-kA/cm^2
JJ Count	4999 JJs	3869 JJs	3073 JJs
Bias Voltage	2.5 mV	0.5 mV	5 mV (data path) 0.5 mV (control unit)
Power	1.6 mW	0.23 mW	1.0 mW
Clock Freq.	15 GHz	35 GHz	100 GHz
Performance	167 MIPS	333 MIPS	800 MIPS
Power Efficiency	100 MIPS/W	1500 MIPS/W	800 MIPS/W
Space Efficiency	100 GIPS/chip	1500 GIPS/chip	800 GIPS/chip

we can select voltage depending on requirement. The CORE100 was designed based on the mixed-voltage RSFQ, targeting ultrafast operation above 100 GHz. Table I shows performance of these bit-serial microprocessors compared with the CORE1α. The maximum power efficiency obtained with LV-RSFQ was 1500 MIPS/W (including cooling penalty of ×1000), which was 15 times higher than CORE1α. The space efficiency was calculated under an assumption of future integrated level (10^7 junctions per chip). The bit-serial architecture is extremely efficient in terms of hardware use and energy use.

The above-mentioned SFQ microprocessors cannot be considered as a real microprocessor because we have not demonstrated programs stored in memory, though there are no reports in VLSIs other than Si-based ones. That is why we started bit-serial microprocessor series called CORE e. With the CORE e2, which had a minimal instruction set and hardware, we experimentally obtained correct operations of all the instructions; the microprocessor successfully executed several small programs stored in the embedded memory, such as integer division, a greatest common divider (the Euclidean algorithm), summation, highest proper factor, with high-speed clocks up to 61 GHz.

Recently, we explored architectural design space to achieve much higher performance for longer word length, such as 32 or 64 bits. Our investigation revealed that bit-parallel, gate-level-pipelining with fine-grained multithreading would be a promising approach to achieve extremely high performance computing, in exchange for increase in hardware costs and design complexity [20]. We demonstrated 50-GHz operation of 8-bit parallel arithmetic logic units (ALU) using AIST 10-kA/cm^2 Advanced Process, and proved the feasibility of gate-level-pipelined, bit-parallel processing at clock frequencies as high as those we demonstrated with bit-serial processing. With this approach, the expected computational capability and energy efficiency exceeds that of the semiconductor microprocessors.

Note that the demonstrated CORE e2 microprocessor and bit-parallel ALU were designed with the conventional RSFQ logic, and introduction of energy-efficient techniques will provide much better performance with keeping comparable level of operating clock frequencies.

IV. CONCLUSION

The third-generation superconductor digital circuit technology has been making a great progress in addition to the above-mentioned topics, such as ferromagnet-based, superconductor phase engineering (flux biasing, reconfigurable circuits, etc.), magnetic Josephson junctions, and a variety of nanostructured devices based on low- and high-temperature superconductors. For microprocessor applications, we successfully demonstrated ultrahigh-speed operation of a bit-serial microprocessor over 100 GHz, a prototype of stored-program computing, and gate-level-pipelined, bit-parallel ALU to explore the path to much high-performance computing. There seem no major technical difficulties toward realization of computers; we believe that superconductor data centers and supercomputers will be available in near future, involving other superconductor technologies.

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