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Design and high-speed demonstration of an SFQ complex event detector circuit for complex event processing

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***Abstract*— Recently, many investigations are conducted for processing the big data. One is known as complex event processing (CEP), which is real time processing to extract meaningful information from an input data stream. High-speed real-time processing is essential in the CEP system. One potential application of the CEP system is for a network intrusion detection system (NIDS). The NIDS monitors packet data streams in the network, and detects packets that contain viruses by performing pattern matching between input data and virus patterns. A complex event detector (CED) circuit is a key component in the CEP system, which performs pattern matching between an input data stream and compared n-bit data patterns called "symbol". The symbol is usually represented by 8-bit data in NIDS. In this study, we develop a CED circuit using single-flux-quantum (SFQ) circuits, which operate at very high speed with extremely low power consumption. In our design, input data is compared with a symbol stored in 1-symbol matching circuit. CED circuits for detecting multiple symbols are designed by connecting the 1-symbol matching circuits in series. This architecture enables the scalability of the CED circuit when extending the symbol length. We designed and implemented an 8-bit 4-symbol SFQ CED circuit using the AIST ADP2 Nb process. The correct operation was confirmed at 52.1 GHz by on-chip high-speed measurements. We also consider the extension of the symbol number and the adaptation to regular expressions toward its practical applications.**

Keywords—SFQ circuits, Complex event detector, Pattern matching, Superconducting integrated circuits.

I. INTRODUCTION

Nowadays there are many researches on high-performance data processing intending to treat the so-called big data. One is known as complex event processing (CEP), which is real time processing to extract a meaningful data from an input data stream. High-speed real-time processing is essential in the CEP system. One potential application of the CEP system is for a network intrusion detection system (NIDS) [1]. The NIDS monitors packet data streams in the network, and detects packets that contain viruses by performing pattern matching between input data and virus patterns. Typically virus patterns are written in regular expressions.

A complex event detector (CED) circuit is a key component in the CEP system, which performs pattern matching between an input data stream and compared data patterns. Nowadays, due to advances in optical network technologies, communication speed is up to about 40 Gbps. In order to deal with this high-speed real-time data, we develop a CED circuit using single-flux-quantum (SFQ) circuits, which operate at very high speed beyond 50 GHz with extremely low power consumption [2]. In this study we designed and implemented a prototype 8-bit 4-symbol SFQ CED circuit and measured its operation by on-chip high-speed tests to show the validity of the SFQ CED system.

II. ARCITECUTRE OF SFQ CED CIRCUITS

The CED circuit performs pattern matching by comparing a 1-bit input data stream with data patterns, called symbols, which are stored in the circuit in advance. One data symbol is represented by an 8-bit word in NIDS [1]. A block diagram of a proposed SFQ CED circuit for four-symbol pattern matching is shown in Fig. 1. The SFQ CED circuit is composed of four 1-symbol matching circuits (1SMCs) connected in series. Each 1SMC has two data inputs. One of them is from an 8-bit SFQ register, which store a symbol to be compared, and the other is an input data stream, "Data". It also has a token input and a token output, "T_in" and "T_out," and a "Start_set" input to set the initial condition of each 1SMC. The 1SMC outputs a token, "T_out" to the next stage of 1SMC when an input data and the compared symbol coincide each other, and also it has already had a token from the previous stage of 1SMC at the last comparison time step.

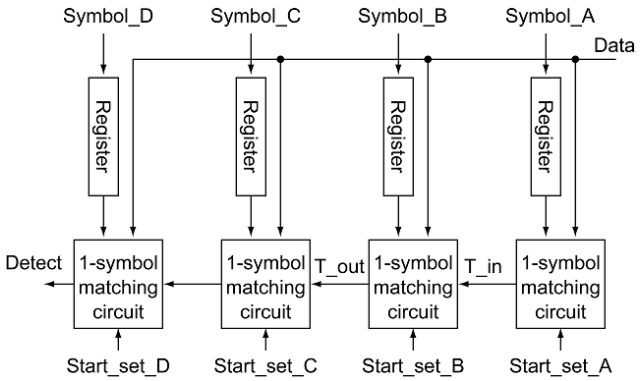

Fig. 1. A block diagram of a 4-symbol SFQ CED circuit

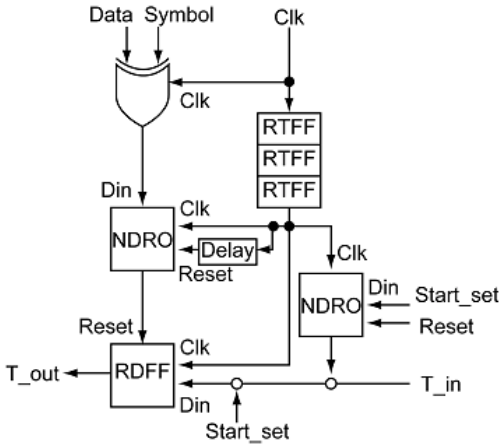

Fig. 2. A circuit diagram of the SFQ 1-symbol matching circuit

In operation of the 4-symbol CED circuit, at first, one of 1SMCs is enabled by applying a "Start_set" signal, which defines an initial position of data comparison in the circuit. Here we assume that the second 1SMC is enabled by a "Start_set_B." In this case the data stored in the second register "Symbol_B" will be always compared with the input data. Then, if the input data coincide with the symbol sored in the second 1SMC, a token signal, "T_out" is sent from the second 1SMC to the third 1SMC. In the next comparison time step, if the input data coincide with the symbol stored in the third 1SMC, a token signal is sent to the fourth stage of 1SMC. By repeating these operations, if the input data stream completely matches with the data pattern represented by (Symbol_B, Symbol C, Symbol D), a "Detect" signal is output from the last 1SMC. It is noted that a token is erased at each 1SMC when the input data do not coincide with the stored symbol at each comparison time step. The number of symbols, which is to be compared to the input data, can be varied from one to four by changing the position of the "Start_set" signal. For example, four-symbol matching is performed when a "Start_set_A" is applied to the circuits as an initial condition.

Fig. 2 shows a circuit diagram of the 1SMC, which is composed of an EXOR gate, non-destructive read-out delay flip-flops (NDROs), a resettable delay flop-flop (RDFF) and a counter composed of resettable T flip-flops (RTFFs). An input data stream and a stored symbol are compared bit-serially using the EXOR gate. The NDRO connected to the EXOR

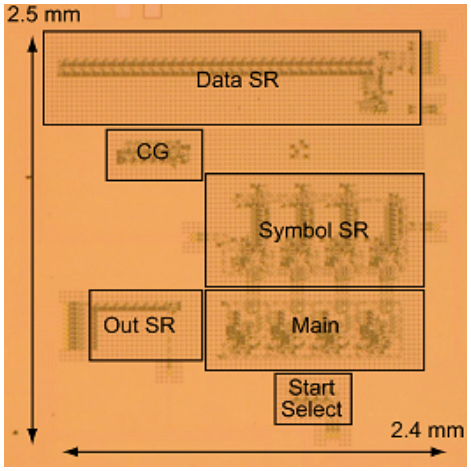

Fig. 3. Microphotograph of an 8-bit 4-symbol SFQ CED circuit with an on-chip high-speed test system.

TABLE I. STORED SYMBOL PATTERNS AND INPUT DATA PATTERNS IN THE MEASUREMENT

Pattern 1	Data	01 80 68 6F 73 74 00 $FF_{(16)}$
	Symbol	68 6F 73 $74_{(16)}$
Pattern 2	Data	B4 80 B4 01 B4 B4 00 $FF_{(16)}$
	Symbol	B4 $B4_{(16)}$

gate is clocked every eight-clock cycles and output a reset signal to the RDFF when any disagreement is detected in the bit-serial comparison. The RDFF store a token from the previous stage of 1SMC, which output a token to the next stage of 1SMC when it is not reset by the neighboring NDRO. The NDRO of the right side stores the "Start_set" signal to send a token to the RDFF at every comparison time step.

III. IMPLEMENATION AND MEASUREMENT RESULTS OF SFQ CED CIRCUITS

A microphotograph of an 8-bit 4-symbol SFQ CED circuit is shown in Fig. 3. The circuit is fabricated by using the AIST ADP2 Nb process. An on-chip high-speed measurement system is integrated with the CED circuit under test, which is composed of a clock generator to make a clock signal, input shift registers to store the input data and symbols to be compared, a "Start_Select" circuit to provide a "Start-set" signal to the CED circuit, and an output shift register to store a "Detect" signal from the CED circuit. The circuit area including the test circuit is 2.4×2.5 mm^2. The total bias current is 540 mA and the number of Josephson junctions is 4476.

The stored symbol patterns and input data pattern used in the measurement are shown in Table I. Data and symbol patterns are given in hexadecimal representation. The "Pattern 1" is a data pattern to check a matching condition of four symbols. The "Pattern 2" is a data pattern for a matching condition of two symbols. Output signals for these test patterns in the measurement are shown in Fig. 4 and 5. The "Clkout" shows frequency-divided clock signals from the CED circuit, which appears at the end of every comparison time step. The "Detect" indicates that the input data and the stored symbol pattern matched completely. In the Fig. 4, one

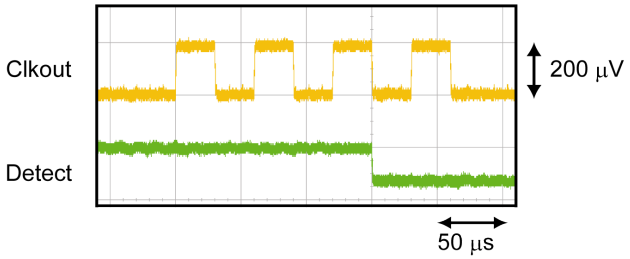

Fig.4. Output signals for the "Pattern 1" in the measurement. Each transition in the waveforms corresponds to the output of an SFQ pulse.

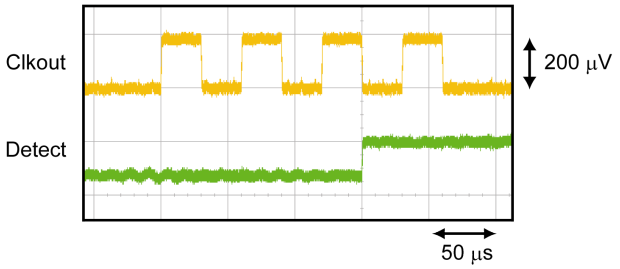

Fig. 5. Output signals of the "Pattern 2" in the measurement. Each transition in the waveforms corresponds to the output of an SFQ pulse.

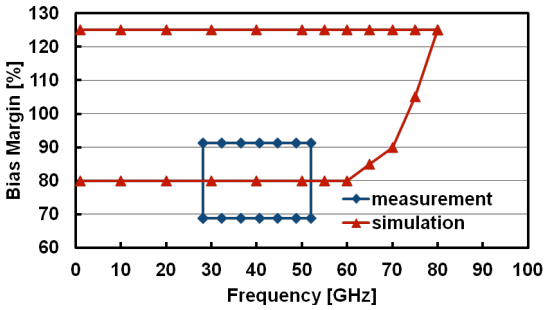

Fig. 6. Simulated and measured bias margins of the 8-bit 4-symbol SFQ CED circuit as a function of clock frequency

can see that a "Detect" output is observed at the 6th "Clkout" output, while the input data and the stored symbols in the "Pattern 1" completely matched at the 6th input data, "74" in the Table I. Similarly, in the Fig. 5, a "Detect" output is observed at the 6th "Clkout" output, while the input data and the compared symbols in the "Pattern 2" matched completely at the 6th input data, "B4". These results show the correct detection of the different length of symbols from the input data stream. Fig. 6 shows frequency dependences of DC bias margins of the 4-symbol SFQ CED circuit obtained by on-chip high-speed tests and circuit simulations. We evaluated that the bias margin at 50 GHz is 80% - 125% and the maximum frequency is 80 GHz by circuit simulations. In the measurement, we confirmed the correct operation at 52.1 GHz. The bias margin at 52.1 GHz is 68.8% - 91.2%. The maximum and minimum frequency was limited by the on-chip clock generator this time.

IV. Scalability of CED Circuits

Due to the scalable design of the proposed CED circuits, we can simply extend the number of symbols to be matched without decreasing the operation frequency. An n-symbol

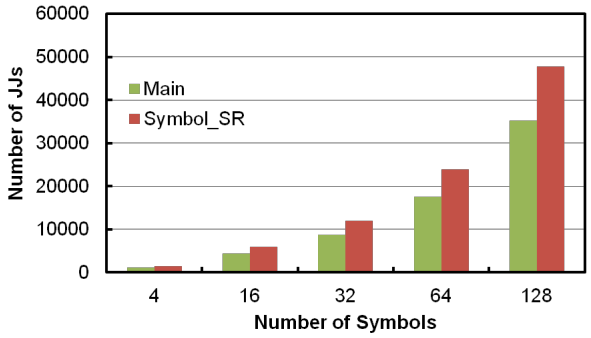

Fig. 7. Estimation of the number of Josephson junctions (JJs) as a function of the number of symbols

matching CED circuit is realized by placing n 1SMCs in series. We estimated the number of Josephson junctions of larger CED circuits in Fig. 7. The number of Josephson junctions increases in proportion to the number of symbols and becomes about 34000 in 128-symbol matching CED circuits. It was pointed out that about 50 % of viruses can be detected by matching 16 symbols in NIDS systems [3].

V. Adaptation to Regular Expressions

Because virus patterns are usually represented in regular expression in NIDS systems, we designed the 1SMCs, which are capable to process several basic regular expressions, including "ANY", "NOT", "OR" and "LOOP" function. "ANY" denotes that all input data are regarded as matched data. "NOT" means that input data other than the compared symbol are judged as matched data. "OR" represents the logical OR of the matching condition. For example OR(A, B) matches to the symbol "A" or symbol "B". "LOOP" means that one or more times of matching of input data is judged as matched data. We have already designed circuit schematics of 1SMCs for these regular expressions.

VI. Conclusion

We developed completion event detector (CED) circuits, which perform pattern matching and key elements in the completion event processing, by using single flux quantum (SFQ) circuits. We designed and implemented an 8-bit 4-symbol SFQ CED circuit by using the AIST ADP2 Nb process, and confirmed its correct operation at 52.1 GHz in the measurement. We considered the extension of the symbol number of CED circuits and showed that the circuit scale increases in proportion to the number of the symbols. We also considered CED circuits correspond to regular expressions and designed circuit schematics of 1-symbol matching circuits for several basic regular expressions.

Acknowledgment

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