

Design and Evaluation of Flash ADC

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Abstract — We have designed single-bit comparators and multi-bit flash ADCs using three flavors of periodic comparators; one flavor uses a differential “quasi-one-junction” SQUID (DQOS) comparator, the second use a differential SQUID wheel comparator and the third uses a symmetric differential SQUID wheel comparator with time-interleaved clocks. We have also developed a new performance analysis scheme that enables full reconstruction of input signal using a single-bit comparator. The signal is reconstructed based on multiple beat frequency measurements that track the position of the comparator thresholds in response to a DC offset to the input signal. In addition, to eliminate the frequency dependent distortions resulting from impedance mismatches over wide bandwidths, the signal and clock distribution network have been optimized using EM simulations. For distributing the clock signal to the multi-bit comparators, a 50 ohm coplanar transmission line has been designed. Test results for a 1-bit comparator using a differential SQUID wheel comparator demonstrates a performance of 4.5 bits of resolution in Gray code for a beat frequency test using a 20 GHz input signal and 5.3 bits for 10 GHz input. 4-bit and 8-bit versions of the flash ADC with a DQOS comparator and a 3-bit time-interleaved ADC using the SDSW comparator have also been designed. The DQOS ADC has been tested up to 25 GHz input signal frequency with performance of 4.3 bits of resolution in Gray code for 19.7 GHz input signal. The time-interleaved ADC performance is 4.3 bits for a 15 GHz beat frequency test with an effective sampling rate of 30 GHz.

Keywords (Index Terms) — Flash ADCs, periodic comparators, Analog-to-Digital Converter, SQUID Wheel.