Multi-input Synchronous Analog-to-Digital Converter

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Abstract — Integration of multiple synchronous identical superconductor analog-to-digital converters (ADCs) on a single chip or a multi-chip module is attractive for numerous applications, including Magnetic Resonance Imaging (MRI) systems. Several dual-ADC chips comprising two phase modulation-demodulation (PMD) ADCs with a common sampling clock, each connected to a digital decimation filter, have been designed. One variant with a single-junction quantizer with two-channel synchronizer and a decimation ratio of 256 has been installed in a modular cryocooled digital-RF receiver system (called ADR), operated with a common clock frequency of 20.48 GHz, and extensively tested with single and multiple input signals. Other variants have reduced decimation ratio for higher RF bands to digitize signals from higher-field MRI systems. Another variant of multi-input ADC integrated circuit chips have no on-chip filtering. We have designed and tested 2 (dual), 3 (tri), and 4 (quad) input versions of such a chip, where each ADC is followed by a deserializer circuit. A proof-of-concept multi-chip module (MCM) with 8 (octo) synchronous ADCs, consisting of four flipped dual-ADC chips on a carrier, has been designed to demonstrate scalability.

Keywords (Index Terms) — MRI, RSFQ, ADC, MCM, Digital Receiver.