Planarized, Extendible, Multilayer Fabrication Process for Superconducting Electronics

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Abstract — We report on technique and results for superconductor electronics fabrication process, featuring customizable number of planarized superconducting layers. The novel technique enhanced yield on stackable vias of our standard planarized process (RIPPLE) by eliminating the need for an additional deposition of Aluminum as an etch stop in the metal-via stack. The drawback of the previous approach was the difficulty in processing Aluminum using either wet or dry etch mechanisms. Here, we discuss details of the novel fabrication process flow and its realization for 4.5 kA/cm^2 fabrication process with six Nb layers with two fully planarized layers. We report test results of various planarization diagnostics structures, accounting the influence of topology on Josephson junction quality, as well as yield and critical current of via stacks. We also report on inductance measurement results providing information on interlayer dielectric thickness for planarized layers; confirming a good uniformity over the wafer. Basic components of superconducting logic such as dc/SFQ, SFQ/dc converters, Josephson transmission lines (JTLs), and simple digital circuits such as half-adder (HA) have been designed, fabricated and tested using either conventional (RSFQ) or energy-efficient (ERSFQ) approach. The ERSFQ HA cells with bias inductors fabricated in two planarized layers were shown to function with the operational margins of +/-22%.

Keywords (Index Terms) — Superconducting integrated circuits, Josephson junction fabrication, stackable vias, planarization