Fabrication Process and Properties of Fully-Planarized Deep-Submicron Nb/Al-AlO_x/Nb Josephson Junctions for VLSI Circuits

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Abstract — A fabrication process for Nb/Al-AlO_x/Nb Josephson junctions (JJs) with sizes down to 200 nm has been developed on a 200-mm-wafer tool set typical for a CMOS foundry. This process is a core of several nodes of fully-planarized fabrication processes developed at MIT Lincoln Laboratory for superconductor integrated circuits with 4, 8, and 10 niobium layers. The process utilizes 248 nm photolithography, anodization, high density plasma etching, and chemical mechanical polishing (CMP) for planarization of SiO_2 interlayer dielectric. JJ electric properties and statistics such as on-chip and wafer spreads of critical current, I_c, normal-state conductance, G_N, and run-to-run reproducibility have been measured on 200-mm wafers in a broad range of JJ diameters from 200 nm to 1500 nm and critical current densities, J_c, from 10 kA/cm^2 to 50 kA/cm^2 where the JJs become self-shunted. Diffraction-limited photolithography of JJs is discussed. A relationship between JJ mask size, JJ size on wafer, and the minimum printable size for coherent and partially coherent illumination has been worked out. The G_N and I_c spreads obtained have been found to be mainly caused by variations of the JJ areas and agree with the model accounting for an enhancement of mask errors near the diffraction-limited minimum printable size of JJs. I_c and G_N spreads from 0.8% to 3% have been obtained for JJs with sizes from 1500 nm down to 500 nm to be utilized in Single-Flux-Quantum circuits with J_c from 10 kA/cm^2 to 50 kA/cm^2. The spreads increase to about 8% for 200-nm JJs. Prospects for circuit densities > 10^6 JJ/cm^2 and 193-nm photolithography for JJ definition are discussed.

Keywords (Index Terms) — Nb/Al-AlO_x/Nb Josephson junctions, RSFQ, RQL, superconducting integrated circuit, superconductor electronics, self-shunted junction, 248-nm photolithography, minimum printable size, mask error enhancement