Design, Implementation and On-Chip High-Speed Test of SFQ Half-Precision Floating-Point Multiplier

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Abstract—We developed a large-scale reconfigurable data path (LSRDP) using single-flux-quantum (SFQ) circuits as a fundamental technology that can overcome the power-consumption and memory-wall problems in CMOS microprocessors in future high-end computing systems. An SFQ LSRDP is composed of several thousands of SFQ floating-point units connected by reconfigurable SFQ network switches to achieve high performance with low power consumption. In this study, we designed and implemented an SFQ floating-point multiplier (FPM), which is one of the key components of the SFQ LSRDP. We designed a systolic-array bit-serial half-precision FPM using the 2.5 kA/cm^2 Nb process. The resultant circuit area and number of Josephson junctions are 6.22 mm × 3.78 mm and 11044, respectively. The designed clock frequency is 25 GHz. We tested the circuit and confirmed the correct operation of the FPM by on-chip high-speed tests.

Index Terms—floating point units, LSRDP, multiplier, SFQ circuits, superconducting integrated circuits

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