Niobium 9-Layer Fabrication Process for Superconducting Large-Scale SFQ Circuits

Shuichi Nagasawa[1], Kenji Hinode[1], Tetsuro Satoh[1], Mutsuo Hidaka[1], Hiroyuki Akaike[2], Akira Fujimaki[2], Nobuyuki Yoshikawa[3], Kazuyoshi Takagi[4], and Naofumi Takagi[4]
[1]AIST, Tsukuba Central 2, 1-1-1 Umezono, Tsukuba, 305-8568, Japan
[2]Nagoya University, Furo-cho, Chikusa-ku, Nagoya 486-0913, Japan
[3]Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan
[4]Kyoto University, Yoshida-honmachi, Sakyo-ku, Kyoto 606-8501, Japan
E-mail: s-nagasawa@aist.go.jp

March 20, 2014 (HP72). We have been developing a niobium multi-layer fabrication process for large-scale single flux quantum (SFQ) circuits. We previously developed the Nb 10-layer fabrication process (ADP2) [1]. After that, since we could manage to compose the SFQ cell structure of the ADP2 without the top Nb layer, we eliminated it to reduce the load on the fabrication process. Figure 1 illustrates the device structure of the current Nb nine-layer fabrication process (ADP2). It is composed of an active layer including JJ and resistor layers at the top, passive transmission line (PTL) layers in the middle, and a DC power layer at the bottom. Although the upper two Nb layers (M8, M9) are not planarized, every other Nb layer (M1-M7) is planarized using the caldera planarization technology [2], [3]. The insulation between M6 and M7 layers is formed by using complemented caldera planarization technology, which enables us to place PTL1 and PTL2 patterns and C1-C5 contacts anywhere, even just below the junctions [1], [4]. This structure enables us to reduce the influence of magnetic fields due to large bias currents, since the active layer including the JJs, which are very sensitive for magnetic fields, is separated magnetically from the DC power layer and shielded by several ground planes (GND1, GND2, GND3, GP) [5]. This structure also enables us to form the Nb/AlOx/Nb junction layer in the last part of the fabrication process. Its advantages include reducing the damage that the JJs suffer during the fabrication and allowing the future utilization of a high-temperature process such as chemical vapor deposition (CVD) for fabricating the underlying layers of the JJs.

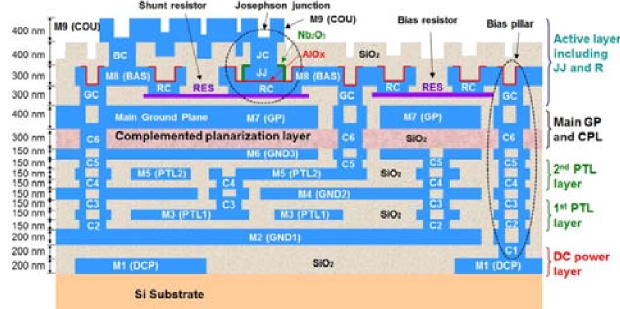

Fig. 1. Device structure of Nb 9-layer fabrication process (ADP2). JJ: Nb/AlOx/Nb junction, M1-M9: Nb layers, M2, M4, M6, M7: Ground planes, RES: Mo resistor (thickness: 45 nm), C1-C6, GC, RC, BC, JC: Contacts between metal layers, SiO_2: Interlayer insulator.

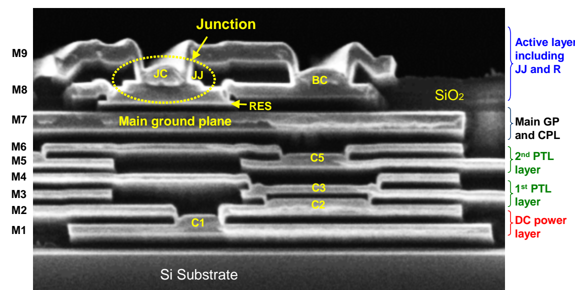

Fig. 2. Cross-sectional SEM photograph of device fabricated in Nb 9-layer process (ADP2). RC type junction (JJ), single contacts (C1, C5, BC, JC), and stack contact (C2/C3) are shown.

We used an RC type junction [6],

[7] to eliminate any degradation in JJ quality due to internal stress of the Nb films. The RC type junction also has the advantage of being able to reduce the circuit area, since part of the shunt resistor can be formed just below the junction. Optical proximity correction (OPC) patterns are used to reduce shrinkage in small junctions and to obtain critical current values that are linear with respect to the design sizes of the junctions [8]. The concave region on each contact is filled with SiO_2 to obtain a flat surface by caldera planarization [3], [6]. Therefore, the stack contact has a shape in which SiO_2 is sandwiched between upper and lower contacts. The electrical connection between them is made in the periphery region of the contacts. A multi-stack contact like a bias pillar [9] can be constructed by connecting several stack contacts vertically.

Figure 2 shows a cross-sectional SEM photograph of a device fabricated in Nb 9-layer process (ADP2). As shown in this figure, junction region was very flat despite the step edges of several underlying wirings and contacts.

Details of recent progress on the fabrication technology and process evaluation for ADP2 are described in the recent paper [10].

References

[1] S. Nagasawa, T. Satoh, K. Hinode, Y. Kitagawa, M. Hidaka, H. Akaike, A. Fujimaki, K. Takagi, N. Takagi, N. Yoshikawa, “New Nb multi-layer fabrication process for large-scale SFQ circuits,” *Physica C*, **469**, 1578-1584 (2009).

[2] K. Hinode, S. Nagasawa, M. Sugita, T. Satoh, H. Akaike, Y. Kitagawa, and M. Hidaka, “Pattern-size-free planarization for multilayered large-scale SFQ circuits,” *IEICE Trans. Electron*., **E86-C**, No. 12, 2511-2513 (2003).

[3] S. Nagasawa, K. Hinode, T. Satoh, H. Akaike, Y. Kitagawa, and M. Hidaka, “Development of advanced Nb process for SFQ circuits,” *Physica C*, **412-414**, 1429-36 (2004).

[4] T. Satoh, K. Hinode, S. Nagasawa, Y. Kitagawa, M. Hidaka, N. Yoshikawa, H. Akaike, A. Fujimaki, K. Takagi, N. Takagi, “Planarization process for fabricating multi-layer Nb integrated circuits incorporating top active layer,” *IEEE Trans. Appl. Supercond*., **19**, No. 3, 167-170, (2009).

[5] H. Akaike, K. Shigehara, A. Fujimaki, T. Satoh, K. Hinode, S. Nagasawa, and M. Hidaka: “The Effects of a DC Power Layer in a 10-Nb-Layer Device for SFQ LSIs”, *IEEE Trans. Appl. Supercond.*, **19**, No. 3, part 1, 594-597, (2009).

[6] S. Nagasawa, K. Hinode, T. Satoh, H. Akaike, Y. Kitagawa, and M. Hidaka, “Reliability evaluation of Nb 10 kA/cm2 fabrication process for large-scale SFQ circuits,” *Physica C*, **426-431**, 1525-1532 (2005).

[7] T. Satoh, K. Hinode, H. Akaike, S. Nagasawa, Y. Kitagawa, M. Hidaka, “Characteristics of Nb/AlO_x/Nb junctions fabricated in planarized multi-layer Nb SFQ circuits,” *Physica C*, **445-448**, 937-940 (2006).

[8] H. Akaike, Y. Kitagawa, T. Satoh, K. Hinode, S. Nagasawa, M. Hidaka, “ Effect of photomask pattern shape for a junction counter-electrode on critical current uniformity and controllability in Nb/AlOx/Nb junctions,” *IEEE Trans. Appl. Supercond.* **15**, No. 2, 102-105 (2005).

[9] H. Akaike, M. Tanaka, K. Takagi, I. Kataeva, R. Kasagi, A. Fujimaki, K. Takagi, M. Igarashi, H. Park, Y. Yamanashi, N. Yoshikawa, K. Fujiwara, S. Nagasawa, M. Hidaka, and N. Takagi: “Design of Single Flux Quantum cells for a 10-Nb-layer process”, *Physica C*., **469**, No. 15-20, 1670-1673 (2009).

[10] S. Nagasawa, K. Hinode, T. Satoh, M. Hidaka, H. Akaike, A. Fujimaki, N. Yoshikawa, K. Takagi, and N. Takagi, “Nb 9-layer fabrication process for superconducting large-scale SFQ circuits and its process evaluation,” *IEICE Trans. Electron*., **E97-C**, No. 3, 132-140 (2014).