Simulation of Superconducting Fault Current Limiters by means of Thermal–Electrical Analogy

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July 4, 2014 (HP82). We have recently reported on the use of the so-called "thermal-electrical analogy" for modeling and simulating Superconducting Fault Current Limiters (SFCLs) [1, 2]. With the thermal-electrical analogy the strong coupling between thermal and electrical phenomena is easier to handle, because the heat transfer equations become equivalent to RC electric circuit equations. Therefore the "thermal-electrical" problem can be mathematically reduced to just an electrical problem. The thermal-electrical analogy - including its mathematical basis - is described in detail in [1]. To our knowledge, there is a paucity of published papers employing this method to simulating SFCL devices, though some studies employed the thermal–electrical analogy to investigate the thermal behavior of SFCLs [3–7].

The electrical model represents each layer of a 2G high temperature superconductor (HTS) tapes as a resistor[1] [2]. The HTS layer is modeled as a variable non-linear resistor connected in parallel to ohmic resistors (substrate, silver solder layer and external shunt). The HTS characteristic of electric field (*E) versus* current desity (*J)* is approximated by a power law equation expressing the transition from superconducting to normal state. The heat transfer across the layers is modeled by using the thermal electrical analogy. In this analogy, the heat conduction of each material is represented by resistors, whereas thermal capacities correspond to capacitors. The convective heat transfer between wires and liquid nitrogen (LN2) is modeled as a "convective resistor". Internal heat generation at each layer is represented by current sources. A DC voltage source (77 V) simulates the LN2 bath (77 K).

Simulations agree quite well with results of short circuit tests undertaken at CEPEL. Simulated and measured limited currents can be seen in Figure 1 (left), as well as the simulated temperature rise in each layer of HTS wire and shunt of a commercial resistive SFCL component [2] (right). Figure 2 shows the simulated

[1] The model is also valid for 1G bulk monofilamentary BSCCO conductor used in earlier SFCL, such as those manufactured by Nexans.

thermal evolution of a resistive SFCL module consisting of commercial bulk-Bi2212 components [1]. These results are supported by Finite Element Method simulations and temperature measurements under the same conditions [8].

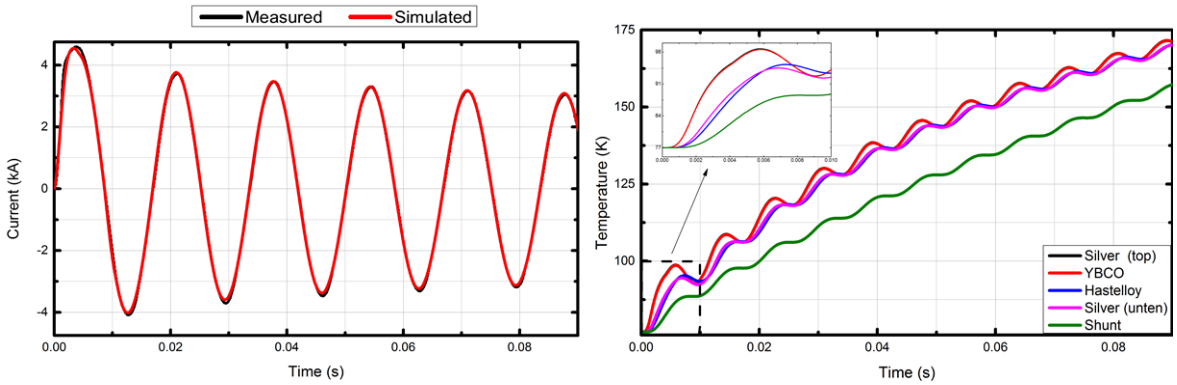

Fig. 1. Experimental and simulated limited currents (left) and simulated temperature rise in each layer of 2G HTS tape (asymmetrical fault current = 53 kA_{peak} (20 kA_{rms}); Vo = 200V_{rms} , right).[2]

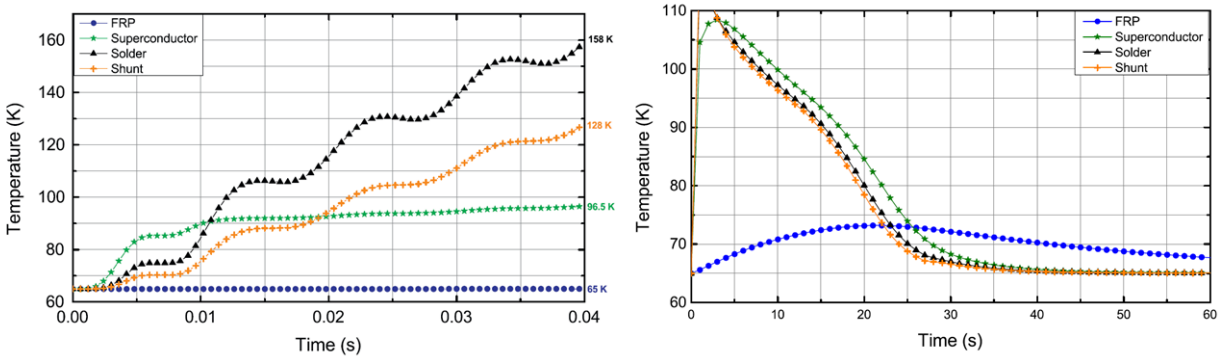

Fig. 2. Simulated temperature rise (left) and cooling after fault clearing (right) of bulk Bi-2212 components of a SFCL module cooled at 65 K (fault current = 10 kA_{rms}; Vo = 650 V_{rms}). The temperature of each subcomponent is shown, including the solder layer between Bi-2212 and shunt (FRP = Fiber Reinforced Plastic) [1].

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