MIT LL Superconductor Electronics Fabrication Processes for VLSI circuits with
4, 8, and 10 Niobium Layers

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Abstract — We present a review of superconductor electronics fabrication processes developed at MIT Lincoln Laboratory for very large scale integrated (VLSI) circuits with 4, 8, and 10 Nb metal layers and Nb/Al-AlO_x/Nb Josephson junctions (JJs). The processes utilize 248-nm photolithography and chemical mechanical polishing of SiO_2 interlayer dielectric for planarization of all layers. The current process node offers minimum feature size of 350 nm for Nb wiring layers, Josephson junctions with critical current density of 10 kA/cm^2 (100 μA/μm^2) and minimum size of 700 nm. The process salient features and characterization is given and our roadmap to achieving circuit densities of 10^6 JJs per cm^2 and beyond is discussed.

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