Progress with Physically and Logically Reversible Superconducting Digital Circuits

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Abstract - We continue to develop a new Superconductor Flux Logic (SFL) family based on nSQUID gates with fundamentally low energy dissipation and the ability to operate in irreversible and reversible modes. Prospective computers utilizing the new gates can keep conventional logically irreversible architectures. In this case the energy dissipation is limited by fundamental thermodynamic laws and could be as low as a few kBTs per logic operation. Highly exotic and less practical logically and physically reversible circuit architectures are more attractive for us because they allow to reduce specific energy dissipation well below thermodynamic threshold kBTln2. The reversible option attracts us because we like to experimentally demonstrate that all technical mechanisms of the energy dissipation could be cut below the fundamental thermodynamic mechanism. In other words, we like to set the absolute energy dissipation record for all conventional digital technologies that (if measured in kBT) is about one million times below the best figures achieved in commercially available semiconductor circuits. Besides, we believe that diving below the thermodynamic threshold would have impressive scientific and philosophical impacts. In the paper we introduce a new timing belt clocking scheme and present new circuits. We still work with test circuits but some of them contain two 8-stage shift registers, one with direct and the other with inverted outputs.

The energy dissipation per nSQUID gate per bit measured at 4 K temperature is already below the thermodynamic threshold. So we are confident that we passed through the critical phase of the project and we simply need more time to make more sophisticated circuits. The extremely low energy dissipation converts our circuits into a natural candidate to support circuitry for any sensors operating at milli-Kelvin temperatures.

Index Terms - Superconductor digital devices, reversible computing.

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