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JCMOS: Josephson-CMOS Hybrids

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***Abstract*—There has been a longstanding expectation that SFQ-DRAM hybrids would address the spatial inefficiency of SFQ memory, yet the point of this talk is that the opportunities for Josephson-CMOS hybrids (coined JCMOS) are far greater. A true hybrid, in the sense of a GaAs-CMOS hybrid being proposed for 6G telecom, would not just support circuits with both DRAM transistors and Josephson junctions, but would allow designing-in logic transistors, floating-gate (Flash) transistors, varactors, memristors, sensors, and a host of other devices that are already present in CMOS processes. The additional devices would increase design flexibility and enable new applications.**

While superconducting multi-chip modules will be essential for interconnect at scale, true hybrid integration would allow connections that could be treated as an equipotential or wire rather than a transmission line, avoiding the need for line drivers and enabling circuits that seamlessly span the two technologies without undue dissipation. This talk will cover the physical structure of a true Josephson-CMOS hybrid, electrical issues for the vias between technologies, new circuit design opportunities, and a system vision.

The new opportunities will be explained through use of an exemplary Semiconductor to Single-Flux Quantum (S2SFQ) data link. S2SFQ's function overlaps with a DC-to-SFQ converter, but it would have far lower dissipation in certain future-looking applications (e.g., a JJ Field-Programmable Gate Array). The key semiconductor device in S2SFQ is a (variable) capacitor, not a transistor, which is an unexpected design twist (as far as I know).

To preview the circuit, the variable capacitor (varactor) connects a wire carrying an SFQ pulse to ground. A CMOS voltage controls the capacitance, changing the SFQ pulse in a way that influences SFQ circuits. If the CMOS voltage has low bandwidth compared to the SFQ signal rate, such as FPGA configuration signals, there will be only static dissipation in the semiconductor devices (where a DC-to-SFQ converter requires CMOS data transitions for every SFQ pulse generated).

The talk will conclude with identification of some challenges and future directions. Cryo-CMOS and Josephson junctions could be tweaked to further improve the long-term benefits. The talk will discuss how semiconductor reversible logic and changes to MOSFET threshold voltages could make CMOS more effective in the hybrid. Some proposed fundamental enhancements to Josephson junctions would help as well. In addition, current processes support (something like a) 10 µm cross-technology via with barely tolerable resistance. A future direction would be shorter stacks with less resistance.

***Keywords (Index Terms)*—Cryo-cmos, sfq, Josephson Junction, cmos+X, vco, varactor**

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