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Cryogenic Electrical Interfaces for Large-Scale Spin-Qubit Quantum Processors

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***Abstract*—Quantum computers are not yet able to tackle practical computational problems because current prototypes only offer too few (<1000) quantum bits (qubits) compared to the millions required for future applications. To follow and support such a growth in quantum-processor complexity, the electrical interface required for controlling and reading the qubits must also scale accordingly. In particular, wiring an increasing number of cryogenic qubits to their room-temperature control electronics will soon hit a brick wall due to the sheer size of the required wires, their cost, and their limited reliability. Such an interconnect bottleneck can be alleviated by operating a cryogenic electronic controller close to the qubits. Realizing such a vision comes, however, with several challenges, as it requires highly complex electronics able to operate at cryogenic temperatures and dissipate very low power to be compatible with the cooling budget of practical refrigerators while delivering high enough performance (in terms of control signal purity, readout sensitivity, and speed) not to limit the quality of the quantum operations.**

Integrated circuits fabricated in commercial CMOS technologies and operating at cryogenic temperatures below 4 K (cryo-CMOS) are consolidating as the preferred choice for these applications by leveraging the very large scale of integration (VLSI) offered by CMOS technologies. Still, several hurdles must be overcome, such as 1) understanding the cryogenic CMOS device behavior and developing reliable device models for efficient circuit simulation and design; 2) holistically optimizing the system by co-designing and co-simulating the quantum and classical components; 3) demonstrating all the required functionalities for signal generation and acquisition and optimizing power/area efficiency of the cryo-CMOS circuits. This talk will address those challenges by analyzing the physical behavior of cryo-CMOS devices and by describing state-of-the-art design examples of both circuits and larger systems with cryo-CMOS electrical interfaces for spin qubits hosted in semiconductors and diamonds. We will highlight future challenges and opportunities regarding device characterization and modeling, circuit design, design automation, and (hybrid) co-integration, thus laying out a roadmap toward the scalable electrical interfaces supporting the future large-scale spin-qubit computers able to make a difference in relevant applications.

***Keywords (Index Terms)*— Quantum computing, cryogenic electronics, CMOS, Cryo-CMOS, Cryogenics**

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