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Progress Towards High-density Superconductor Digital Logic

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***Abstract*–Superconductor digital logic offers compelling advantages in both speed and energy efficiency as a beyond-CMOS technology for demanding applications in digital computing and signal processing. Recent developments in advanced chip-scale fabrication processes and multi-chip packaging strategies show encouraging results towards achieving the integration scales necessary for the most promising applications. This talk will present recent progress at MIT Lincoln Laboratory on fabrication process modules for advanced nodes aimed at increasing circuit density to ~10^8 JJs/cm^2, including self-shunted junctions (Nb/Al-AlOx/Nb, Nb/NbNx/Nb and NbN/NbNx/Nb) and high-kinetic-inductance elements. In addition, recent results on shift-register diagnostic circuits provide guidance on how mitigation of flux trapping is an important factor in process stack-up design as circuit densities increase. Finally, recent results on utilizing both passive and active superconducting large-area carriers for multi-chip integration will be reviewed.**

***Keywords (Index Terms)*–Digital, Flux Pinning, Josephson Devices, Nanofabrication**

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