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Keys needs in the technology roadmap for superconductor electronics

D. Scott Holmes
International Roadmap for Devices and Systems (IRDS)
2022-10-24 ASC **1EOr2B-01**

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Keys needs in the technology roadmap for superconductor electronics

Abstract

A technology roadmap for superconductor electronics is under development within the framework of the International Roadmap for Devices and Systems (IRDS). Significant technology improvements are required for superconductor electronics to meet the needs expected for applications such as quantum computing, artificial intelligence, or large-scale digital computing. Metrics for improvement include circuit density, chip or system complexity, and energy efficiency. Key needs are identified in areas including fabrication processes, devices, logic families, and system architectures. Metrics and methods are under development to evaluate potential solutions for the key needs. A challenge is that evaluation of overall benefit often requires large-circuit or system-level modeling, which can be difficult without the necessary electronic design automation (EDA) tools.

Presenter: D. Scott Holmes

Applied Superconductivity Conference

2022 October 24–28, Honolulu, Hawaii, USA
https://www.appliedsuperconductivity.org/asc2022/

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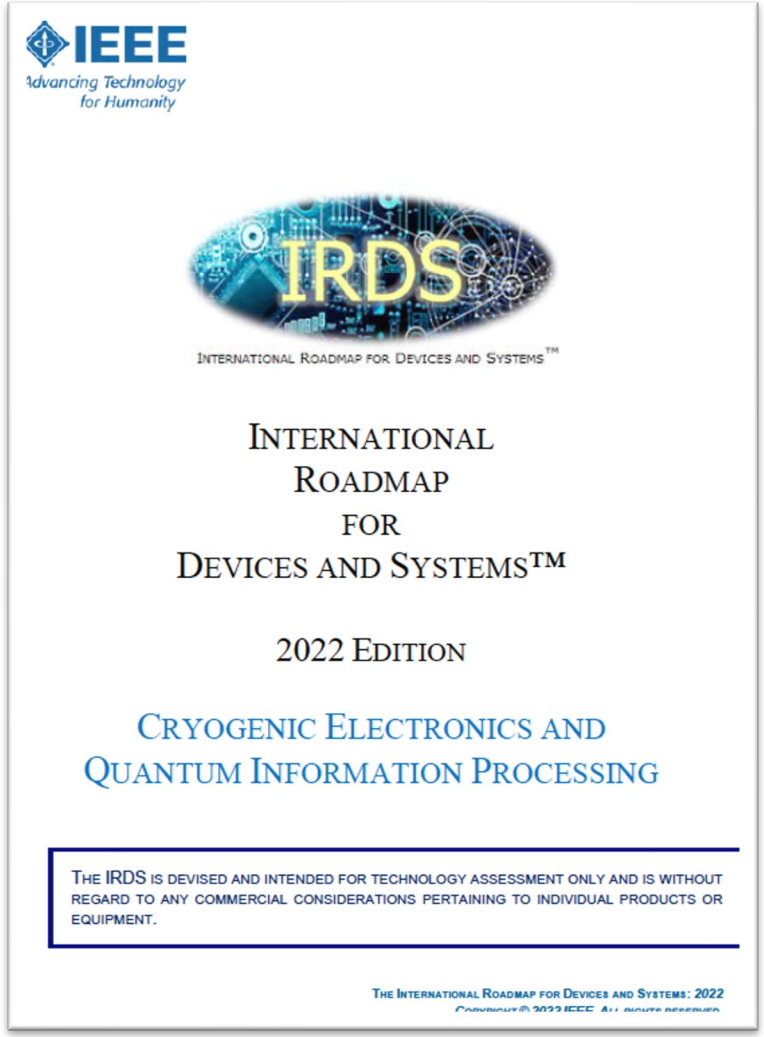
2022 IRDS CEQIP summary

- Coverage
  - Superconductor Electronics (SCE)
  - Cryogenic Semiconductor Electronics
  - Quantum Information Processing (QIP)
- Key Messages from the 2022 report
  - SCE: Partial roadmaps
  - QC: Not yet ready for roadmaps
- Summary slides:
  - Difficult Challenges
  - Technology Requirements
  - Potential Solutions
- Updates
  - New Technology Requirements
  - Breakthroughs in Technology, Research
  - New Disruptors
  - Potential Solutions
- Conclusions and Recommendations

Available:
https://irds.ieee.org/editions



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2023 CEQIP Members

Name	Area	Organization	Region
Byun, Ilkwon	Cryo-Semi, QIP-QC	Seoul National University, Korea	Asia
Cuthbert, Michael	Cryo, QIP	National Quantum Computing Centre, UK	Europe
DeBenedictis, Erik	QIP-QC	Zettaflops, USA	Americas
Fagaly, Bob	SCE-App	Honeywell (retired), USA	Americas
Fagas, Giorgios	QIP	Tyndall National Institute, Ireland	Europe
Febvre, Pascal	SCE-Fab	Université Savoie Mont Blanc, France	Europe
Filippov, Timur	SCE-Log	Hypres, USA	Americas
Fourie, Coenrad	SCE-EDA	Stellenbosch University, South Africa	Africa
Frank, Mike	SCE-Log, -Rmap	Sandia National Laboratories, USA	Americas
Gupta, Deep	SCE, Cryo-Semi	SEACORP, USA	Americas
Herr, Anna	SCE-Logic, -Rmap	IMEC, Belgium	Europe
Holmes, D Scott [Chair]	SCE, Cryo-Semi, QIP	Booz Allen Hamilton, USA	Americas
Humble, Travis	QIP-QC	Oak Ridge National Laboratory, USA	Americas
Leese de Escobar, Anna	SCE-App, -Bench	Navy NIWC-PAC, USA (retired)	Americas
Min, Dongmoon	Cryo-Semi, QIP-QC	Seoul National University, Korea	Asia
Mueller, Peter	QIP-QC-SC	IBM Zürich, Switzerland	Europe
Mukhanov, Oleg	QIP-QC, SCE-Log	Seeqc, USA	Americas
Nemoto, Kae	QIP	The National Institute of Informatics (NII), Japan	Asia
Papa Rao, Satyavolu	SCE-Fab, QIP	SUNY Polytechnic, USA	Americas
Pelucchi, Emanuele	QIP-QC	Tyndall National Institute, Ireland	Europe
Plourde, Britton	QIP	Syracuse University, USA	Americas
Soloviev, Igor	SCE	Lomonosov Moscow State University, Russia	Europe
Tzimpragos, George	SCE-Logic, -Metrics, -Rmap	University of Michigan, USA	Americas
Vogelsang, Thomas	Cryo-Semi	Rambus, Inc., USA	Americas
Weides, Martin	SCE, QIP	University of Glasgow, UK	Europe
Yoshikawa, Noboyuki	SCE-Log, -Bench	Yokohama National University, Japan	Asia
You, Lixing	SCE	SIMIT, CAS, China	Asia

Additions for 2023

13: Americas
9: Europe + Africa
5: Asia

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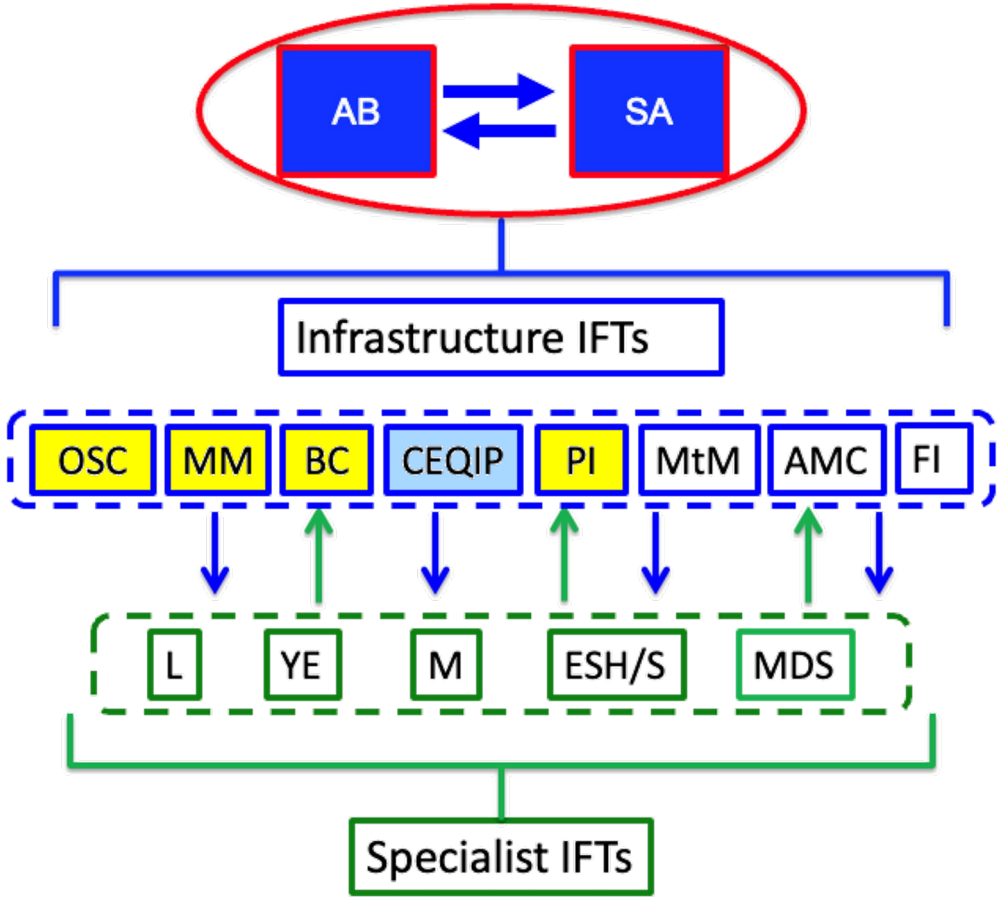
IRDS IFT Cross-team and Collaborative Alignments

IFT: International Focus Team

- CEQIP primary interactions with IRDS teams
  - **AB**: Application Benchmarking
  - **SA**: Systems and Architectures
  - **BC**: Beyond CMOS
  - **MM**: More Moore
  - **OSC**: Outside System Connectivity
  - **PI**: Packaging and Integration

- External Organizations (contact person)
  - IEEE Quantum Initiative (Erik DeBenedictis)
  - QED-C: Quantum Economic Development Consortium (Erik DeBenedictis)
  - UK National Quantum Computing Centre Roadmap (Michael Cuthbert)



IFT structure of the IRDS

2022 IRDS Executive Summary, Fig. ES35

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2022 Report: Superconductor Electronics (SCE)

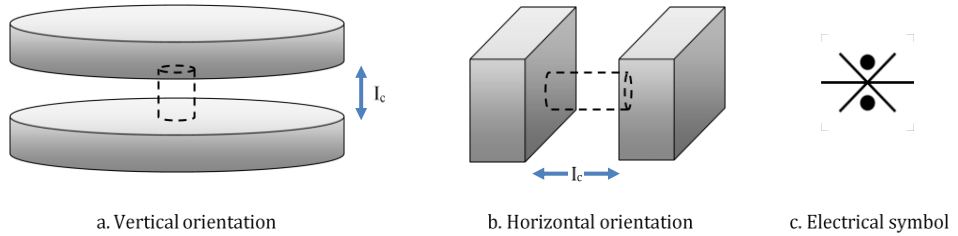

Figure CEQIP-1. Josephson Junction Device Structures

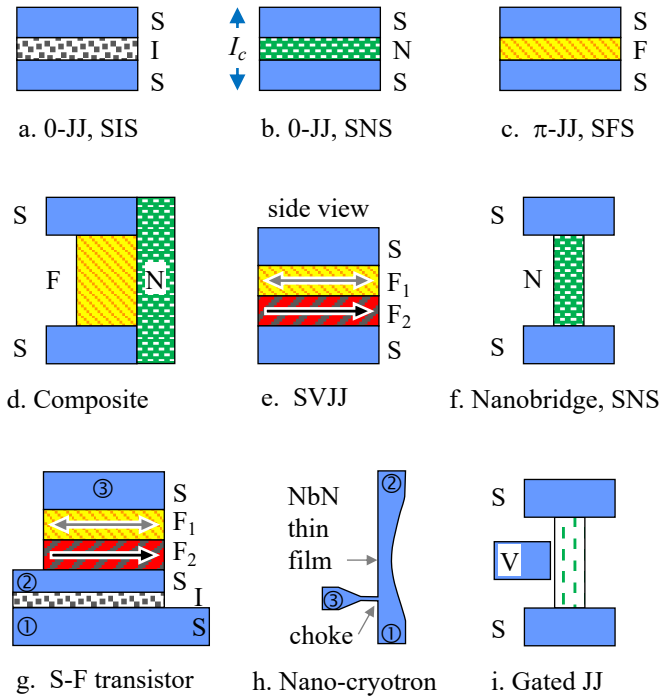

Figure CEQIP-3. Superconductor (S) switching devices

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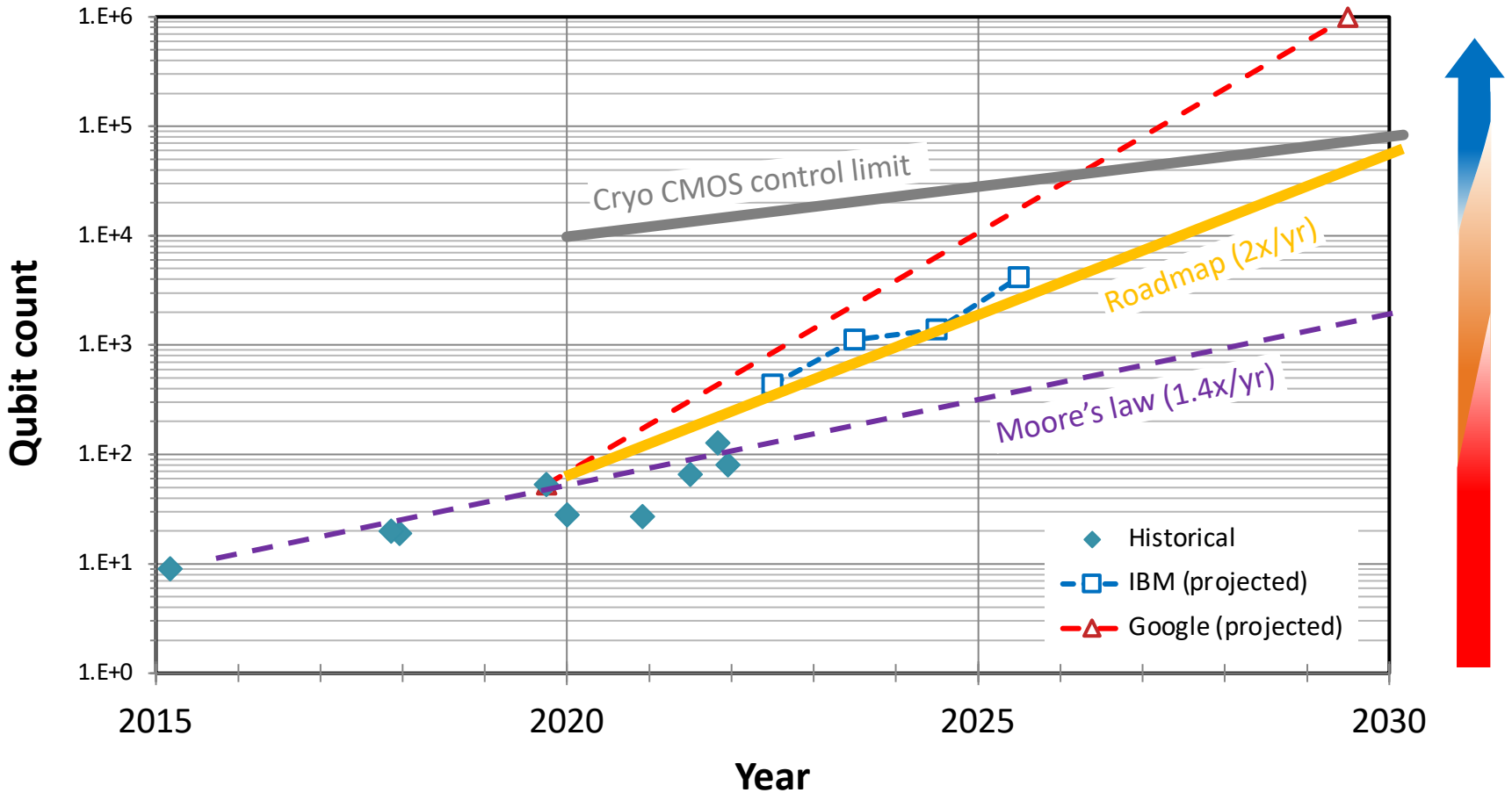
2022 SCE Roadmap Status

- Status summary
  - SCE is a developing technology with a small market and big promise
  - Quantum information processing (QIP) is currently a driver
  - Logic: Many competing approaches
  - Memory: Little available; no clear solutions
  - Fabrication: Research + some commercial (slow progress)
- Technology roadmap benefits
  - Provide metrics and goals to guide effort and to evaluate alternatives
  - Identify key needs for research and development

Application: Superconducting Quantum Computing

Superconducting qubit roadmap

~ 2.7x/year



Control:

Superconductor
~ 4 K

Semiconductor
~ 4 K

External
~ 300 K (RT)

Google: https://www.cnet.com/tech/computing/quantum-computer-makers-like-their-odds-for-big-progress-soon/

IBM: https://research.ibm.com/blog/ibm-quantum-roadmap-2025

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2023 Superconducting QC Roadmap, First Cut

Metric	2020	2022	2024	2026	2028	2030	2032
Qubit growth per year	2×	2×	2×	2×	2×	2×	2×
Qubit count	5.5e+1	2.2e+2	8.8e+2	3.5e+3	1.4e+4	5.6e+4	2.2e+5
Qubit type	Transmon	Transmon	Transmon	Transmon	?	?	?
Qubit lifetime T1, med. [ms]	0.5					10	
2 qubit gate error rate, median (p_2Q)	1.0e-2					1.0e-4	
Gate depth (1/p_2Q)	1.0e+2					1.0e+4	
Error correction code	Surface	Surface	Surface	Surface	Surface	Surface	?
Phys. qubits per logical qubit				1000	1000	1000	1000
Logical qubit count				3	14	56	220
Logical qubit error rate						1.0e-15	
Control type, temp. [K]	CMOS, 300	CMOS, 300	CMOS, 300	CMOS, 4	CMOS, 4	CMOS, 4	SCE, 4
SCE control complexity [JJ]	1.1e+5	4.5e+5	1.8e+6	7.2e+6	2.9e+7	1.2e+8	4.6e+8

In Progress

- ASC 2022 Oct 27 09:00, **4EOr1C-01**, Holmes

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2021 DIFFICULT CHALLENGES (SCE)

Technology Road Blocks…Highlight gaps and showstoppers, possible disconnects within the roadmap

- Near term (2020-2027)
  - EDA tools for superconductor electronics
    - EDA tools for CMOS are not adequate for SCE. Inductance is critical in superconducting circuits and connecting wires must have inductance values within a specified range. Circuit simulators and timing analysis must be modified.
  - PDKs for fabrication processes
    - Complete process design kits (PDKs) are needed for fabrication processes for superconductor electronics.
  - Yield improvement of circuits with > 1 M Josephson junctions (switching devices)
    - Variation in device parameters reduces the operating margins of circuits. Needed is better process control, better device designs, or circuit designs that tolerate or compensate for device variability.
- Long term (2028-2035)
  - Temperature limits compatible with CMOS fabrication processes
    - Nb/Al-AlO_x/Nb Josephson junctions are sensitive to temperature. Temperatures are currently limited to < 200 °C, which requires different processes than CMOS technology, which has a limit of 400 °C.
  - Optical input/output (I/O)
    - Communication with room-temperature systems and networks will require a high-data-rate I/O, but interconnection cannot introduce significant heat into a low-temperature environment. Optical fiber digital links would be ideal, but efficient SFQ-to-optical converters must be developed.
  - Magnetic materials fabrication process integration
    - Magnetic materials are desired to make both memory and passive devices. Integrating magnetic materials into foundry processes will be difficult.

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2022 Difficult Challenges (Near-term) for SCE

Technology roadblocks, gaps, and possible disconnects within the roadmap

Near-Term Challenges: 2022–2029	*Summary of Issues (why is it a challenge?)*
Logic (current implementations)	• Many competing approaches • Sensitivity to magnetic fields and fabrication variation • Supply current is mostly spent biasing junctions • Power and clock pulse distribution add complexity and jitter • Scalable to solve big problems (DSP, AI, QC, HPC)
Memory	• Density is too low for single-flux-quantum memory (like SRAM) • Multiplexing is difficult for single-flux-quantum logic • New materials and processes add cost
Phase shift elements	• Present approach (external supply current through inductors) does not scale. DC bias is ~ 0.7 *Ic* per junction, so chip supply current becomes too large for > 1 million junctions. Inductors require shielding. • Phase batteries such as pi junctions require new materials, device layer.
NbN or NbTiN fabrication process	• NbN and NbTiN now deposited by reactive sputtering, which is difficult to make uniform across a 200 mm or 300 mm diameter wafer • CVD or ALD processes will require development

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2022 Difficult Challenges (Long-term) for SCE

Technology roadblocks, gaps, and possible disconnects within the roadmap

Long-Term Challenges: 2030–2037	*Summary of Issues (why is it a challenge?)*
Switching device scalable below 200 nm	• Nb/Al-AlOx/Nb Josephson junctions are almost good enough • Alternatives will require different materials and fabrication processes, possibly including magnetic materials
3-terminal switching device	• Small available flux ~ 2 mA·pH or voltage ~ 1 mV • Fabrication more difficult than the traditional tri-layer device
Integrated circuit fabrication processes	• Foundries for commercial production now process 200 mm or smaller wafers using equipment lacking state-of-the-art capability. • Temperatures are currently limited to < 200 °C, which requires different processes than CMOS technology, which has a limit of 400 °C. • Circuit approaches and fabrication processes are interdependent, requiring co-development. • Magnetic materials need to be added.
Optical input/output (I/O)	• Heat budget in the low-temperature environment is very low. • Optical data links require development of efficient SFQ-to-optical converters.

- But can these wait?

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Key Need Areas

for superconductor electronics (SCE)

1. Power supply
2. Sensitivity to external magnetic fields, currents, and trapped flux
3. Area reduction
4. Logic
5. Memory
6. Fabrication for scale

Other

1. Design tools
2. Testing

1. Power Supply

Approaches for improvement:

1. DC Serial biasing
2. AC to DC
3. AC power distribution

DC Supply Current to Bias JJs

Biasing sets signal flow direction ➔

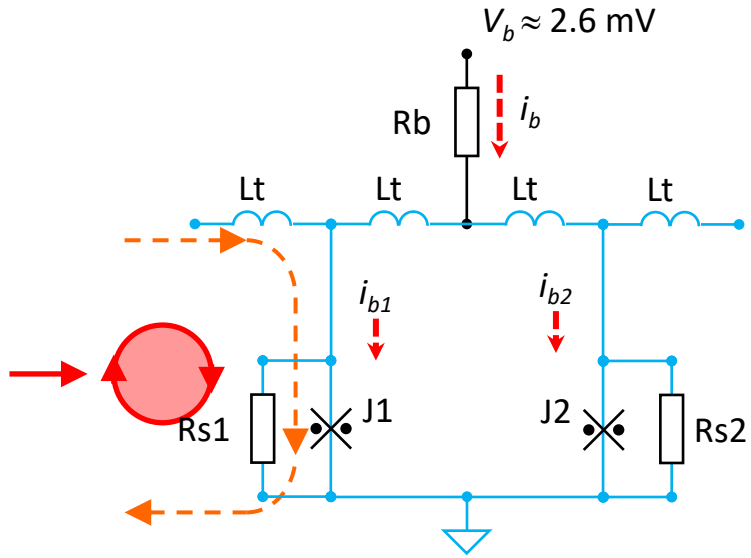
- $I_C \approx 100$ µA (constraints: thermal noise, switching energy)
- $K_0 \approx 0.7$ (bias current ratio, $K_0 \equiv i/I_C$)
- $\alpha \approx 0.5$ (fraction of biased junctions)

- Bias current for 1 million junctions in parallel?

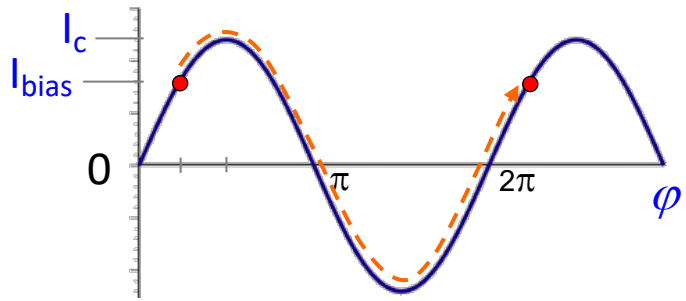
$$I_b = N\, I_C\, K_0\, \alpha = (1e{+}6)(100e{-}6)(0.7)(0.5) = 35\ A$$

- Way too much current and not nearly enough junctions!

▸ Traditional DC biasing will not scale.



Junction bias in RSFQ



$$i = I_c \sin(\phi)$$

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Supply Current: Recycling

DC bias current

- Pass DC bias current through a series of *N* ground plane 'islands'
  - *N* = 16 demonstrated with highly regular circuits (shift registers) [1]
- Advantages
  - *N*× bias current reduction
- Disadvantages
  - Clock, data nets also require separation
  - Area multiplier ≈ 1.5× (??)
  - JJ return current paths can affect margins
  - Complexity of balancing island currents
  - Capacitive coupling between floating islands
  - Ground plane gap shields needed

▸ Perhaps the first thing to try

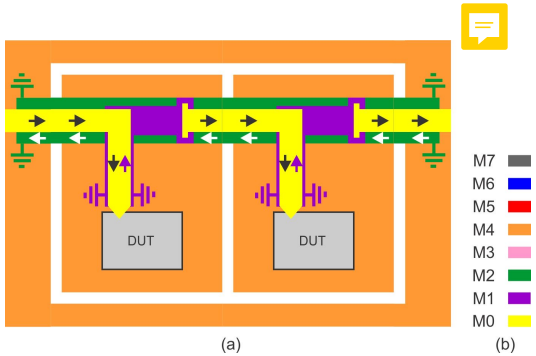

Fig. 1. Grapevine distribution of DC bias currents. [2]

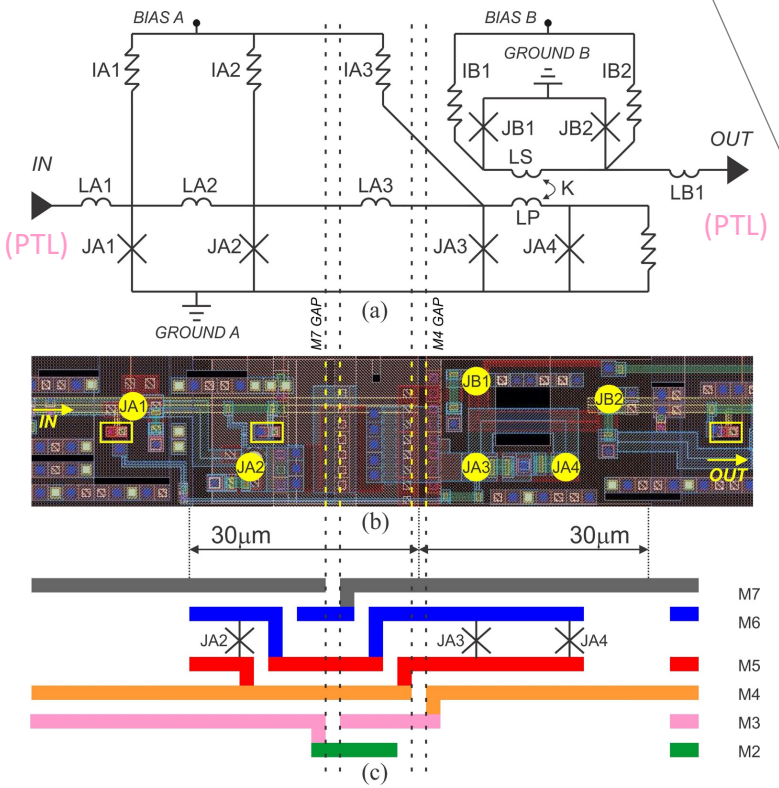

Fig. 2. Driver-receiver pair (DRP) to transfer clock and data pulses between islands. [2]

[1] Semenov+, "Current recycling: New results," 2019, doi: 10.1109/TASC.2019.2904961

[2] Shukla+, "Serial biasing technique for electronic design automation in RSFQ circuits," 2022, doi: 10.1109/TASC.2022.3214767

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Supply Current: AC/DC Conversion

- Convert AC to DC on chip using rectifiers [1, 2] or local flux biasing [3]
- Best used with logic cells that require AC or **no** bias current
- Advantages
  - AC supply to converters in series, so can supply more cells (≈ 100× ?)
- Disadvantages
  - Complexity, area overhead factor ≈ 2× (?)
  - Transformers don't scale well
  - $f_{AC} > f_{clock}$ for best energy efficiency
  - Need to design more logic cells that use AC or no bias current

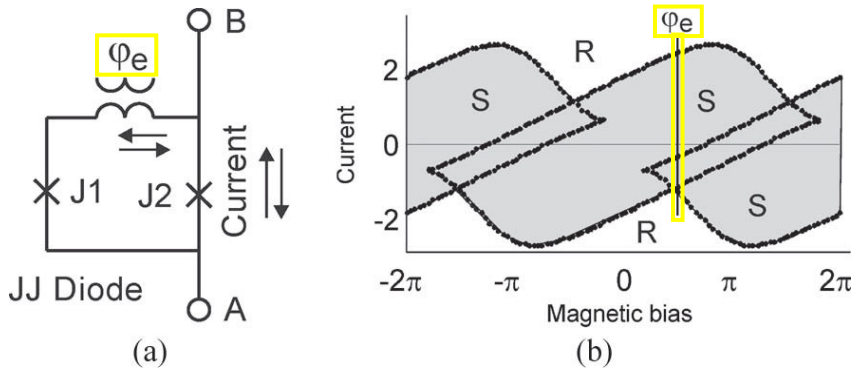

Fig. 1. Rectifier based on a magnetically biased SQUID. [1]

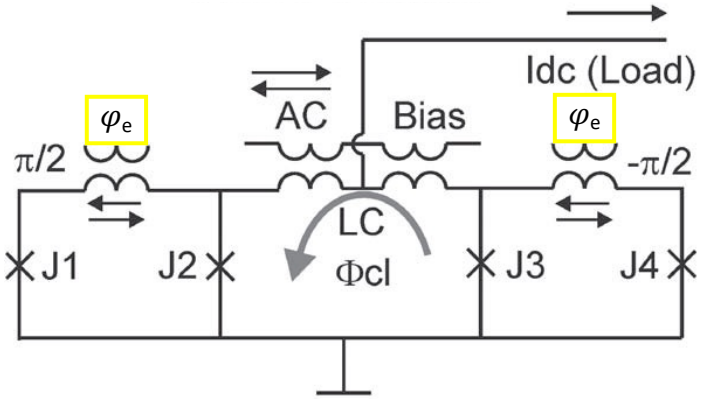

Fig. 2. AC/DC converter. [1]

[1] Semenov+, 2015, doi: 10.1109/TASC.2014.2382665

[2] Semenov+, 2017, doi: 10.1109/TASC.2017.2669585

[3] Asada+, 2021, doi: 10.1088/1361-6668/abf23a

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Supply Current: AC/SFQ Conversion

- Better: Convert AC to SFQ (not DC) on chip using rectifiers
- Best used with logic cells that require AC or **no** bias current
- Advantages
  - AC supply to converters in series, so can supply more cells (≈ 1000× ?)
- Disadvantages
  - Complexity, area overhead factor ≈ 2× (?)
  - Transformers don't scale well
  - $f_{AC} > f_{clock}$ for best energy efficiency
  - Need to design more logic cells that use AC or no bias current

▸ Needs further investigation

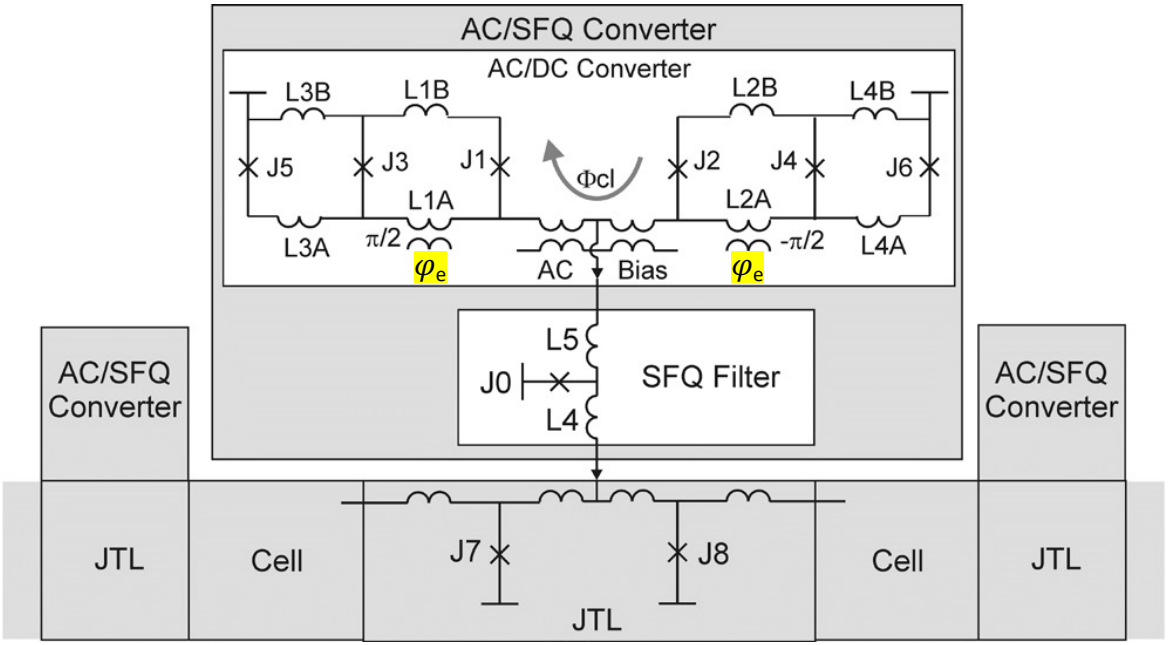

Fig. 3a. AC/SFQ converter supplying a JTL. [1]

[1] Semenov+, 2021, doi: 10.1109/TASC.2021.3067231

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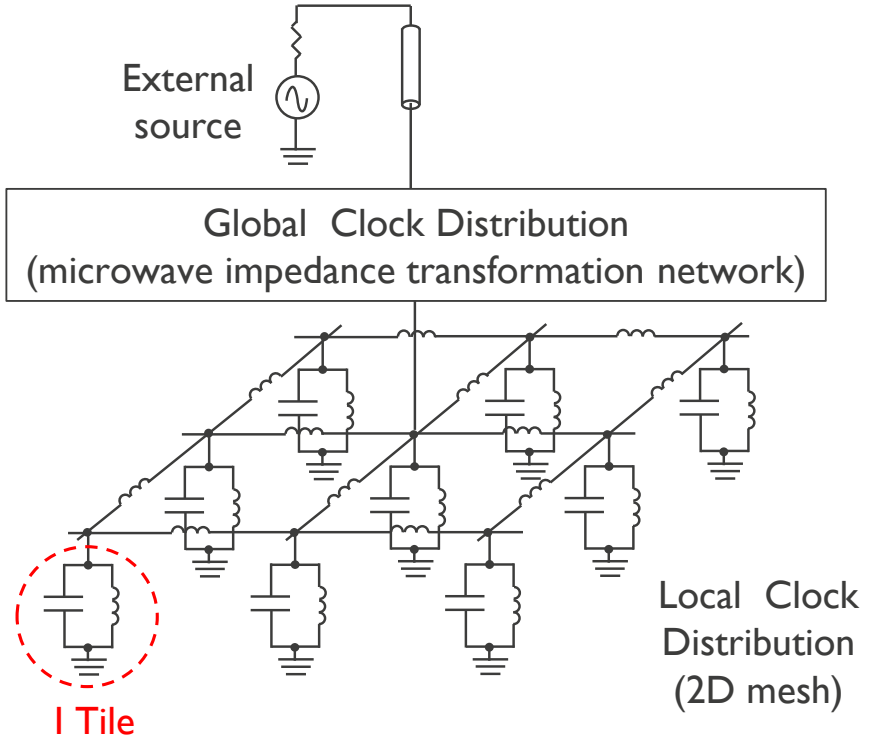
AC Power Distribution

Design concept for large-scale clock distribution

- Local storage of power and clock signal in high-Q LC-resonators
  - 1 resonator per tile
- 2D mesh of LC resonators has a zero-order mode
  - Clock signal distribution over large area with only small amplitude and phase variation
- 30 GHz design with 400 M taps/cm^2



▸ ASC 2022 Oct 26 14:30, **3EPo2B-06** [E11], Q. Herr

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2. Sensitivity to external magnetic fields, currents, trapped flux

Approaches for improvement:

1. Moat design
2. Phase-shift devices
3. “Inductorless” circuits with small mutual inductances

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Phase Engineering: φ Junctions

One Junction to rule them all?

- Storing element compaction [1]

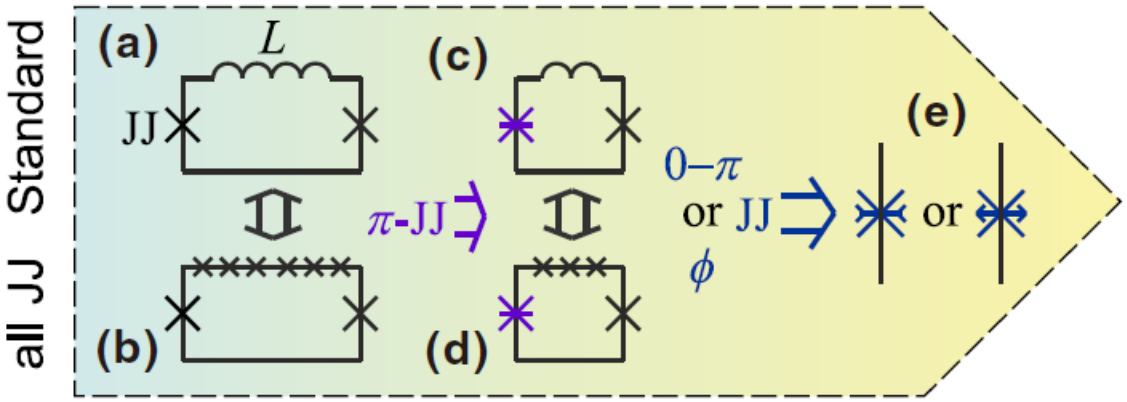

Fig. 1

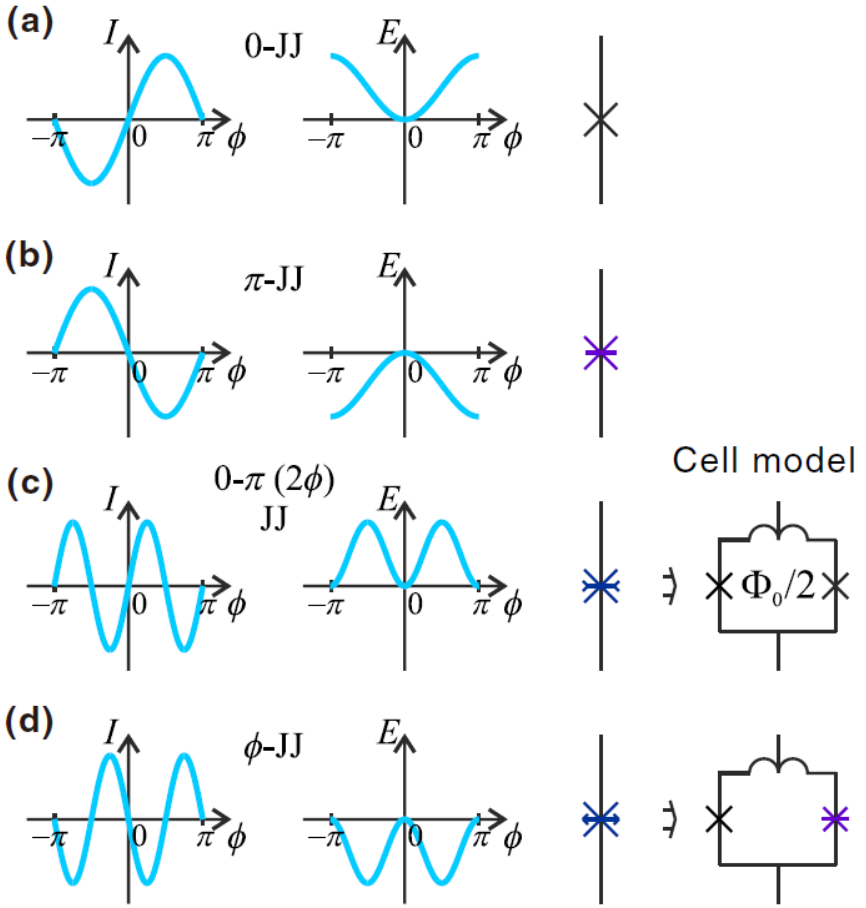

Fig. 2

- Question:
  - Can the devices be made?

[1] I. I. Soloviev, "Superconducting circuits without inductors based on bistable Josephson junctions," 2021, doi: 10.1103/PhysRevApplied.16.014052

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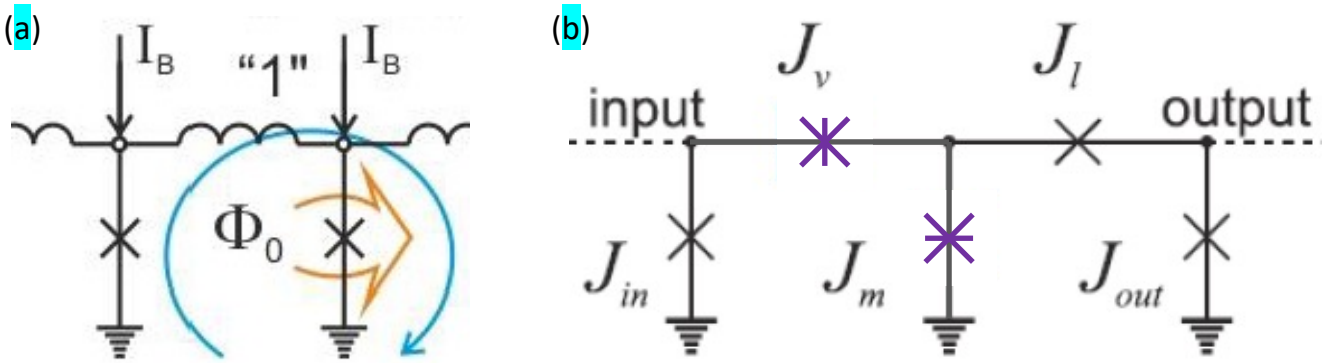
"Inductorless" circuits with small mutual inductances

Non-traditional Josephson junctions to replace inductors, reduce JJ count

- Junction types
  - 0 junctions (SIS), switching
  - **0 junction stacks** (SNsNsNS)
  - **π junctions** (SFS)
  - **ϕ junctions** [1], [3]

- Questions:
  - Can the devices be made?
  - And with sufficiently small parameter variations (I_c, L)?



[1] (a) JTL with inductors, (b) JTL with magnetic junctions

[1] Soloviev +, "Superconducting circuits without inductors based on bistable Josephson junctions," 2021, doi: 10.1103/PhysRevApplied.16.014052.
[2] Maksimovskaya +, "Phase logic based on π Josephson junctions," 2022, doi: 10.1134/S0021364022600884.
[3] Bakurskiy +, "Compact Josephson ϕ-junctions," 2018, doi: 10.1007/978-3-319-90481-8_3.

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3. Area Reduction

Approaches for improvement:

1. Inductors
2. Transformers (miniaturization, replacement, or avoidance)
3. Passive transmission lines (PTL)
4. Josephson junction (JJ) size reduction

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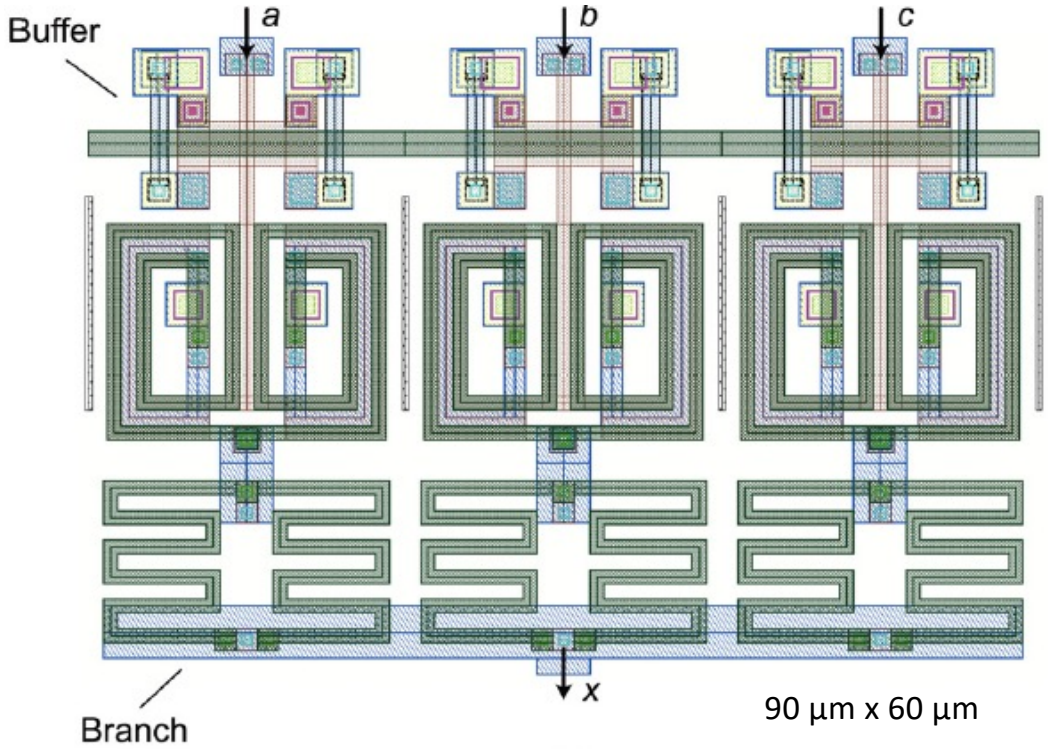
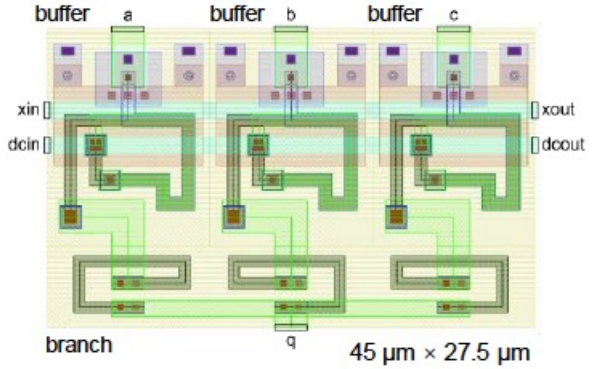
Gate set example: AQFP (MAJ+INV)



(Output inversion takes no additional area)



Takeuchi+, **2015**, doi: 10.1063/1.4919838

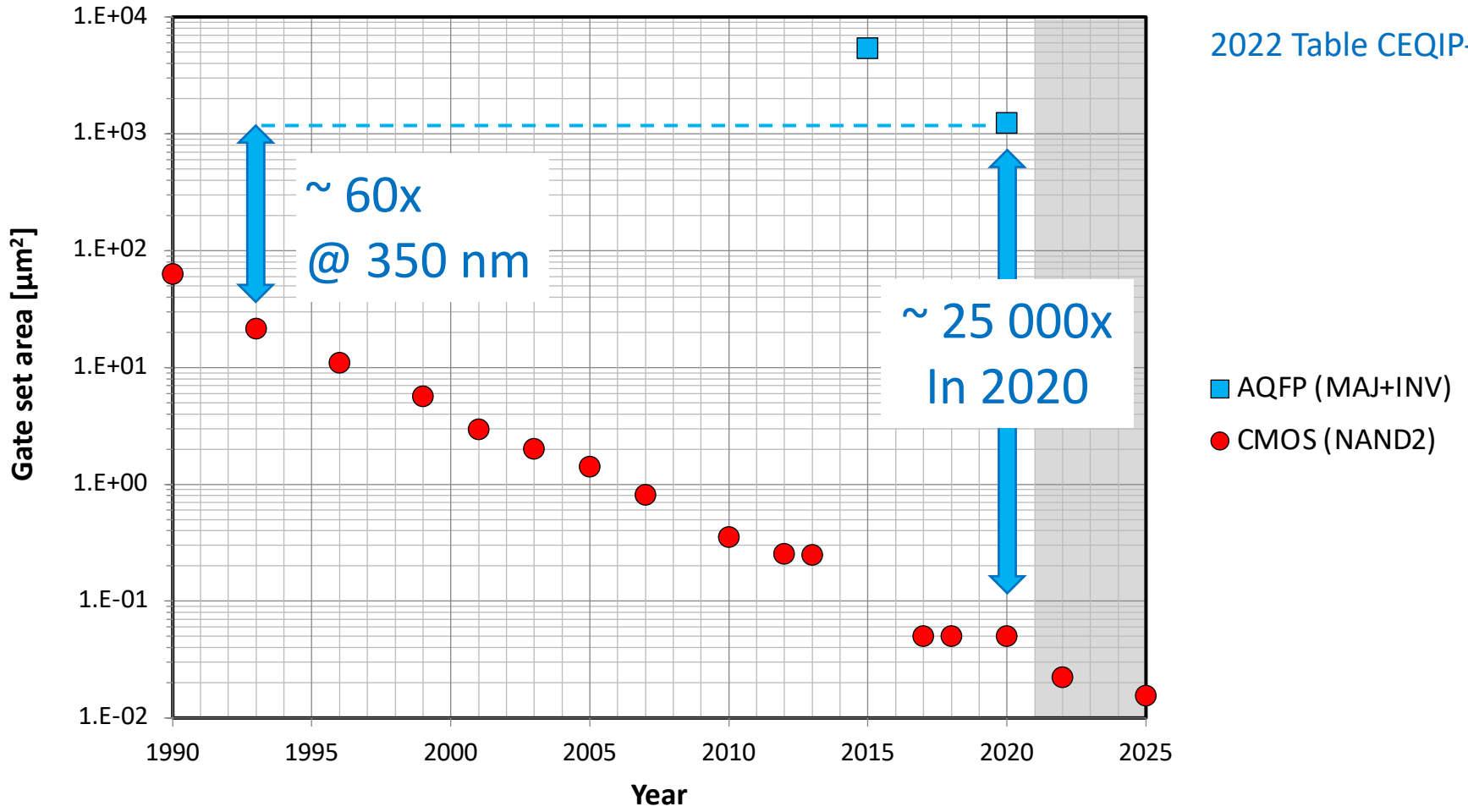
- AIST STP2 process
- M = F = 1500 nm
- 4 Nb layers, 1 JJ layer
- Jc = 25 MA/m^2
- Area = 5400 µm^2

1238/5400
= 0.23 ~ 1/4

He+, **2020**, doi: 10.1088/1361-6668/ab6feb

- MIT-LL SFQ5ee process
- M = F = 350 nm
- 8 Nb layers, 1 JJ layer
- Jc = 100 MA/m^2
- Area = 1238 µm^2

Gate Set Area: Comparison with CMOS



2022 Table CEQIP-5

- Why is SCE logic area so much larger? (= lower density)

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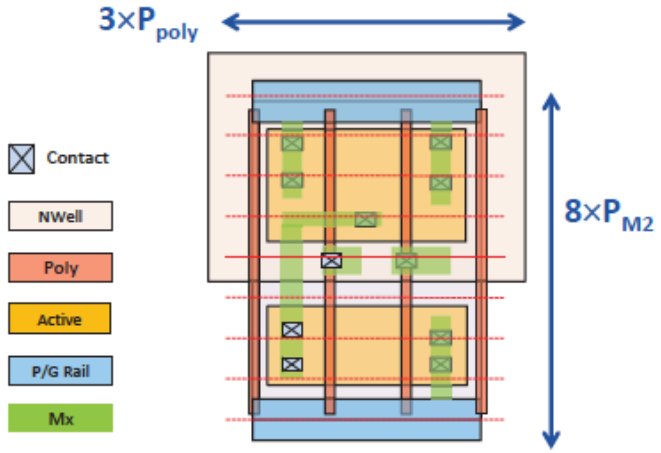
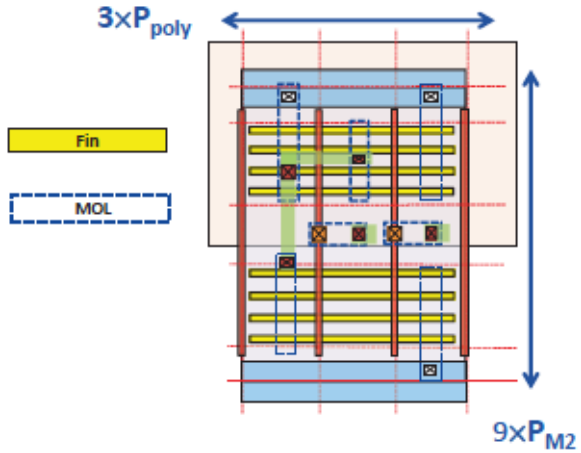
Gate sets: CMOS (NAND2) vs AQFP (MAJ+INV)

NAND2
(4 bulk planar FETs, 2011)



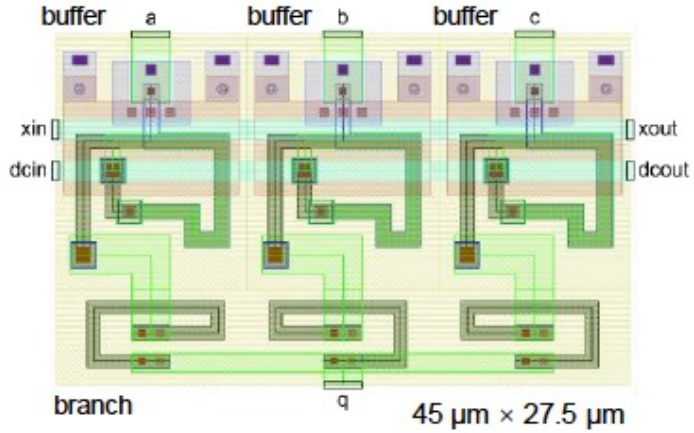
$U_{logic} = 3P_{poly} \times 8P_{M2} = 180F^2$
calibrated → $175F^2$

NAND2
(4 FINFETs, 2013)



$U_{logic} = 3P_{poly} \times 9P_{M2} = 162F^2$
calibrated → $155F^2$

MAJ+INV
(6 JJs, 2020)



Chan+, 2014, doi: 10.1109/ICCD.2014.6974675
- NAND2 area (bulk FET, ITRS 2011) = 175 F^2
- NAND2 area (FINFET, ITRS 2013) = 155 F^2

He+, 2020, doi: 10.1088/1361-6668/ab6feb
- MIT-LL SFQ5ee process, M = F = 350 nm
- MAJ area = 1238 μm² = 1238/(0.35)²
  = 10,106 F^2

10,106/175
= 58

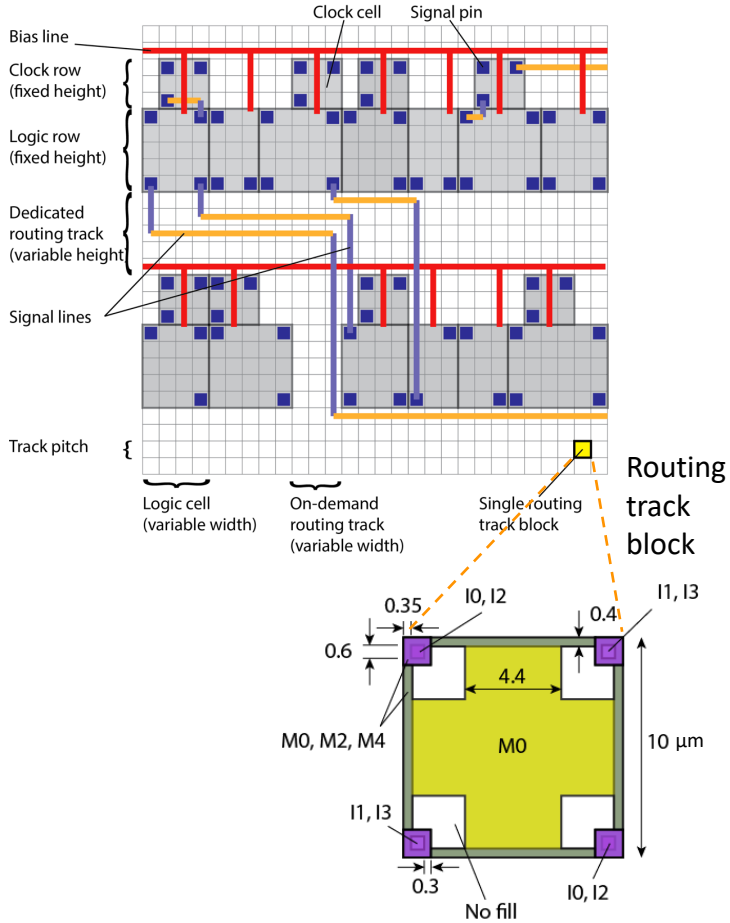
Need to reduce the factor of ~ 60

Circuit area reduction

SCE approaches

- Wiring layers: increase 8 → 10 → ?
- Inductor size
  - Decrease wire width or thickness
  - Use multiple wiring layers
  - Increase JJ current I_c (but $E_{switch} \propto I_c$)
  - High kinetic inductance layers
  - JJ stack inductors?
  - Transformers don't scale well (Tolpygo, 2022, arXiv:2210.02632)

    ▸ ASC 2022 Oct 25 14:15, **2EPo2F-01**, Tolpygo
- JJ size
  - Area $\propto 1/J_c$
  - No shunt resistor needed if $J_c \gtrsim 500$ μA/μm^2
  - Multiple JJ layers
  - Device options?



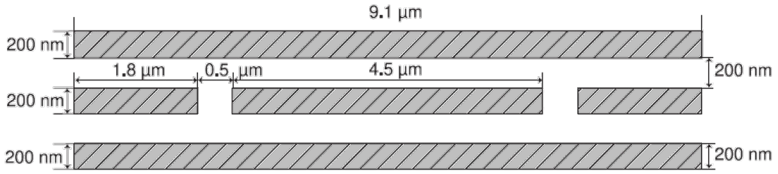
Row-based place-and-route architecture for RSFQ
Fourie+, 2020, doi: 10.1109/TASC.2020.2988876

▸ Needed: models to guide roadmapping

Passive transmission lines (PTL)

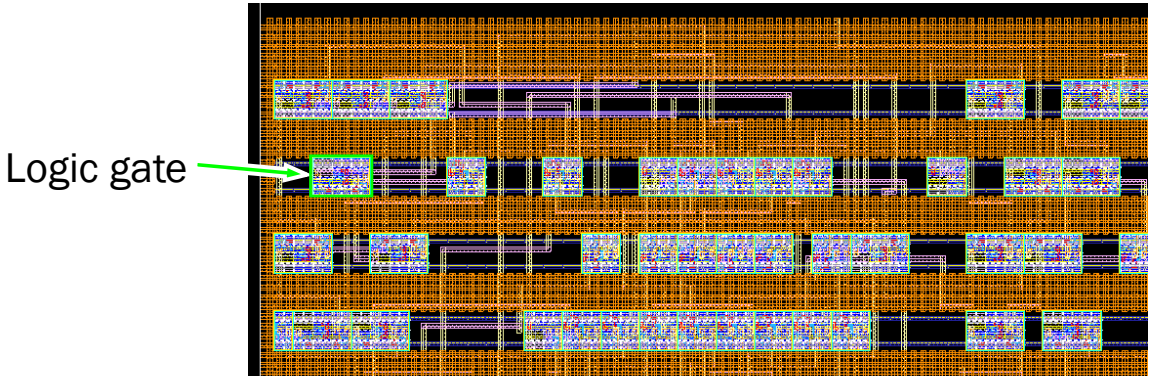
Important interconnects

- PTL width (~ 4 μm) is a major obstacle to scaling
  - JJs are low impedance drivers
  - Reducing the PTL width increases impedance, which causes reflections due to impedance mismatch
  - Reducing JJ Ic increases impedance, but reduces pulse energy
- Using only PTLs for routing requires too much area
- Additional PTL layers would increase area density but require +2 metal layers each



PTL cross section

Herbst +, 2020, doi: 10.1109/TASC.2020.3006988



AMD2901 4-bit processor design with 16,840 gates (upper left portion of overall layout)

Placed and routed in Synopsys **Fusion Compiler** (FC) and viewed in Custom Compiler

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4. Logic

Approaches for improvement:

1. AC clocking
2. Clock reduction or elimination
3. Data representation
4. Phase-shift devices
5. Macro blocks or cell-abutment logic
6. Neuromorphic Circuits
7. Quantum phase-slip junctions (QPSJ)
8. Multi-terminal (3+) switching devices

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Superconductor Digital Logic Families

2022 Summary of current status

Name	*SFQ*	*Power*	*Static Power*	*Dynamic power per switch*	*Trans-formers*	*Clocked Gates*	*JJ count $log_{10}(n)$*
RSFQ: rapid single flux quantum	1	– DC	High	$\alpha I_c \Phi_0 f$	-	Yes	4.4
LR-RSFQ: inductor-resistor RSFQ	1	– DC	Low	$\alpha I_c \Phi_0 f$	-	Yes	1.6
LV-RSFQ: low-voltage RSFQ	1	– DC	Low	$\alpha I_c \Phi_0 f$	-	Yes	3.7
ERSFQ: energy-efficient RSFQ	1	– DC	0 *	$I_b \Phi_0 f$	-	Yes	3.8
eSFQ: efficient SFQ	1	– DC	0 *	$I_b \Phi_0 f$	-	Yes	3.4
Clockless SFQ	1	– DC					2.8
DSFQ: dynamic SFQ	1	– DC	‡	‡	-	Some	0.7
TSFQ: temporal SFQ	1	– DC			-	No	(2.8)
xSFQ: alternating SFQ	2	– DC	‡	‡	-	No	
nTron: nanowire cryotron	1	– DC	~0	varies	-	Yes	1.5
hTron: heater-cryotron nanowire	1	– DC	~0	varies	-	Yes	1.2
HFQ: half flux quantum	0.5	– DC	Low		-	Yes	1.2
SFQ-AC: AC-powered SFQ	1	~ AC	‡	‡	P	Yes	5.9
RQL: reciprocal quantum logic	2	~ AC	~0	$\alpha I_c \Phi_0 f$ 2/3	P, G	Some	4.9
PML: phase mode logic	1	~ AC	~0	$\alpha I_c \Phi_0 f$ /3	P, G	Some	
AQFP: adiabatic quantum flux parametron	-	~ AC	~0	$\alpha I_c \Phi_0 2 f \tau_{sw}/\tau_x$	P, G	Yes	4.3
RQFP: reversible QFP	-	~ AC	~0	$\alpha I_c \Phi_0 2 f \tau_{sw}/\tau_x$	P, G	Yes	1.4

Other metrics?

- Area
- Current
- Logic depth
- JJ per gate
- Scalability

2022 Table CEQIP-4

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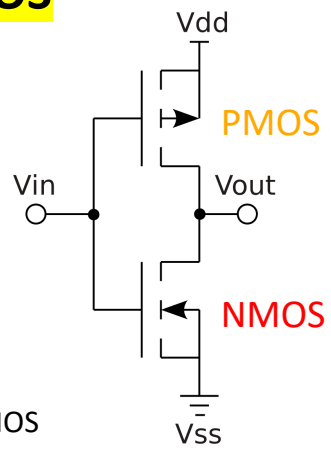
Searching for a winning combination

Semiconductor logic families

1960s	1980s
ECL	ECL
DTL	DTL
TTL	TTL
NMOS	NMOS
PMOS	PMOS
CMOS	**CMOS**



en.wikipedia.org/wiki/CMOS

Superconductor logic families

2010s	2030s
– RSFQ	
– ERSFQ	
– eSFQ	
– DSFQ	
– HFQ	?
– nTron	
– xSFQ	
~ SFQ-AC	
~ RQL	
~ PML	
~ PCL	
~ AQFP	
~ DQFP	
~ RQFP	

Considerations:

- Performance
- Power
  - Static
  - Dynamic
  - Supply
- Cost
  - Ease of design
  - Area
  - Fabrication process
  - Yield
  - Shielding
- Compatibility
- …

▸ ASC 2022 Oct 24 18:00, **1EOr2B-06**, Tzimpragos

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AC Clocking

Use AC power as the clock

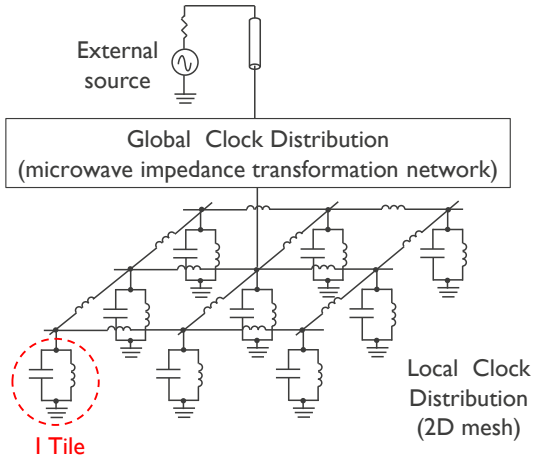
- AQFP (most established)
  - **Advantages**: JJs are all the same size and small (50 μA), energy efficient, good margins, majority logic
  - **Disadvantages**: large area, transformers, clocked gates, memory (?), majority logic
- Reciprocal quantum logic (RQL)
  - **Advantages**: Few JJs per logic gate, good margins, proven
  - **Disadvantages**: transformers, clock frequency limits, EDA tool support (?), controlled by Northrop Grumman
- **Pulse conserving logic (PCL)**
  - 12 levels of logic at 30 GHz
  - OMA3 gate (OR3/MAJ3/AND3)

New!

▸ ASC 2022 Oct 25 14:15, **2EPo2F-06** [E40], T. Josephsen

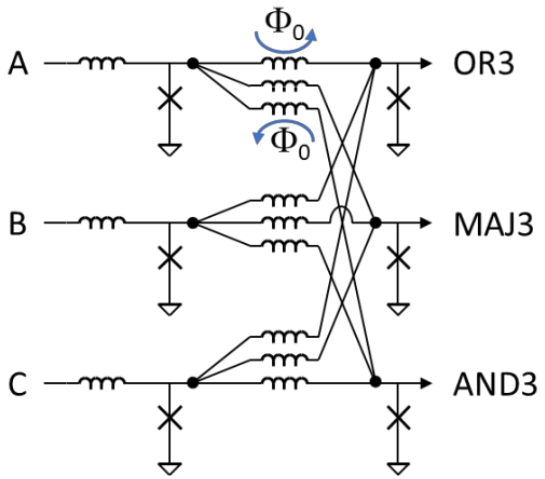
Design concept for large scale clock distribution
2D array of tightly coupled local, lumped LC resonators

- Local storage of power and clock signal in high-Q LC-resonators
  - 1 resonator/tile (1 tile ~5x5 μm²)
- 2D mesh of LC resonators has a zero-order mode
  - Clock signal distribution over large area with only small amplitude and phase variation



- 30 GHz design with 400 M taps/cm²

▸ ASC 2022 Oct 26 14:30, **3EPo2B-06** [E11], Q. Herr



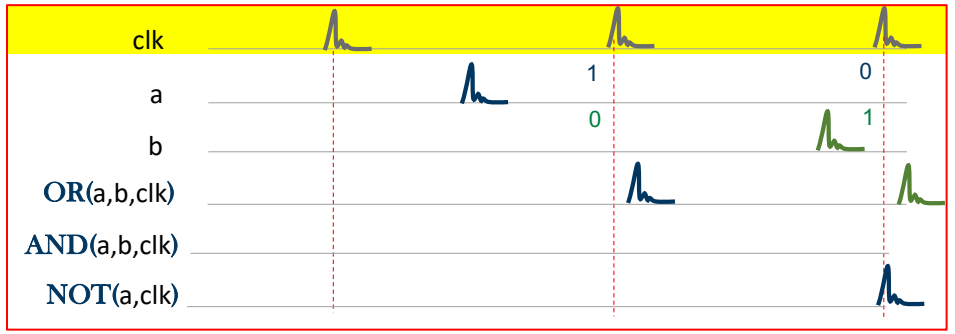
Clock Reduction or Elimination

Overhead multiplies the cost of clocking!

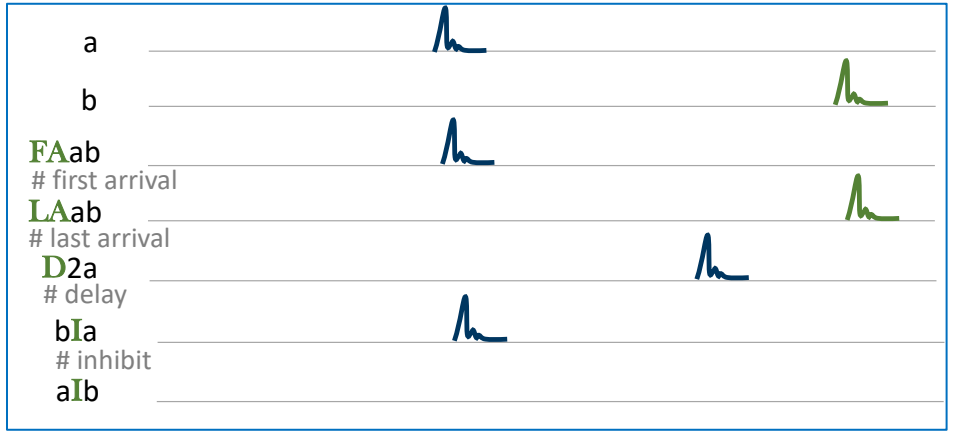
- Bias current overhead estimates **per clocked gate**:
  - ≈ 1.5× (?) for clocking (splitters, mostly)
  - ≈ 4× (?) for path balancing (superlinear)
  - ≈ 20× (?) for unused clock time (allowing for jitter, long lines, pipeline hazards, etc.)
  - ≈ 1.5× (?) for higher fraction of JJs that switch
- ≈ 180× (?) total

▸ Reduce or eliminate clocked cells

Clocked SFQ [1]



Temporal SFQ [1]



[1] Volk, "Circuit Abstractions for Low-Cost Fan-Out," ISCA, 2022

[2] Tzimpragos +, 2020, doi: 10.1145/3373376.3378517

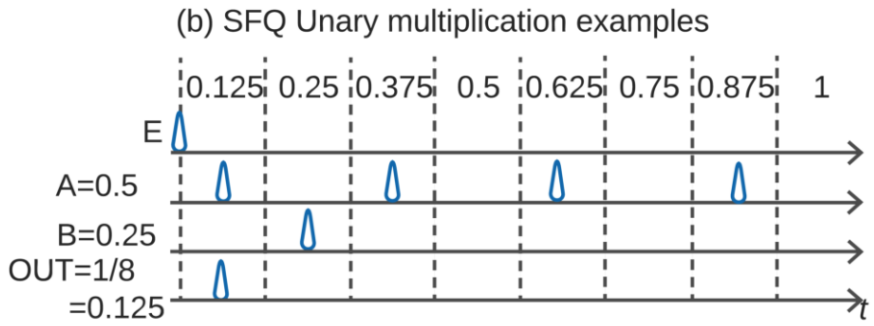
[3] Tzimpragos +, 2021, doi: 10.1109/ISCA52012.2021.00057

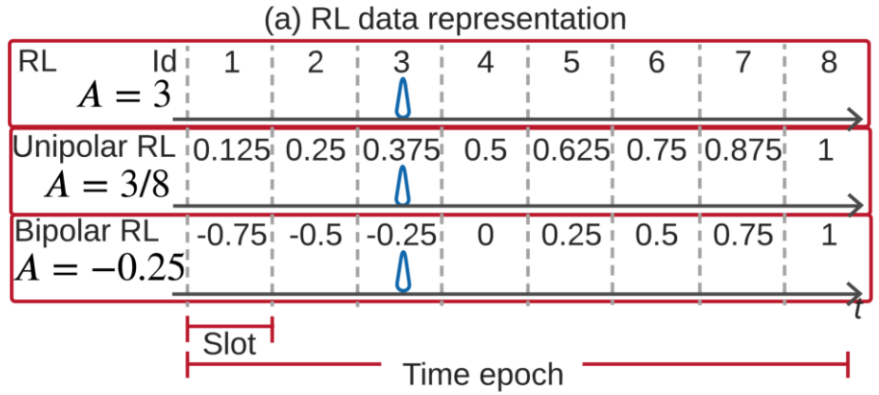
IEEE-CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), March 2023; Submitted October, 2022; Selected October, 2022. Presentation 1EOr2B-01 given at Applied Superconductivity Conference, Honolulu, HI, USA, October 24, 2022.

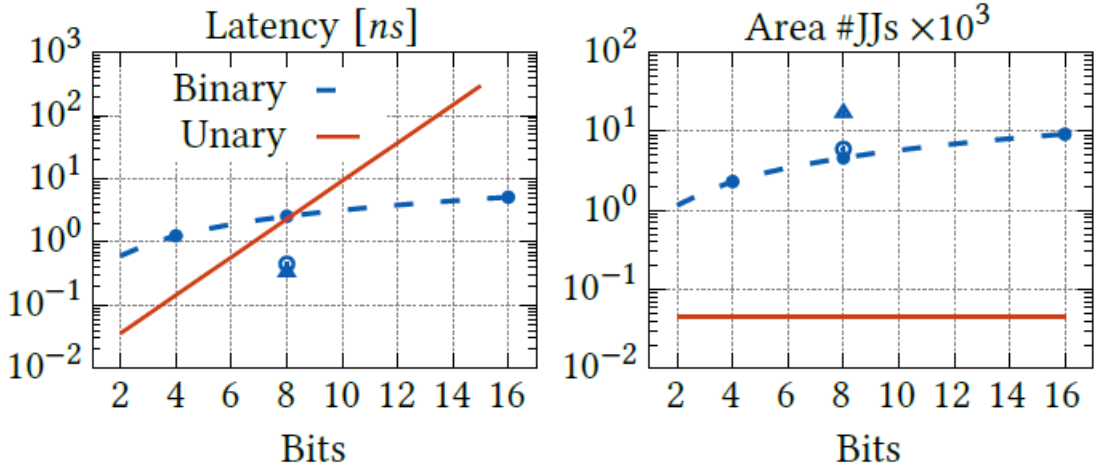
Data representation

"0" and "1" are not the only way

- Race logic (RL) represents data in time
- Time slots within a clock period can be used to represent information and perform computations
  - Unary SFQ is a combination of pulse-stream arithmetic and race logic
- Benefits can include greatly reduced circuit area







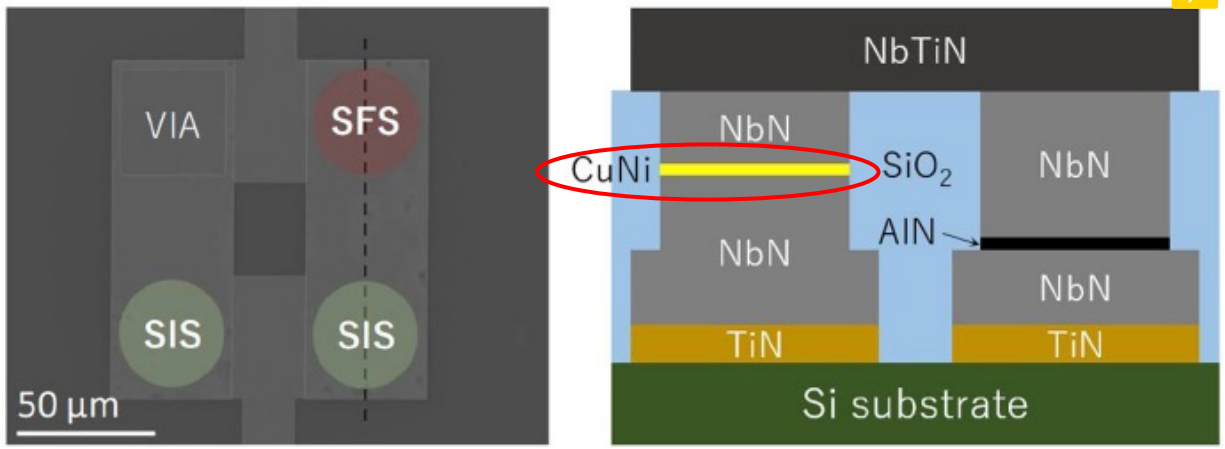
Multiplier circuit Latency and area comparison [1] Fig. 4

[1] Gonzalez-Guerrero +, 2022, doi: 10.1145/3503222.3507765

Pi Junctions

- Advantages
  - ≈ 10× (?) reduction in supply current
  - Better margins
- Disadvantages
  - Area overhead factor ≈ ×1.5 (?)
  - Separate junction layer (adds cost)
  - Barrier material is different
  - No polarity: current goes either way!
- SCE roadmap
  - 2020 onwards
  - Ni only (change?)
  - Design tool support?
- Superconducting diode in series?

▸ Worth further development

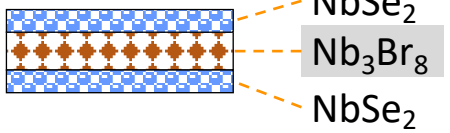


[1] Fig. 1. T_dep: 650 °C for TiN, < 100 °C for NbN, NbTiN

▸ pi-JJ (NbN/CuNi/NbN): Jc = 629 MA/m^2 (= µA/µm^2)

[1] T. Yamashita +, "π phase shifter based on NbN-based ferromagnetic Josephson junction on a silicon substrate," 2020, doi: 10.1038/s41598-020-70766-9.

Josephson diode: 2D quantum layers in the junction barrier



(hosts a net electric dipole)

[2] H. Wu et al., "The field-free Josephson diode in a van der Waals heterostructure," Nature, April 2022, doi: 10.1038/s41586-022-04504-8.

[3] https://www.tudelft.nl/en/2022/tnw/discovery-of-the-one-way-superconductor-thought-to-be-impossible

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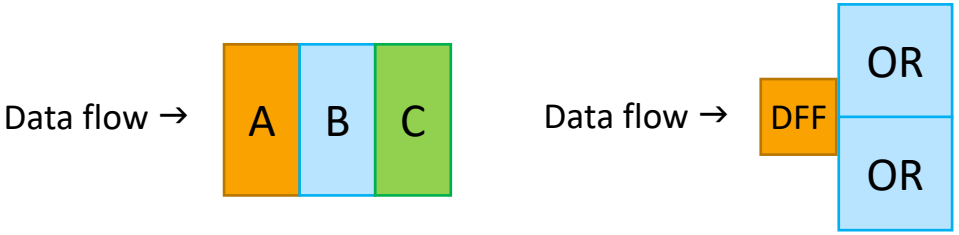
Macro blocks or cell-abutment logic

- **Macro blocks** to perform complex functions
  - Smaller, better performance
  - Licensed as intellectual property (IP) blocks
  - We need more of these!

- **Cell abutment logic**
  - Cells connect directly, like LEGO blocks
  - Blocks can contain JTLs or PTLs
  - Problem: EDA tools do not currently support abutment

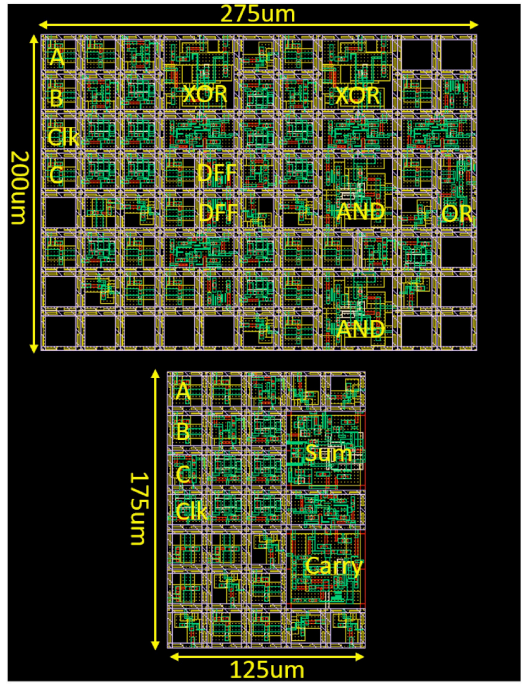


Volk +, 2022, arXiv:2206.07817

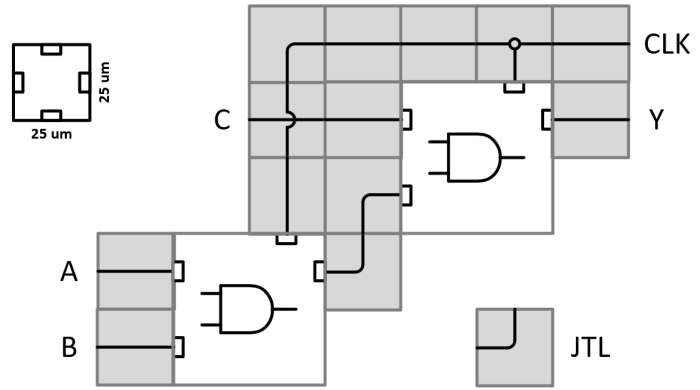
▸ ASC 2022 Oct 24 14:15, **1EPo2E-05** [E-38], Volk

2.5x area reduction: 8-bit multipliers using standard RSFQ gates and single-stage complex RSFQ gates

Cong +, 2021, doi: 10.1109/TASC.2021.3091963



Cell abutment strategy



▸ ASC 2022 Oct 26 14:30, **3EPo2B-05** [E-10], Cong

Neuromorphic Circuits using Superconductor Electronics

A more natural fit?

- Characteristics
  - Natural spiking behavior of Josephson junctions
  - Pulses travel on striplines without the RC time constants that typically hinder spike-based computing
  - Possibly tolerant to variations in component parameter values
- Needed:
  - Design methodology
  - Demonstrations at larger scale

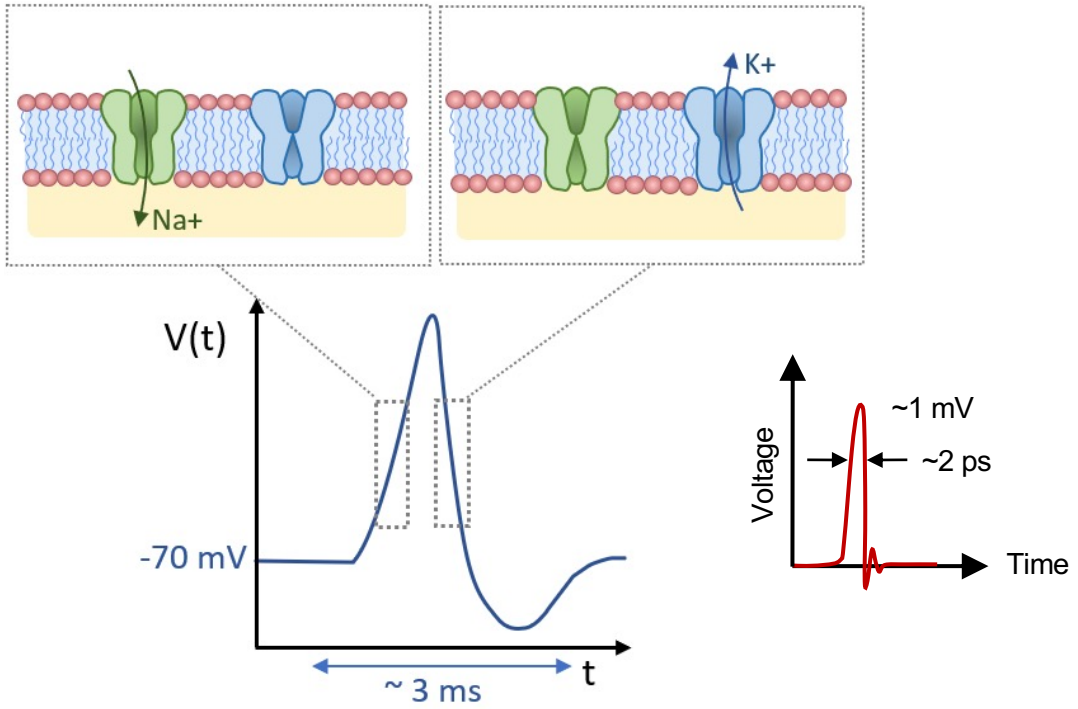


Fig. 3a. Spiking in biological neurons [1]

- ASC 2022 Oct 26 17:00, **3EOr2C-02**, Primavera "Superconducting optoelectronic single-photon synapses"

[1] Schneider +, "**Supermind**: a survey of the potential of superconducting electronics for neuromorphic computing," 2022, doi: 10.1088/1361-6668/ac4cd2

Quantum phase-slip junctions (QPSJs)

Voltage controlled devices might interface better with semiconductor electronics

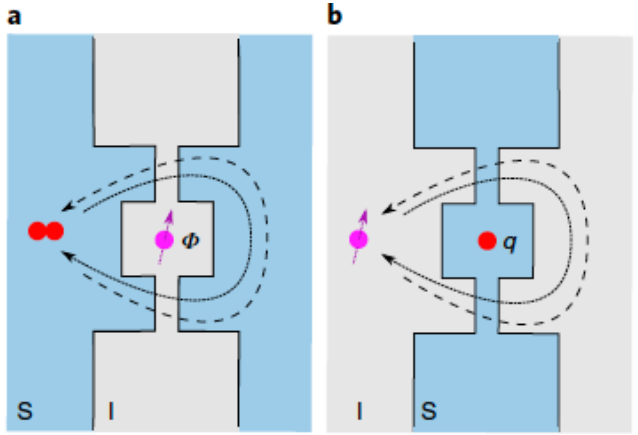
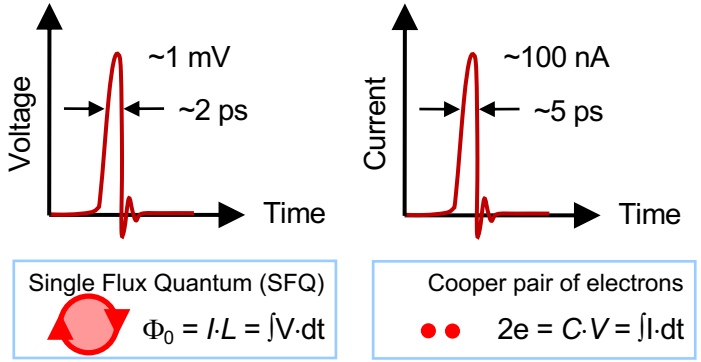


Fig. 1. SQUIDs using (a) JJs, (b) QPSJs [1]



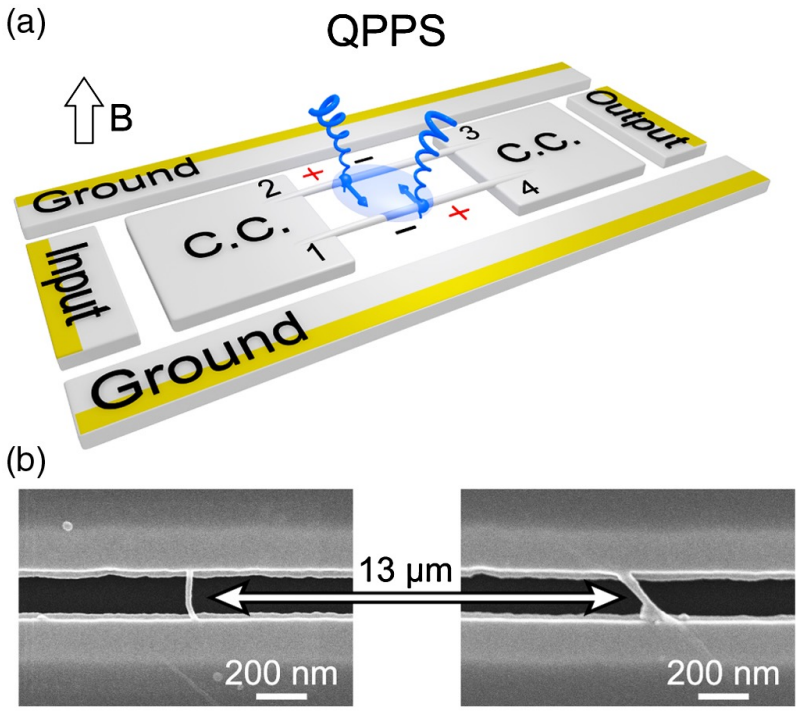


Fig. 2. MoGe nanowire QPSJs [2]

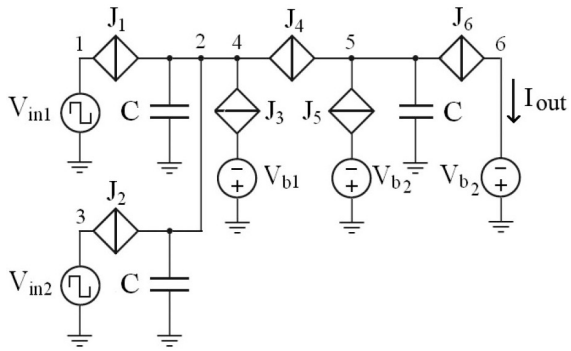


Fig. 3. Memoryless OR gate [3]

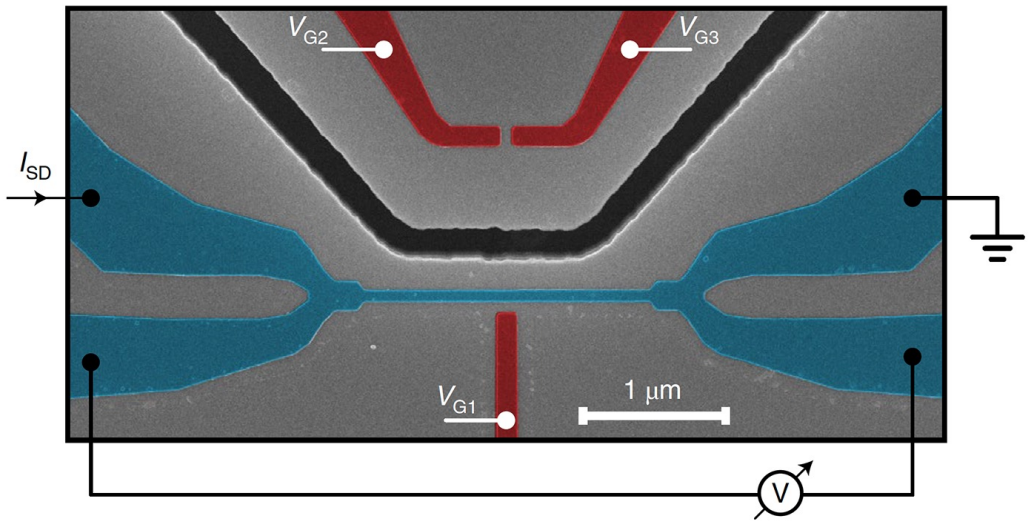
- Demonstration needed!

[1] de Graaf +, 2018, doi: 10.1038/s41567-018-0097-9
[2] Belkin +, 2015, doi: 10.1103/PhysRevX.5.021023
[3] Malekpoor +, 2021, doi: 10.1109/TASC.2021.3121344

Multi-terminal (3+) switching devices

Gated superconducting nanowire device using... phonons!

- Electric field effect had been postulated
- Phonons now seem to be the cause
- What is the best way to generate and control phonons?



M. F. Ritter *et al.*, "Out-of-equilibrium phonons in gated superconducting switches," *Nat. Electron.*, vol. 5, Feb. 2022, doi: 10.1038/s41928-022-00721-1.

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5. Memory

Status

- Memory problems
  - Small memory capacity
  - Low area density
  - Addressing can add significant overhead
  - No commercial sources

Table CEQIP-6 Superconductor Memory Status (**demonstrated**)

Name	*RAM*	*Cell Size [μm^2]*	*Latency [ns]*		*Energy [fJ]*		*Static Power*	*Bits*
			Read	*Write*	*Read*	*Write*		
SR: shift register, ac-biased		300 (15×20)						202 280
SR: shift register			0.02	0.02	0.1	0.1	0.2 mW	1024 *
VTM: vortex transition memory	✓	99 (9×11)	0.10	0.10	100	100		72
JJ-RAM: Josephson junction RAM	✓	484 (22×22)					4.5 mW	4096
RQL-RAM : reciprocal quantum logic	✓	1452 (33×44)						1024
PRAM: PTL-RAM	✓	1452 (33×44)						512
SHE-MTJ: Spin Hall effect MTJ	✓	2470 (38×65)	0.10	2	1000	8000		16
SNM: superconducting nanowire mem.	✓	26.5 (5×5.3)	0.10	3	10	10		8
Hybrid: JJ-CMOS	✓		2 ~ 4	2 ~ 4	100	100		65 536

* Incorrectly given as 64 in the 2022 report

- A critical need!

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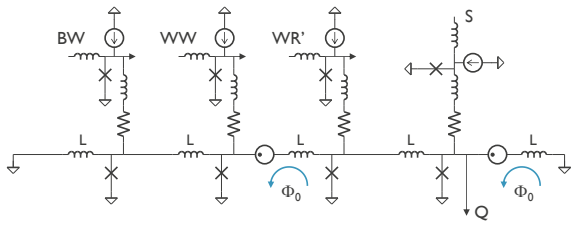
Memory

Approaches for improvement (1):

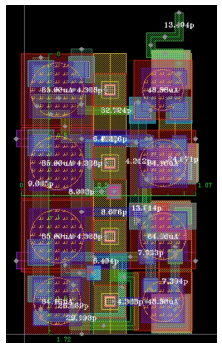
- Magnetic memory devices
  - Challenging to fabricate
  - Memory element is only a small part of the problem!
  - Composite junctions seem promising

- JJ SRAM using pulse conserving logic (PCL)
  - Density 4 MB/cm^2
  - Throughput 30 Gb/s

Unit Cell Schematic



Unit cell 1.75μm x 1.1 μm



- ASC 2022 Oct 24 14:15, **1EPo2E-07** [E39], Q. Herr

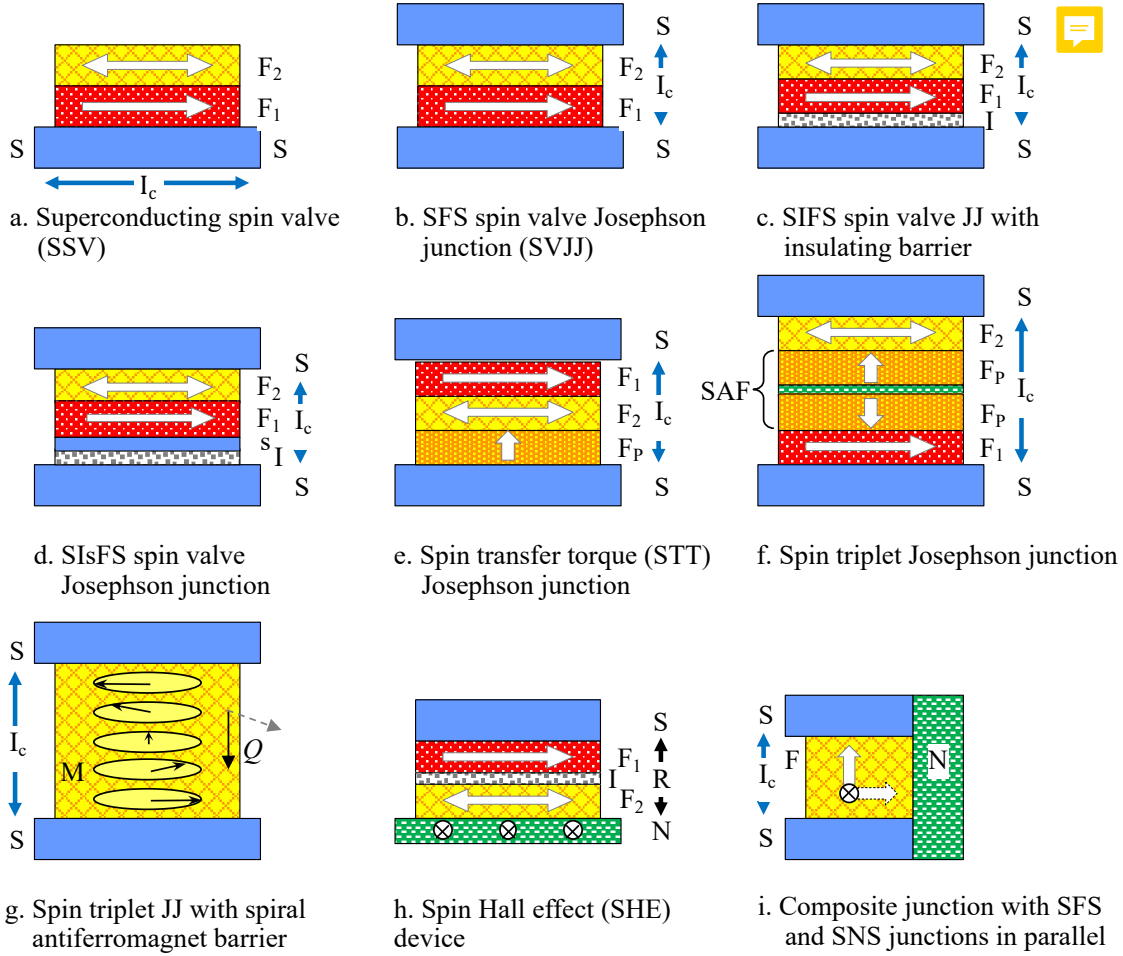
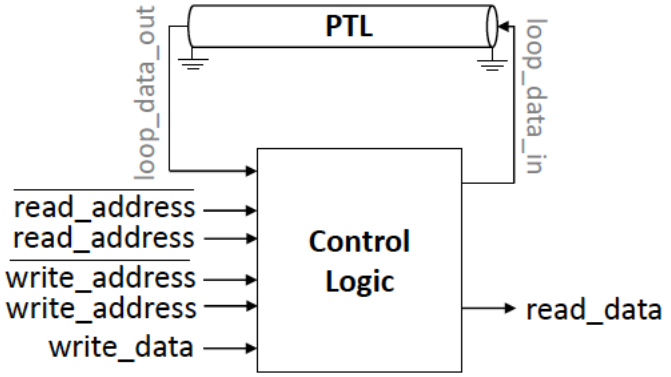


Figure CEQIP-3 Magnetic Memory Device Structures

Memory

Approaches for improvement (2):

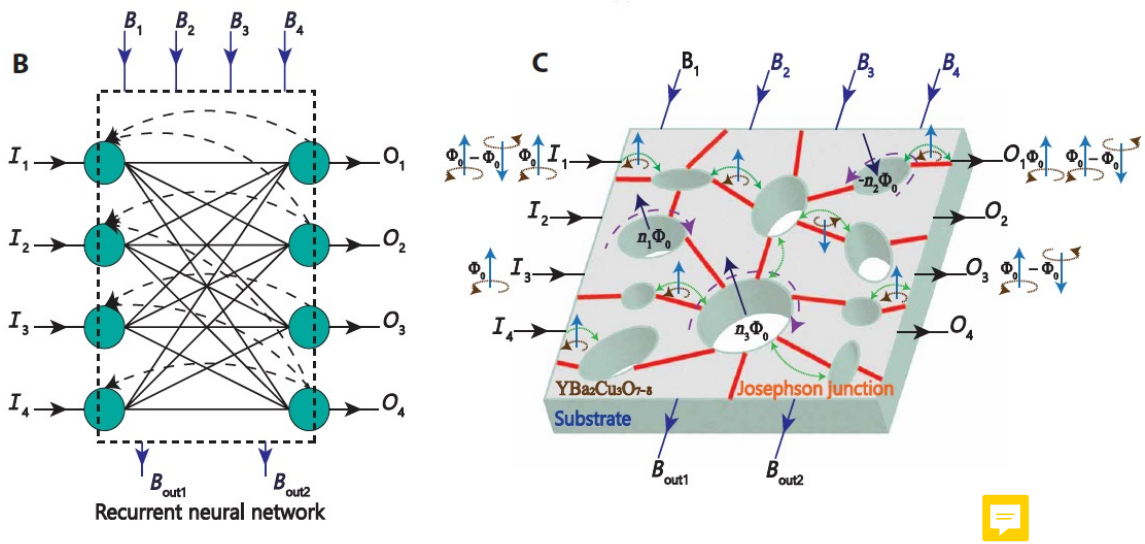
- Pulsar: A superconducting delay-line memory
  - Pulse velocity slows down in high-inductance PTLs, allowing higher memory density
  - NbN or NbTiN are candidate PTL materials
  - Control using temporal logic seems simpler than addressing logic for array-based RAM



PTL-based superconducting delay line memory system
Tzimpragos +, 2022, arXiv:2205.08016

- Loop memory
  - Superconducting disordered loop neural networks
  - He-ion beam defined JJs between holes in YBCO film
  - Memory states are affected by input signals or applied currents

▸ ASC 2022 Oct 25 16:15, **2EOr2B-08**, Goteti



Goteti +, 2022, doi: 10.1126/sciadv.abn4485

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6. Fabrication for scale

Approaches for improvement:

1. Josephson junctions with reduced variation
2. Phase-shift devices *
3. NbN or NbTiN
4. Processing temperature compatible with CMOS BEOL (400 °C)
5. Multi-terminal (3+) switching devices *

* Covered earlier

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Roadmap: Fabrication for Superconductor Electronics (SCE)

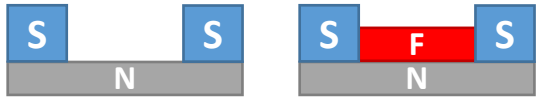
Year	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Digital SCE Fabrication															
"Node Range" label (nm)	**"250"**	**"250"**	**"250"**	**"150"**	**"150"**	**"150"**	**"150"**	**"90"**	**"90"**	**"90"**	**"90"**	**"65"**	**"65"**	**"65"**	**"65"**
Substrate material, maximum size (mm)	Si, 200	Si, 200	Si, 200	Si, 200	Si, 200	Si, 200	Si, 200	Si, 300	Si, 300	Si, 300	Si, 300	Si, 300	Si, 300	Si, 300	Si, 300
Wiring															
Superconductor	Nb	Nb	Nb	Nb	Nb	Nb	Nb	Nb	Nb	Nb	Nb	Nb	Nb	Nb	Nb
Superconductor layers	**8**	**8**	**8**	**10**	**10**	**10**	**10**	**12**	**12**	**12**	**12**	**14**	**14**	**14**	**14**
Linewidth, minimum (nm)	**250**	**250**	**250**	**150**	**150**	**150**	**150**	**90**	**90**	**90**	**90**	**65**	**65**	**65**	**65**
Ic, minimum (μA)	**200**	**200, 1200**	**200, 1200**	**100, 580**	**100, 580**	**100, 580**	**100, 580**	**50, 290**	**50, 290**	**50, 290**	**50, 290**	**20, 110**	**20, 110**	**20, 110**	**20, 110**
Junctions, Switching															
Junction materials	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx
Junction layers	**1**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Junction critical current densities, Jc (μA/μm^2)	**100**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**
Minimum junction diameter (nm)	**500**	**500**	**500**	**350**	**350**	**350**	**350**	**250**	**250**	**250**	**250**	**150**	**150**	**150**	**150**
Minimum junction critical current, Ic (μA)	**20**	**20, 118**	**20, 118**	**10, 58**	**10, 58**	**10, 58**	**10, 58**	**5, 29**	**5, 29**	**5, 29**	**5, 29**	**2, 11**	**2, 11**	**2, 11**	**2, 11**
Killer defect density per layer (1/cm^2)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**
Jc wafer-to-wafer variation	**10%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
Maximum relative spread (σ/Ic) at minimum Ic	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
Junctions, Magnetic (Pi)															
Junction materials		Ni	Ni	Ni	Ni	Ni	Ni	Ni	Ni	Ni	Ni	Ni	Ni	Ni	Ni
Junction layers	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Junction critical current densities (μA/μm^2)		**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**
Junction diameter, minimum (nm)	**500**	**500**	**500**	**350**	**350**	**350**	**350**	**250**	**250**	**250**	**250**	**250**	**250**	**250**	**250**
Resistors															
Resistor material	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx
Resistor layers	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Resistor sheet resistance (Ω/□)	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**
HKI (high kinetic inductance) Layers															
HKI material	MoNx	**NbNx**	NbNx	NbNx	NbNx	NbNx	NbNx	NbNx	NbNx	NbNx	NbNx	NbNx	NbNx	NbNx	NbNx
HKI layers	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2021 Table CEQIP-16 → 2022 Table CEQIP-17

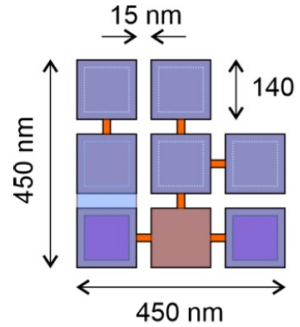
Junction scaling

Alternatives to the Nb/Al-AlO$_x$/Nb junction

- Semiconductor barriers
  - a-Si, a-SiNb$_x$ [1]
- Nanobridges
  - Nanowire superconductor
  - SN-N-NS and SN-NF-SN junctions [2]-[4]



- Question:
  - Can the devices be made with sufficiently small parameter variations (I_c, L)?



[2] Notional D flip-flop layout using magnetic junctions instead of inductors.

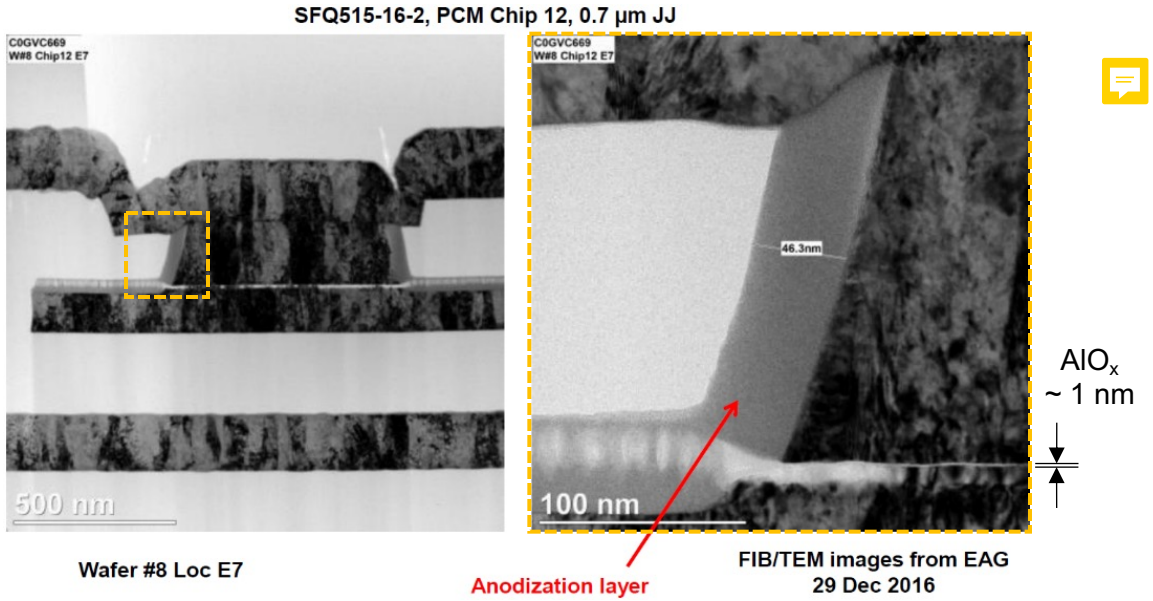
▸~ NAND2 area in 2012

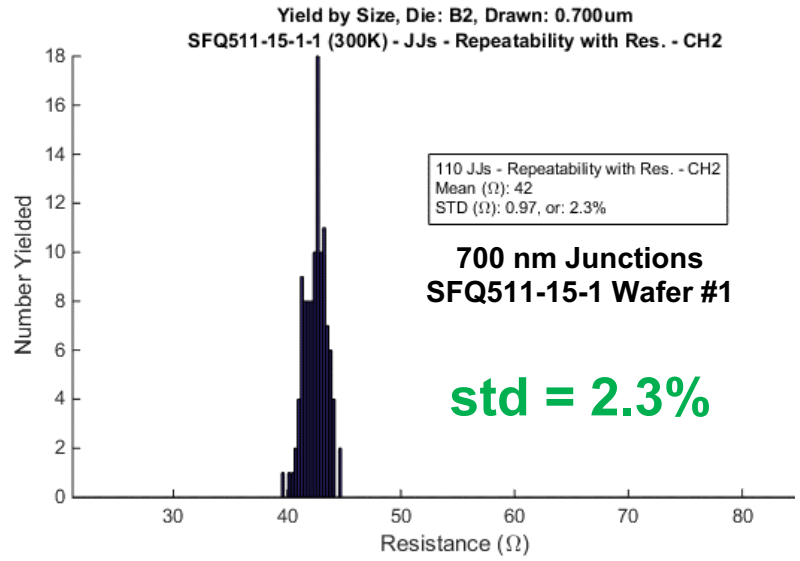
[1] D. Olaya, "Nb/a-Si/Nb Josephson junctions for superconducting analog and digital electronics," ASC 2020, Wk1EOr3B-02.
[2] I. I. Soloviev, "Superconducting digital circuits scaling pathway," ASC 2020, Wk2EOr1B-07.
[3] I. I. Soloviev +, "Miniaturization of Josephson junctions for digital superconducting circuits," 2021, DOI: 10.1103/PhysRevApplied.16.044060.
[4] S. V. Bakurskiy et al., "Compact Josephson ϕ-junctions," 2018, DOI: 10.1007/978-3-319-90481-8_3.

Junction scaling

Nb/Al-AlOx/Nb Josephson junctions are almost good enough

- Nb
  - Columnar grain growth produces roughness, grain boundaries and cracking at via edges [1]
- AlOx barriers formed by oxidation of Al:
  - Properties depend on oxidation conditions [2]
  - Variation increases for diameters smaller than ~ 500 nm, and critical current density $Jc > 100$ MA/m^2 (thickness < 1 nm)
  - Temperature limits < 200 °C make gap fill difficult
- Anodization:
  - Stress on junction increases as junction radius decreases
  - Not scalable to 300 mm?
- Temperature: < 200 °C, CMOS BEOL: 400 °C

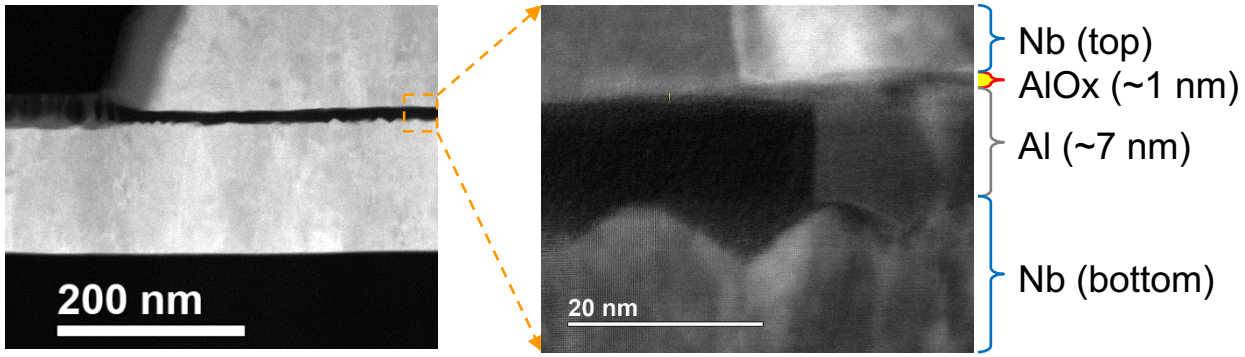




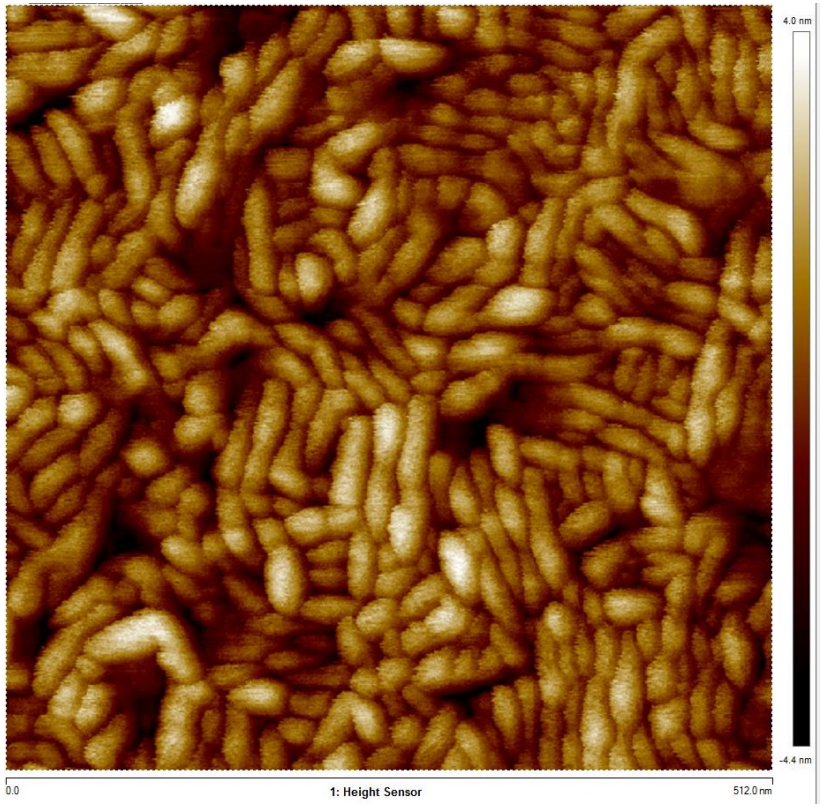
[1] N. Pokhrel, et al., "Modeling the effect of fabrication process on grain boundary formation in Nb/Al-AlOx/Nb Josephson junction circuit," *IEEE Trans. Appl. Supercond.*, Aug. 2021, doi: 10.1109/TASC.2021.3066533.

Surface roughness within a Josephson junction

- Roughness of the surfaces within a Josephson junction contributes to critical current variations
  - STEM pictures of cross sections previously provided by MITLL only gave a qualitative measure of the Nb and Nb+Al surface roughness below the ~ 1 nm thin AlOx layer in the junction.
  - TCAD process models need better information about the surface roughness.
- MITLL recently completed atomic force microscope (AFM) scans of surfaces at various stages of junction formation
  - Scans after: SiO2 underlayer polishing, Nb deposition, Al deposition
  - Fourier analysis on the scan data should allow better understanding and modeling of the surface roughness.



Josephson junction cross sections (side view)



AFM surface scan (512 nm x 512 nm) of a 150 nm thick niobium layer, 15 mm from the edge of a 200 mm diameter wafer

Image statistics:

0.96 nm	Ra (arithmetic roughness average)
1.20 nm	Rq (rms surface roughness)
9.16 nm	Z range

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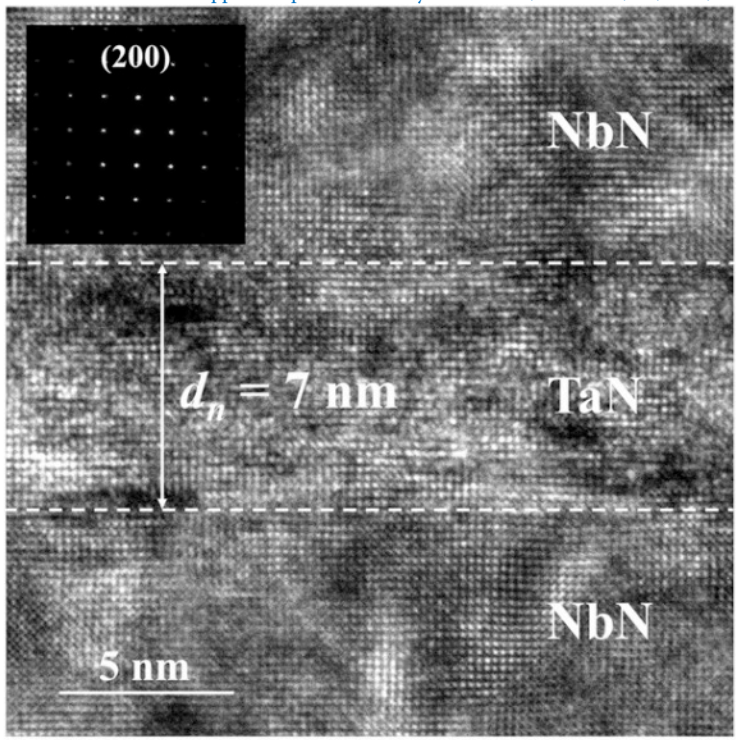
NbN or NbTiN superconductor

A step up in critical temperature

- Nb
  - Critical temperature T_C = 9.1 K
  - Processing temperature: < 200 °C; CMOS BEOL: 400 °C
  - Columnar grain growth produces roughness, grain boundaries and cracking at via edges
- NbN or NbTiN
  - Critical temperature $T_C \approx 9–16$ K (10–100 nm thick)
  - Epitaxial growth on MgO or Si\TiN substrates by reactive sputter deposition from room temperature to 400 °C
  - CVD or ALD deposition is possible
  - Smoother surface than Nb, less chemically reactive, less sensitive to oxygen contamination
  - High kinetic inductance
  - Josephson junction barriers: AlN , TaN_X, NbN_X [1-3]



[2] Figure 1b. **NbN** (200 nm)/**TaN** (7 nm)/**NbN** (200 nm) epitaxial trilayer fabricated on MgO

- Jc = 1.08–1.43 GA/m^2 (= mA/μm^2)

[1] Z. Wang *et al.*, "High-quality epitaxial NbN/AlN/NbN tunnel junctions with a wide range of current density," *Appl. Phys. Lett.*, Apr. 2013, doi: 10.1063/1.4801972.

[2] K. Yan et al., "Intrinsically shunted Josephson junctions with high characteristic voltage based on epitaxial NbN/TaN/NbN trilayer," Appl. Phys. Lett., Oct. 2021, doi: 10.1063/5.0064733.

[3] L. Zhang et al., "Electrical properties of NbN/NbNx/NbN Josephson junctions," Supercond. Sci. Technol., Dec. 2021, doi: 10.1088/1361-6668/ac2eaf.

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NbN or NbTiN fabrication processes

- **NbN**/Nb bilayers
  - 2-step patterning process
  - Current flows through lowest inductance path (Nb, if present)

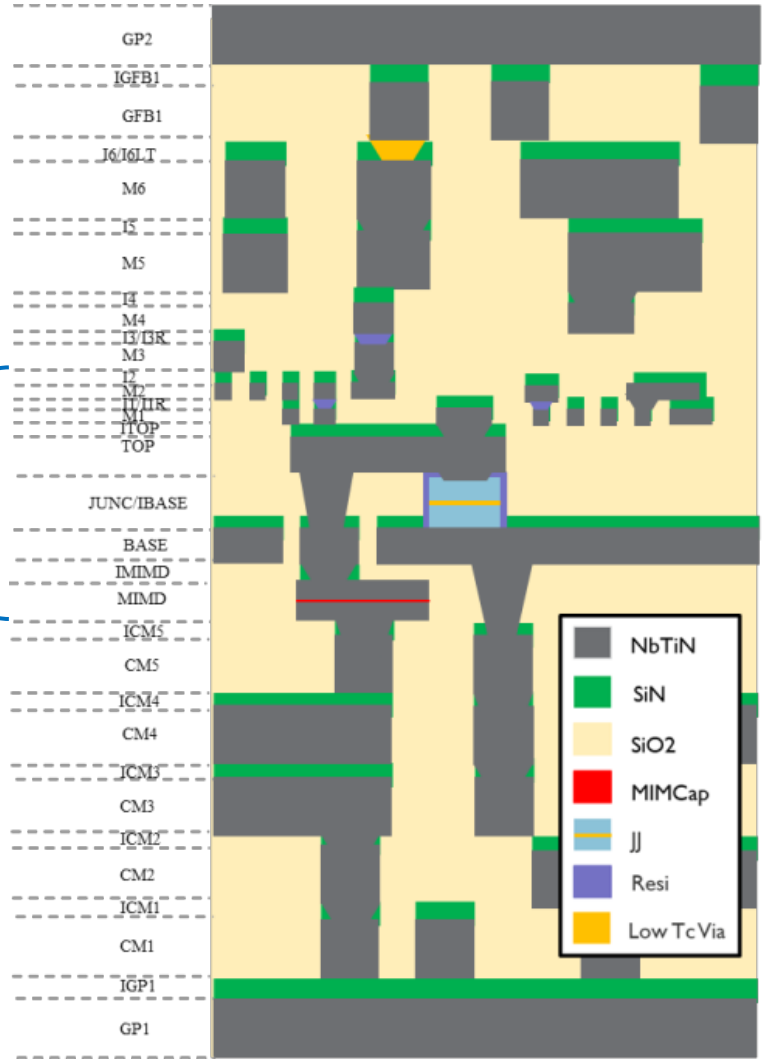
Tolpygo +, 2022, arXiv:2210.10705

- Process with planarized **NbN** layers (MITLL)
  - ASC 2022 Oct 24 16:15, **1EOr2C-01**, Tolpygo

- **NbTiN** digital stack process (IMEC)
  - Tc = 11 to 13 K
  - NbTiN films can scale to 7.6 nm thickness
  - 50 nm line widths demonstrated with Tc = 12.5 K and Ic = 200 µA

  - ASC 2022 Oct 24 17:15, **1EOr2C-04**, A. Herr
    "Scaling superconducting digital technology to 400M JJ/cm²"

In development



NbTiN digital stack process vision (IMEC)

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Conclusions

Keys needs in the technology roadmap for superconductor electronics

1. **Power distribution**
   - Biasing junctions using externally-supplied direct current (DC) does not scale!
2. **Sensitivity to external magnetic fields, currents, and trapped flux**
   - Greatest improvements involve disruptive changes
3. **Area reduction**
   - Many approaches, finding the best combination is the challenge
4. **Logic**
   - Clocking every logic gate does not scale! Still searching for a winning combination.
5. **Memory**
   - Greatest need for innovation!
6. **Fabrication for scale**
   - Changes are costly and require consideration.

▸ Some solutions on the horizon, but plenty of room for innovation!

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Catching the wave

Be ready!

Image by Kanenori from Pixabay

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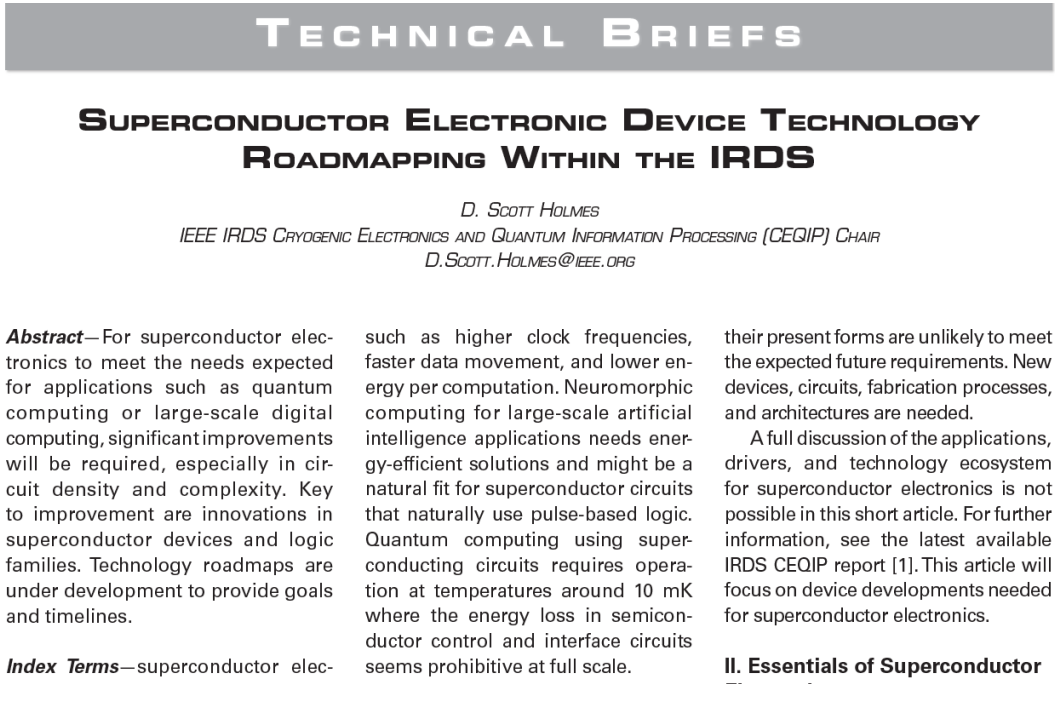
References

1. "IRDS 2022: Cryogenic Electronics and Quantum Information Processing," IEEE International Roadmap for Devices and Systems, 2022. https://irds.ieee.org/editions/2022
2. D. S. Holmes, "Superconductor electronic device technology roadmapping within the IRDS," *IEEE Electron Devices Society Newsletter*, pp. 6–11, Apr. 2022. https://eds.ieee.org/images/files/newsletters/Newsletter_Apr22.pdf



TECHNICAL BRIEFS

SUPERCONDUCTOR ELECTRONIC DEVICE TECHNOLOGY ROADMAPPING WITHIN THE IRDS

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IEEE IRDS CRYOGENIC ELECTRONICS AND QUANTUM INFORMATION PROCESSING (CEQIP) CHAIR
D.SCOTT.HOLMES@IEEE.ORG

Abstract—For superconductor electronics to meet the needs expected for applications such as quantum computing or large-scale digital computing, significant improvements will be required, especially in circuit density and complexity. Key to improvement are innovations in superconductor devices and logic families. Technology roadmaps are under development to provide goals and timelines.

Index Terms—superconductor elec-

such as higher clock frequencies, faster data movement, and lower energy per computation. Neuromorphic computing for large-scale artificial intelligence applications needs energy-efficient solutions and might be a natural fit for superconductor circuits that naturally use pulse-based logic. Quantum computing using superconducting circuits requires operation at temperatures around 10 mK where the energy loss in semiconductor control and interface circuits seems prohibitive at full scale.

their present forms are unlikely to meet the expected future requirements. New devices, circuits, fabrication processes, and architectures are needed.

A full discussion of the applications, drivers, and technology ecosystem for superconductor electronics is not possible in this short article. For further information, see the latest available IRDS CEQIP report [1]. This article will focus on device developments needed for superconductor electronics.

II. Essentials of Superconductor