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1EOr2B-03: An adiabatic quantum-flux-parametron block permutation unit for a superconductor SHA-3 cryptoprocessor

Christopher L. Ayala[1], Tomoyuki Tanaka[2], Ro Saito[2], and Nobuyuki Yoshikawa[1]

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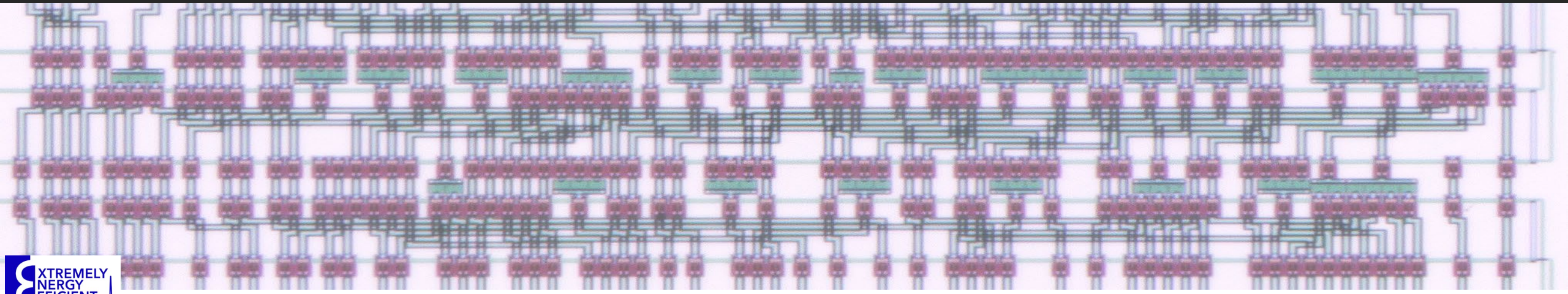
[2]*Department of Electrical Engineering and Computer Engineering, Yokohama National University, Japan*
email: ayala-christopher-pz@ynu.ac.jp



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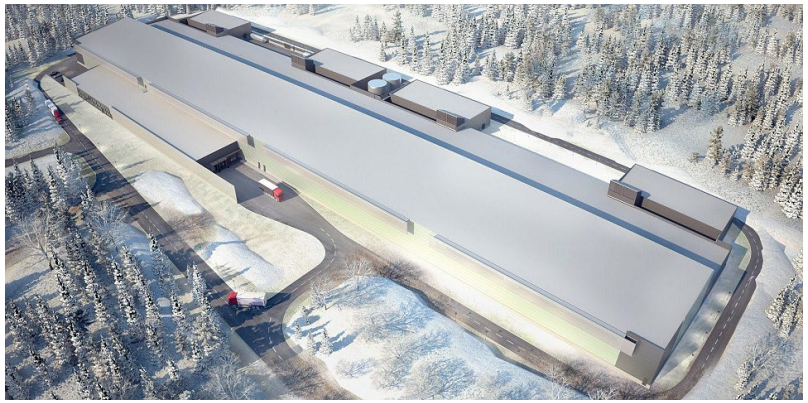
Motivation

Trend of rising electricity demand of information and communications technology (ICT).

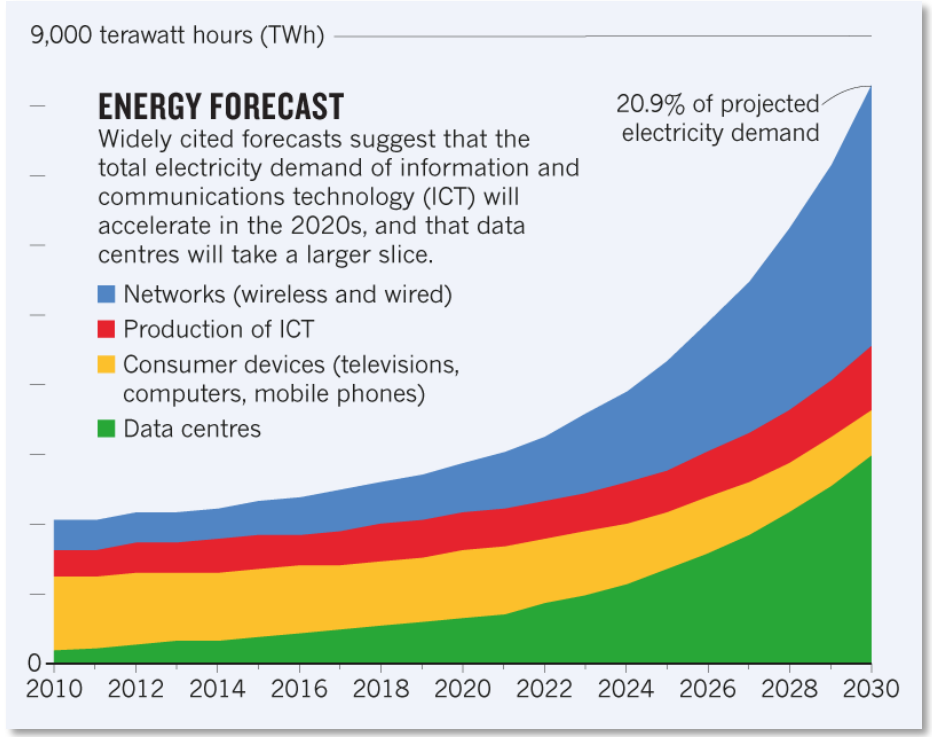
Currently 10% of the total electric power worldwide as of 2020.

Facebook Data Center, Lulea, Sweden



Performance: 27-51 PFLOP/s
Power 84 MW avg* (120 MW max)

D.S. Holmes, ISS 2013, Tokyo, Japan.
http://worldstopdatacenters.com/renewable-energy-output-rankings/



N. Jones, *Nature*, vol. 561, no. 7722, pp. 163–166, Sep. 2018.

Worst-case scenario: ICT could use as much as 50% of global electricity by 2030.

A. S. G. Andrae and T. Edler, *Challenges*, vol. 6, no. 1, pp. 117–157, Jun. 2015.

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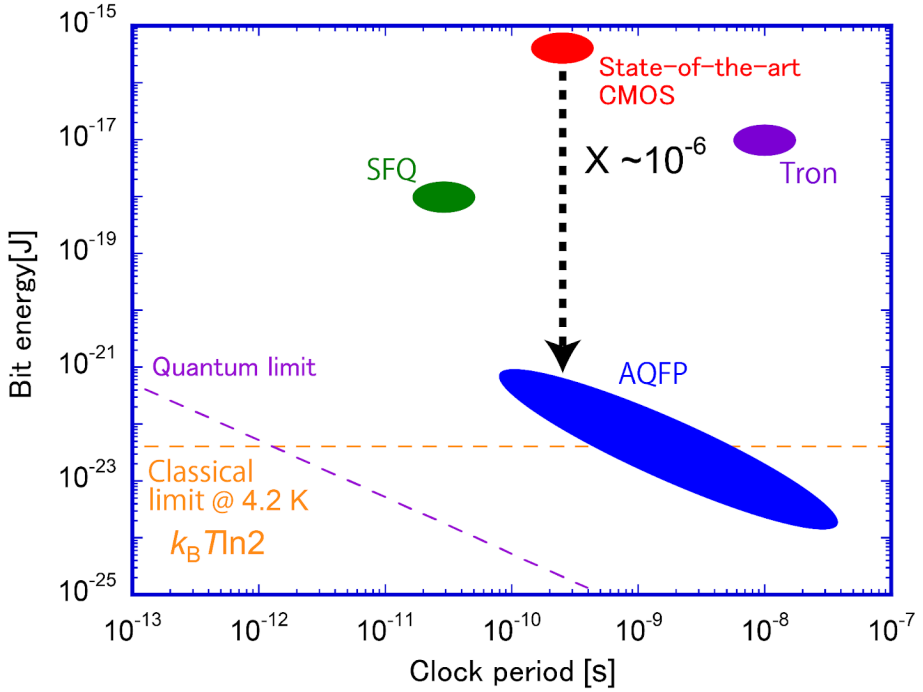
AQFP logic for computing

- **A**diabatic **q**uantum-**f**lux-**p**arametron (AQFP) logic
  - Composed of a pair of Josephson junction (JJ) superconductor devices
  - Extremely small bit energy << $I_c\Phi_0$
    - Very small switching energy due to adiabatic operation
    - 1.4 zJ per JJ at 4.2 K in experiment [1]
  - High gain
    - 10-50x gain from μA's of input current
  - High robustness
  - Clock speeds on par with state-of-the-art CMOS logic (5-10GHz)



After cooling overhead [2], **~80x more efficient** than 7nm FinFET with V_{DD} = 0.8V [3]

[1] N. Takeuchi et al., Appl. Phys. Lett., vol. 114, no. 4, p. 042602 (2019)
[2] D.S. Holmes et al., IEEE TAS, 23, no.3, (2013)
[3] A. Stillmaker et al., Integration. 58, pp. 74-81 (2017)

AQFP logic a promising candidate for energy-efficient computing.

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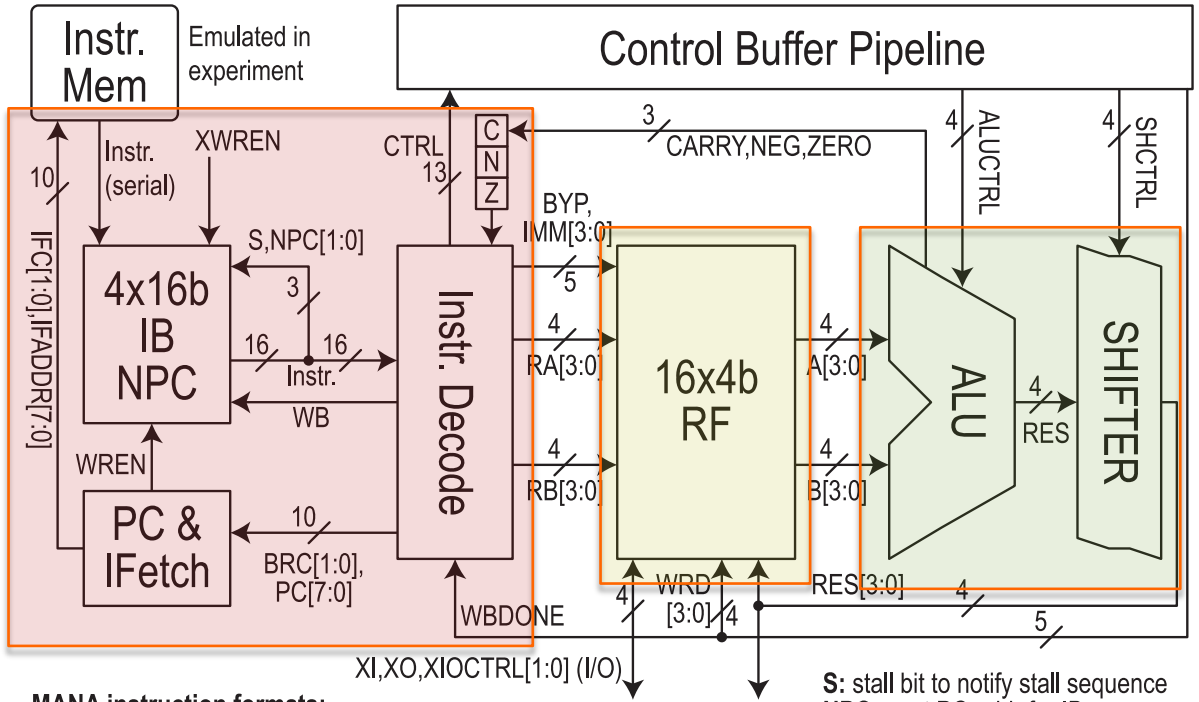
MANA microarchitecture



MANA instruction formats:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
S	NPC		OPCODE					IMM				RB				Immediate format
S	NPC		OPCODE					BRC/JMP ADDR								Branch/jump format
S	NPC		OPCODE					RA				RB				ALU format
S	NPC		OPCODE					SOP		AMT		RB				Shifter format
S	NPC		OPCODE					MEM								Memory access format

S: stall bit to notify stall sequence
NPC: next PC addr for IB
OPCODE: opcode of instr.
IMM: immediate value
BRC/JMP: branch/jump addr.
RA: reg. A addr.
RB: reg. B addr. (also destination)
SOP,AMT: shift opcode and amount
MEM: Mem. addr. for data.

MANA – Monolithic Adiabatic iNtegration Architecture

- **Goal:** Demonstrate AQFP can do both logic and memory
- RISC-like datapath + dataflow-like control
- In-order, single-issue
- 4-bit data word size
- 16-bit instr. word
- Program branching
- 21,460 JJs in 1 x 1 cm^2 chip
- 30 fJ/op at RT @ 5 GHz
- 4-phase 5 GHz clock
- Latency: 108 clock phases or 27 cycles (5.4 ns @ 5 GHz)

Instruction Buffer, Decode, and Issue (IDI)
5,596 JJs
8 cycles (32 phases)

Register File with external I/O (RFX)
8,142 JJs
8 cycles (32 phases)

ALU-Shifter (EX)
2,238 JJs
9 cycles (36 phases)

Ctrl buffer, routing, write-back (WB)
5,484 JJs
17 cycles (68 phases) overlapped
2 cycles (8 phases) write-back

C. L. Ayala et al., "MANA: A Monolithic Adiabatic iNtegration Architecture Microprocessor Using 1.4-zJ/op Unshunted Superconductor Josephson Junction Devices," IEEE JSSC, Apr. 2021.

MANA featured in media

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IEEE SPECTRUM

Superconducting Microprocessors? Turns Out They're Ultra-Efficient

The 2.5 GHz prototype uses 80 times less energy than its semiconductor counterpart, even accounting for cooling

By **Michelle Hampson**

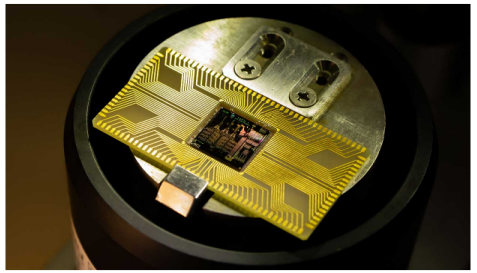


Photo: Christopher Ayala

The AQFP-based MANA microprocessor seated on a chip holder. The microprocessor die contains over 20,000 superconductor Josephson junctions. It is the first ever adiabatic superconducting microprocessor.

Computers use a staggering amount of energy today. According to one recent estimate, data centers alone consume two percent of the world's electricity, a figure that's expected to climb to eight percent by the end of the decade. To buck that trend, though, perhaps the microprocessor, at the center of the computer universe, could be streamlined in entirely new ways.

One group of researchers in Japan have taken this idea to the limit, creating a superconducting microprocessor—one with zero electrical resistance. The new device, the first of its kind, is described in a study published last month in

SUPERCONDUCTOR WEEK -6- FEBRUARY 4, 2021

YNU Pioneers Superconducting 4-bit Adiabatic Processor

Six Partners to Coordinate Decoherence Effort

Northwestern, Ames, Fermilab, Rigetti Computing, the NIST, and the Italian National Institute of Physics (INFN) are all united in this decoherence effort. Rigetti Computing will be fabricating qubits and full stack quantum computing capabilities required for the SQMS quantum computer. The NASA Ames Research Center quantum group contributing with programs investigating quantum algorithms, programming, and simulation. The INFN has research programs centered around detector development, cryogenics and environmental measurements, and the worlds largest underground facility.

"Our approach is a parallel track of improving 2D quantum processors utilizing the expertise from Rigetti in building full-stack quantum computers, and integrating transmon qubits with SRF cavities to develop a new generation of 3D quantum processors utilizing the multi-mode photon states of these high Q SRF cavities," Sauls explained. "A strength of Fermilab is the experience in large-scale integration of cryogenic and microwave technologies, and in Rigetti's experience and facilities for building superconducting transmons and 2D quantum processors."

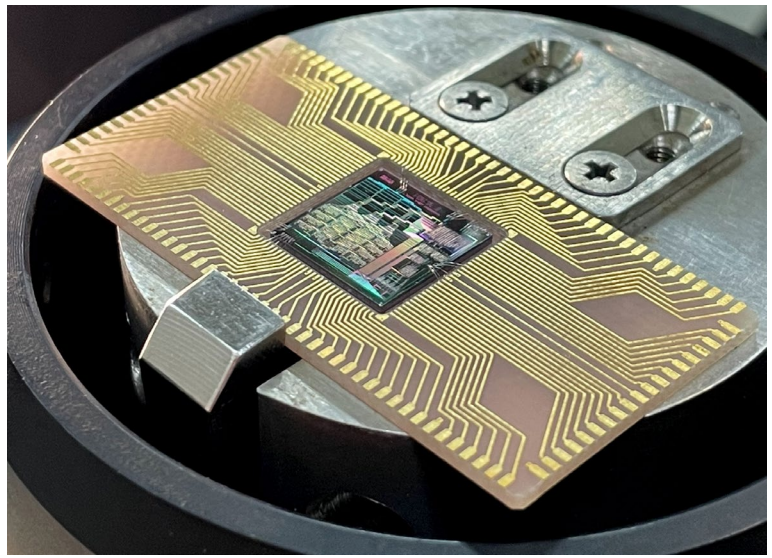
Sauls noted that Fermilab aims to deliver the next generation of quantum processors based on 2D architectures and qubits with longer coherence times in three years, and beyond state-of-the-art quantum computers based on 3D architectures in five years: "There is a great deal of basic research that will be carried out within SQMS to reach these goals, and that knowledge will also inform the direction of research and development of quantum devices and sensors. In terms of quantum sensing, short of discovering dark matter, we expect major new limits to be set for two dark matter candidates using SRF cavities as quantum sensors for detection of the dark matter candidates, the axion and dark photon." ■

Researchers from Yokohama National University (YNU) have successfully demonstrated a prototype microprocessor that uses superconducting niobium, the first time an adiabatic superconductor microprocessor has ever been demonstrated. (DOI: 10.1109/JSSC.2020.3043138). Their novel device delivers a significant increase in energy efficiency compared to the semiconductor microprocessors that are commonly used today, which suggests that they might be suitable in applications in large data processing centers.

Computation power is currently responsible for about 10% of global energy consumption. If improvements are not made on communications infrastructure or the electronics that drive communications networks, this figure could climb to 50% by 2030. "With an ever increasing demand for computational power and the energy to power it, the coming years will surely see great demand for and potential benefit from technologies improving data transmission efficiency.

Device is Built into an AQFP Structure

The Yokohama 4-bit processor, dubbed the Monolithic Adiabatic iNtegration Architecture (MANA), is based on unshunted Josephson



日経 XTECH

Hot News ＋ 連載をフォロー

超電導コンピューターが離陸へ、スパコンの電力を1/2000に

量子コンピューターの制御にも利用

野澤 哲生 日経クロステック／日経エレクトロニクス

2021.03.19

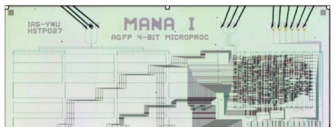
全5067文字

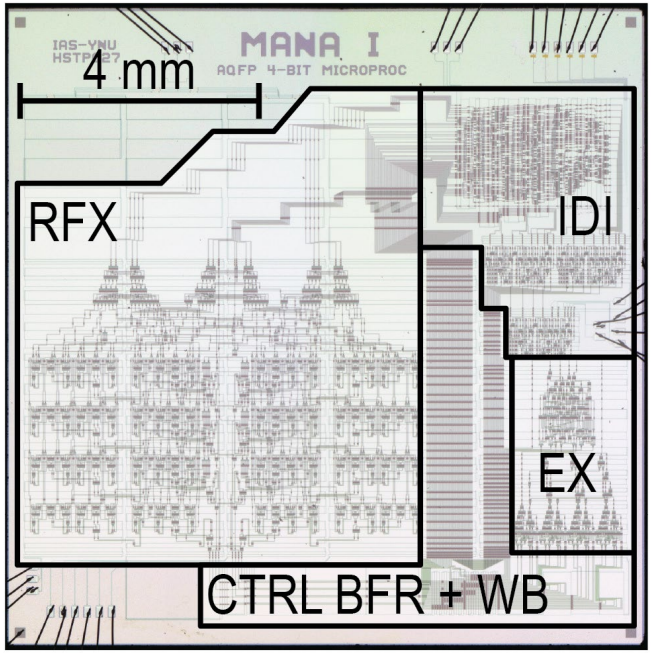
PR

脱炭素時代の到来に合わせて、コンピューターの消費電力を圧倒的に低減する技術が登場してきた。それが「超電導コンピューター」だ。横浜国立大学 工学研究院 知的構造の創生部門 教授の吉川信行氏の研究室は、4ビット動作の超電導RISC型マイクロプロセッサー「MANA 1†」を開発した（図1）。動作周波数は5G～10GHz前後で、消費電力は冷却用電力を別にした場合、一般的なSi半導体に基づくマイクロプロセッサーの約100万分の1以下と猛烈に低い。

冷却プローブ上の超電導プロセッサー（写真：横浜国立大学）
[画像のクリックで拡大表示]

†MANA＝Monolithic Adiabatic iNtegration Architecture Processor。





CRAVITY
AIST

MANA featured in media

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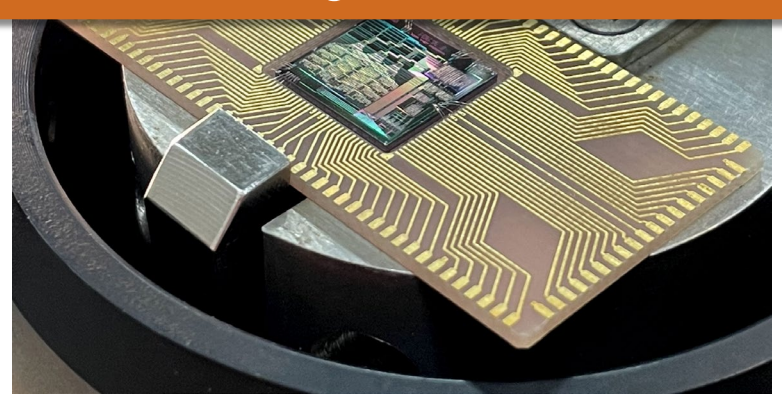
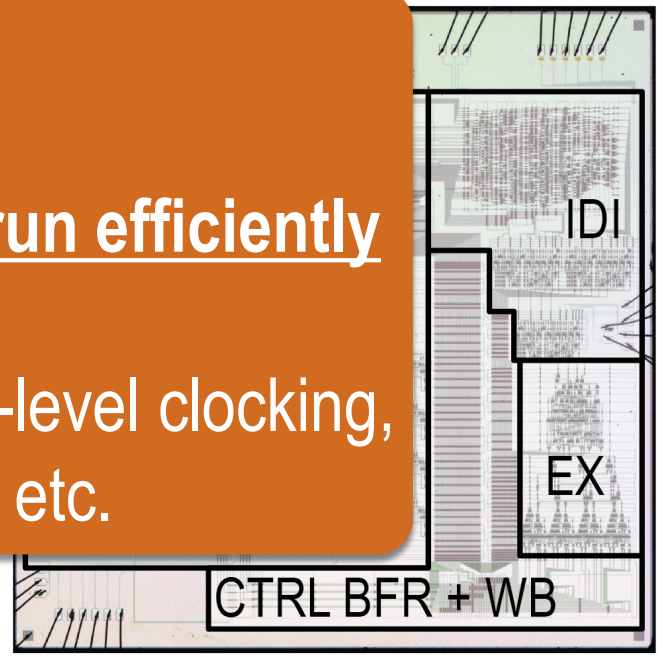


日経 XTECH

Hot News + 連載をフォロー

超電導コンピューターが離陸へ、スパコンの電力を1/2000に

- MANA: prototype, conceptual demo
- Small instruction buffer, real-world programs **would not run efficiently**
- Ongoing AQFP research on low-latency techniques, chip-level clocking, impedance matching of data interconnect, circuit density, etc.



CRAVITY
AIST

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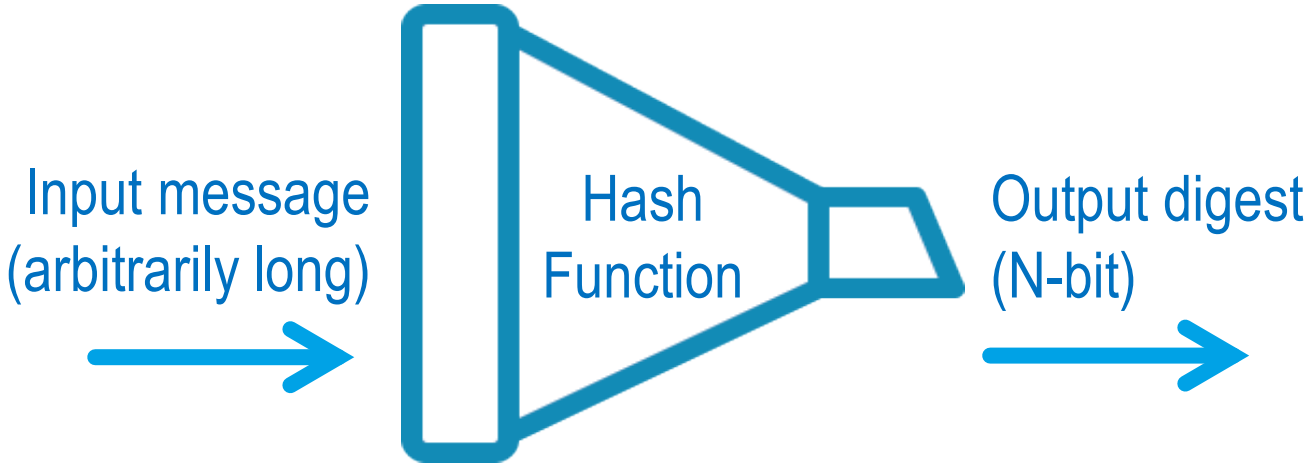
Cryptography: hashing

In what application can we leverage SCE technology today?

- How about cryptography – hashing?
  - $h : \{0, 1\}^* \longrightarrow \{0, 1\}^n$
  - Input: "message" arbitrarily long binary input
  - Output: "digest" fixed length (*n*) binary output
    - Ideally a unique signature for the input message
  - Similar inputs ⇒ dissimilar outputs
  - Ideally difficult to reverse engineer input using output



Uses:

- O(1) data structure in programs (Hash Table)
- Digital signatures
- Encryption/cybersecurity
- Cryptocurrency

Architecture implementation properties:

- Data feedback is typically well-controlled
- Control is simple, usally defined as fixed rounds/iterations (counters)
- Easy to keep pipeline filled
- Usually no need for centralized memory during hashing

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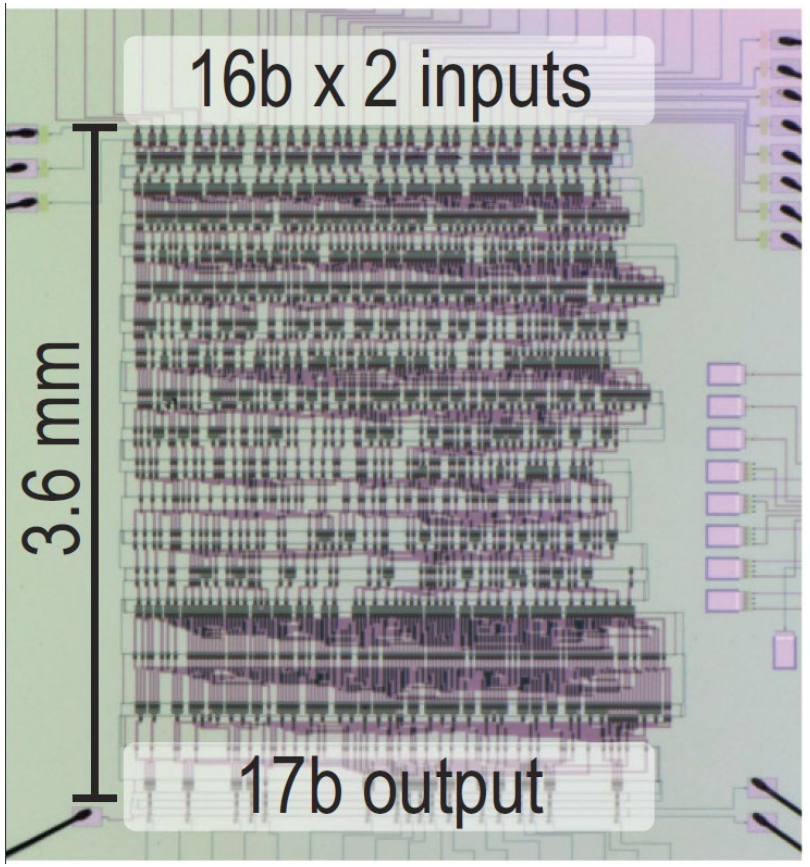
Secure Hashing Algorithms (SHA)

Algorithm	Year	Output Size	State Size	Operations	Collisions Found?
SHA-0	1993	160-bit	160-bit	AND, XOR, OR, ROT, ADD32	Yes ($\leq 2^{34}$ evaluations)
SHA-1	1995	160-bit	160-bit	AND, XOR, OR, ROT, ADD32	Yes ($< 2^{63}$ evaluations)
SHA-2 (SHA-256)	2001	256-bit	512-bit	AND, XOR, OR, ROT, SHR, ADD32	No (2^{128} evaluations)
SHA-3 (SHA3-256)	2015	256-bit	1600-bit*	ADD, XOR, ROT, NOT	No (2^{128} evaluations)

SHA3/Keccak (“Ket-chak”) algorithm won the NIST hash function competition in 2012

SHA-3 is paramterizable*, simple, and modern – good candidate for implementation.



16-bit AQFP Kogge-Stone adder component [1]

[1] T. Tanaka et al, “A 16-bit parallel prefix carry look-ahead Kogge-Stone adder implemented in adiabatic quantum-flux-parametron logic,” IEICE Transactions on Electronics, vol. E105–C, no. 6, Jun. 2022.

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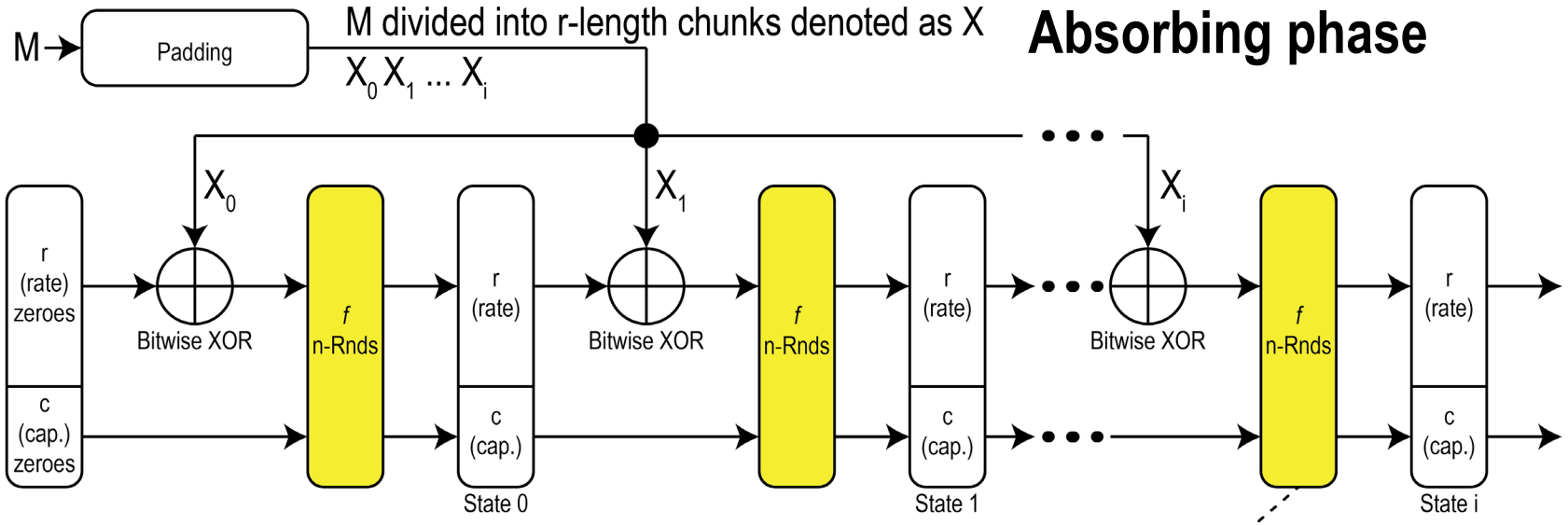
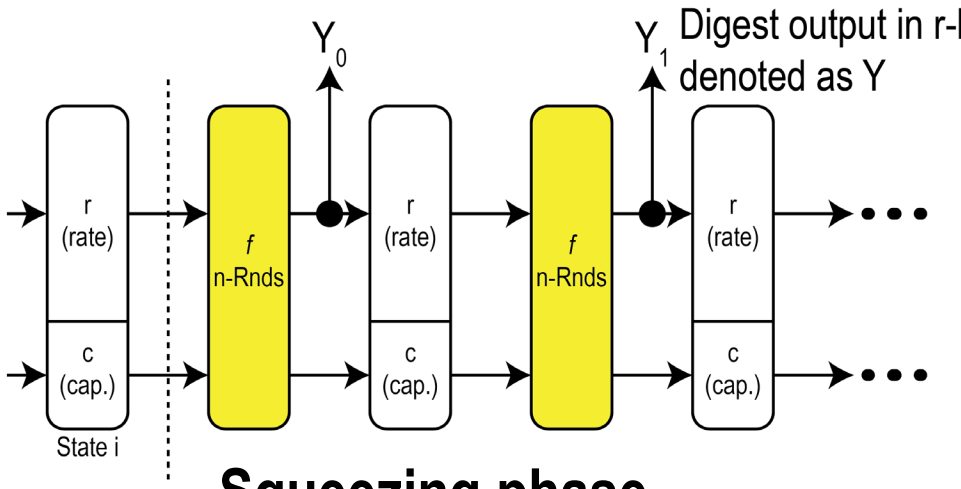
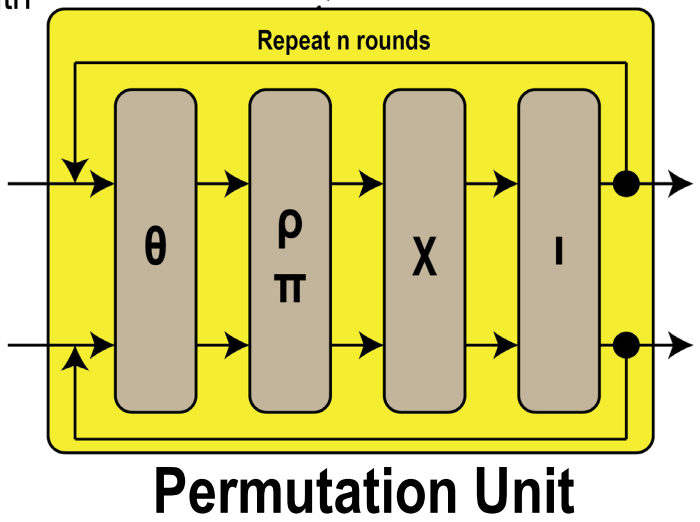
SHA3 overview

Standard: https://nvlpubs.nist.gov/nistpubs/FIPS/NIST.FIPS.202.pdf







- ”Sponge construction”
- State size (bits):
  $$b = 5 \times 5 \times 2^l$$
- l = 0, 1, 2, 3, 4, 5, **6**
- b = 25, 50, 100, 200, 400, 800, **1600**
- $b = c + r$
  c is capacity, *r* is rate
- *c* determines security level
- *r* determines block size
- Permute functions:
  θ (theta), ρ (rho), π (pi), ι (iota)
- Permutation rounds:
  $$n = 12 + 2l$$

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SHA3 overview

Pseudo code of permute functions:

```
Round[b](A,RC) {
# θ step
C[x] = A[x,0] xor A[x,1] xor A[x,2] xor A[x,3] xor A[x,4], for x in 0…4
D[x] = C[x-1] xor rot(C[x+1],1), for x in 0…4
A[x,y] = A[x,y] xor D[x], for (x,y) in (0…4,0…4)

# ρ and π steps
B[y,2*x+3*y] = rot(A[x,y], r[x,y]), for (x,y) in (0…4,0…4)

# χ step
A[x,y] = B[x,y] xor ((not B[x+1,y]) and B[x+2,y]), for (x,y) in (0…4,0…4)

# ι step
A[0,0] = A[0,0] xor RC

return A
}
```

Just AND, XOR and NOT bitwise operators and ROT (rotate) operation

- ”Sponge construction”
- State size (bits):
$$b = 5 \times 5 \times 2^l$$
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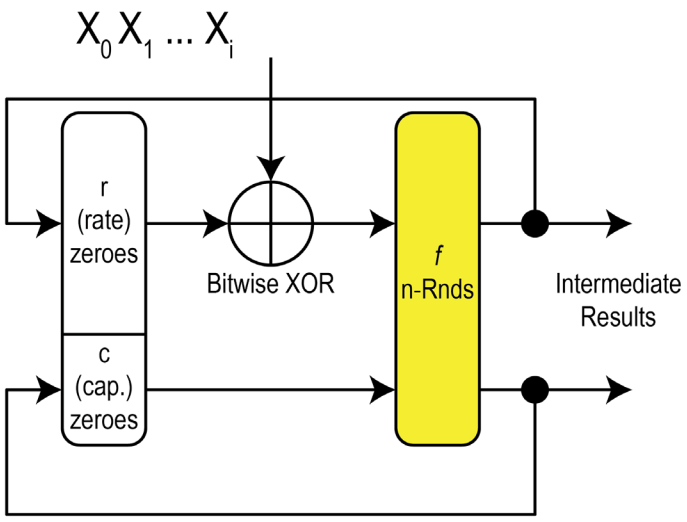
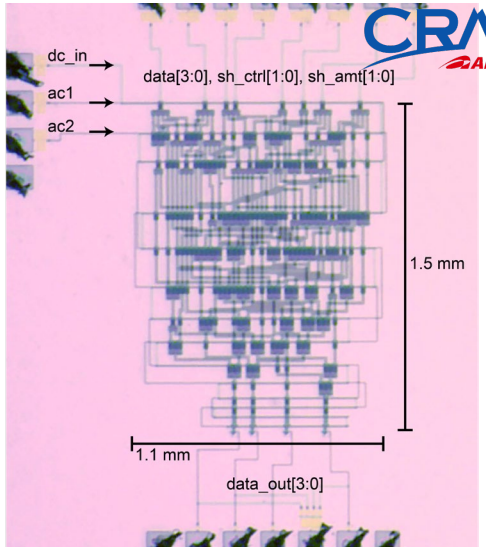
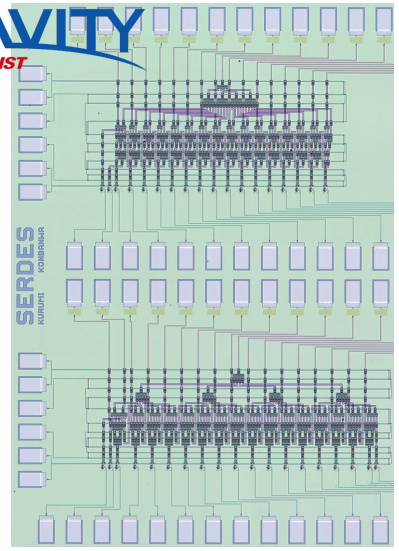
Implementation of SHA3 permutation block



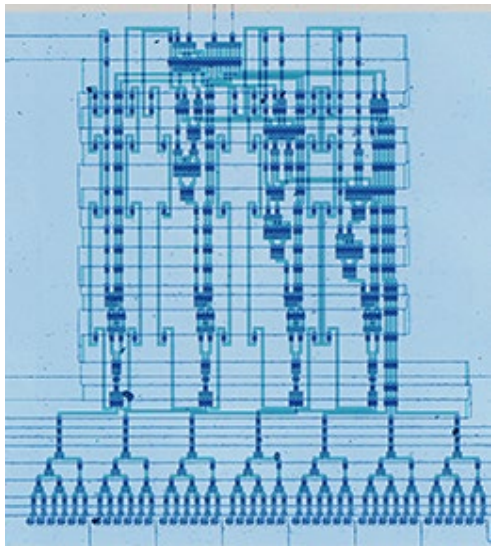
Permutation block



Data shifter [1]



SerDes [2]



Gray counter [3][4]

Power-clock impedance matching [5]

- Input pre-padded, non-standard parameters: $l = 0, b = 25, r = 16, c = b - r = 9$
- Circuit divided into 3 clocked networks supplied by a resistor-based power divider
- Key components needed:
  Data rotator – similar to shifter, SerDes for I/O and debugging, sequential finite-state machine techniques, and improved impedance design power-clock lines

[1] C. L. Ayala, ISS 2017, Tokyo, Japan. [2] C. L. Ayala, ISS 2020, Online. [3] R. Saito et al., DOI: 10.1109/tasc.2021.3061636. [4] T. Yamae et al., DOI: 10.1109/TASC.2020.3044677. [5] N. Takeuchi et al., DOI: 10.1109/TASC.2021.3058080

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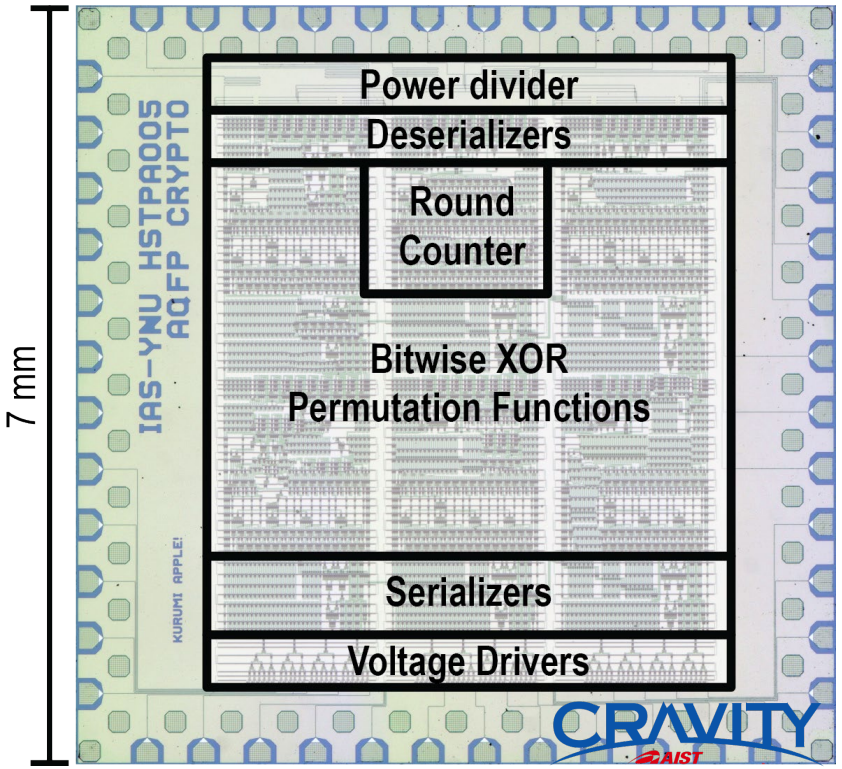
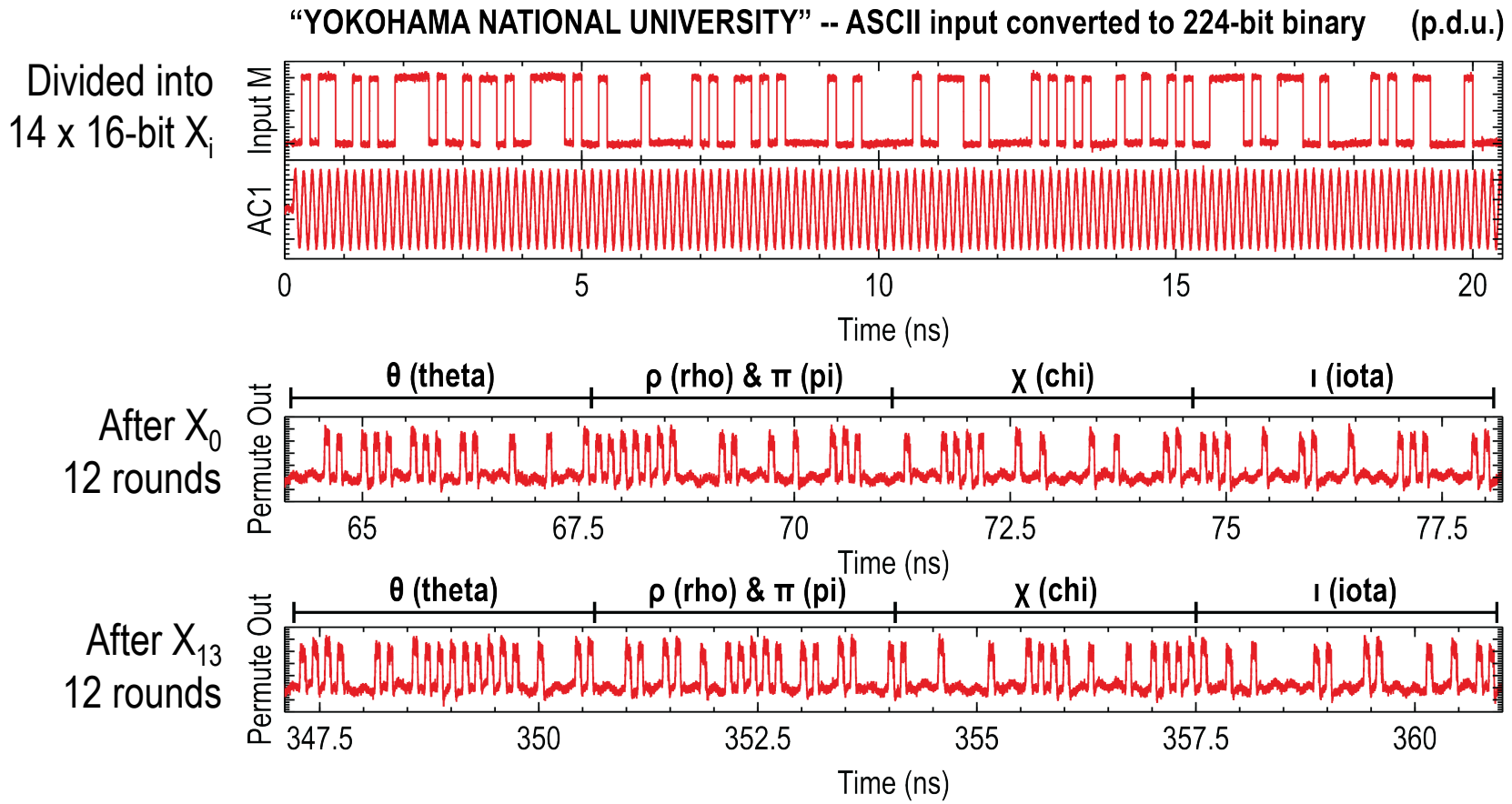
Measurement of permutation block



JJ count: 13,008 JJs
Chip: 7 mm x 7 mm, 48 pad
Active circuit area: 5.0 mm x 5.6 mm
Maximum operation: 7 GHz
AC margins: +16% / -12%



- Complex test – PyVISA used to help automate experiment
- First +10k JJ AQFP chip at GHz speeds – 2 chips measured
- BER rather high on the permutation outputs (10^{-4}) at 7 GHz
- BER on debug shift-registers (SR) reasonable (10^{-18}) at 7 GHz

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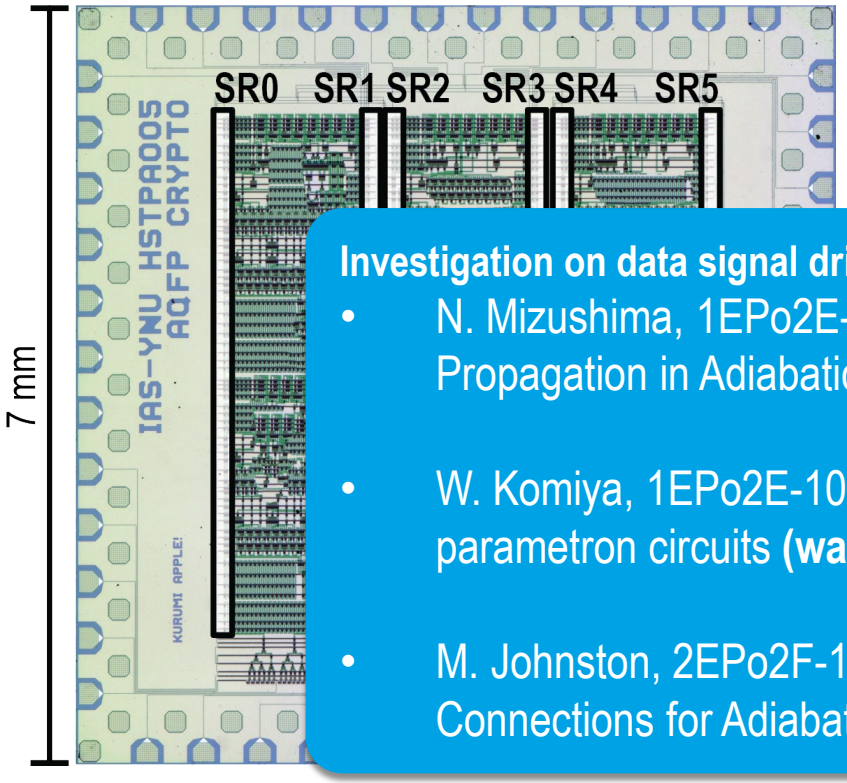
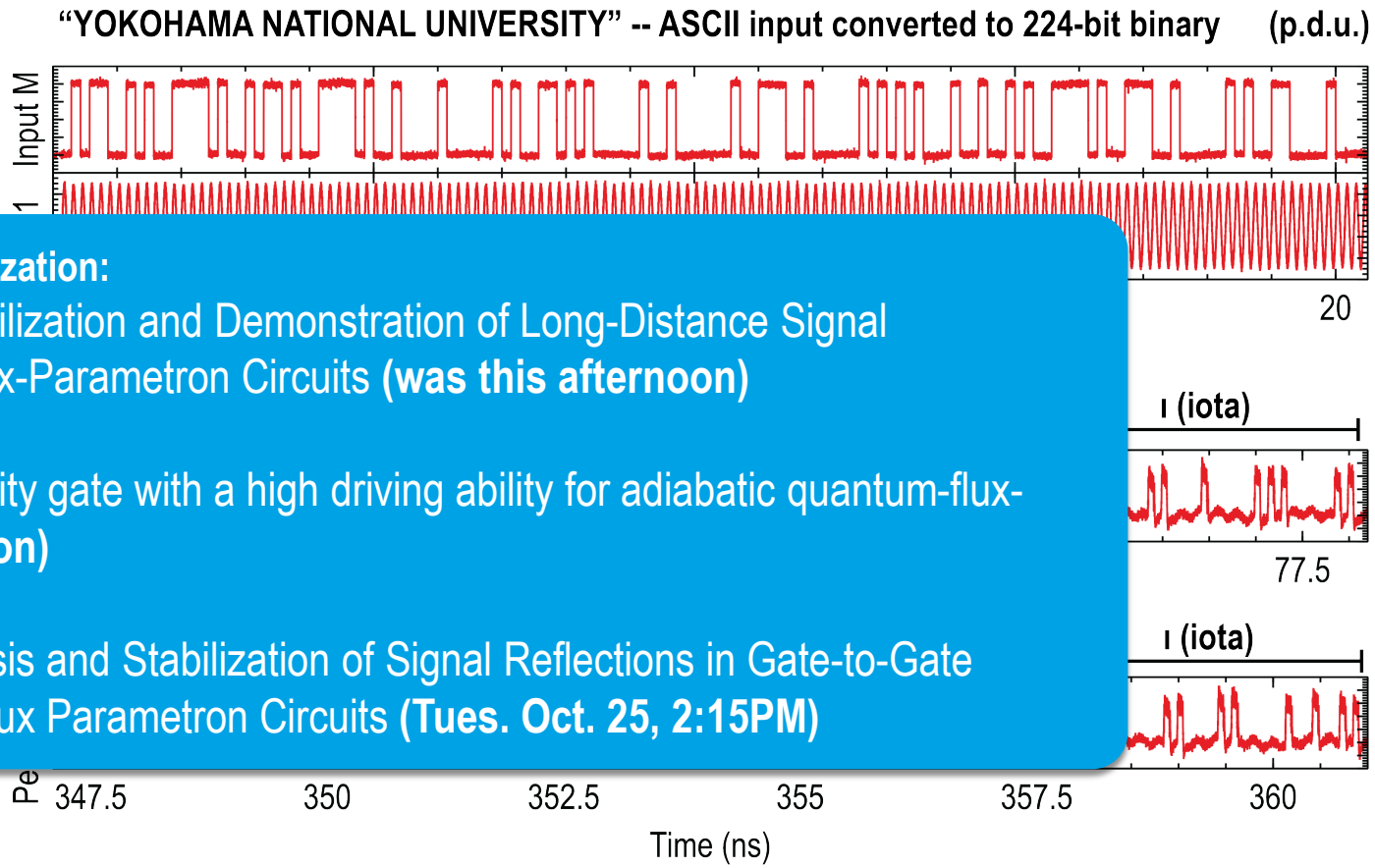
Measurement of permutation block



Divided into 14 x 16-bit X_i



Investigation on data signal driving and stabilization:

- N. Mizushima, 1EPo2E-09 [E41]: Stabilization and Demonstration of Long-Distance Signal Propagation in Adiabatic Quantum-Flux-Parametron Circuits **(was this afternoon)**
- W. Komiya, 1EPo2E-10 [E42]: A majority gate with a high driving ability for adiabatic quantum-flux-parametron circuits **(was this afternoon)**
- M. Johnston, 2EPo2F-10 [E43]: Analysis and Stabilization of Signal Reflections in Gate-to-Gate Connections for Adiabatic Quantum Flux Parametron Circuits **(Tues. Oct. 25, 2:15PM)**

JJ count: 13,008 JJs
Chip: 7 mm x 7 mm, 48 pad
Active circuit area: 5.0 mm x 5.6 mm
Maximum operation: 7 GHz
AC margins: +16% / -12%

- Complex test – PyVISA used to help automate experiment
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Summary and next steps

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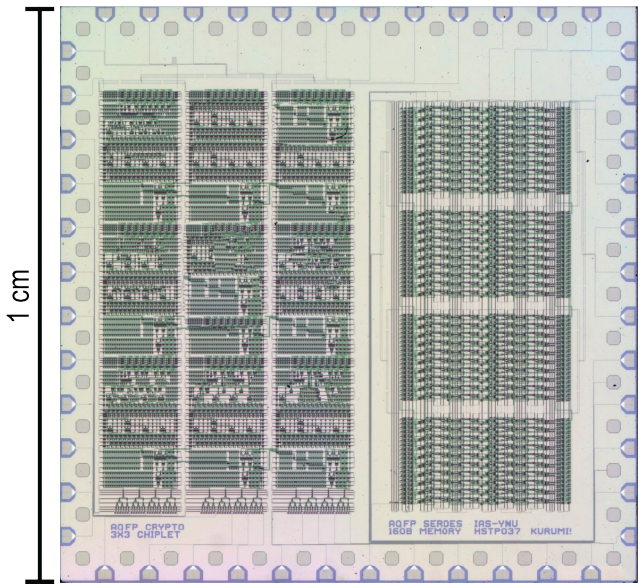
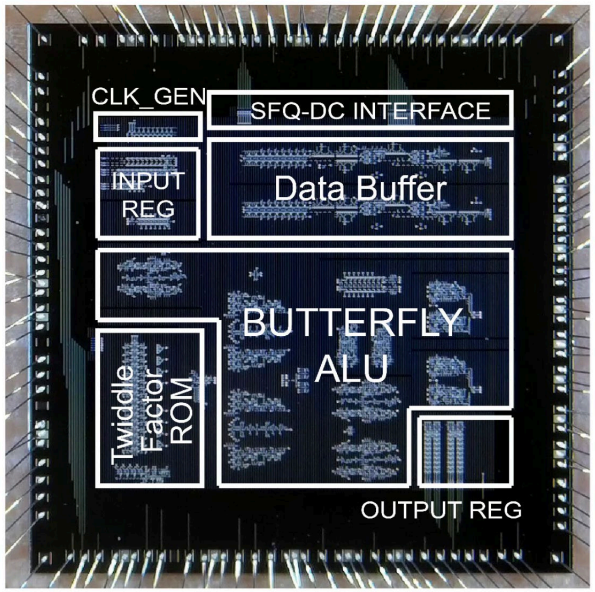
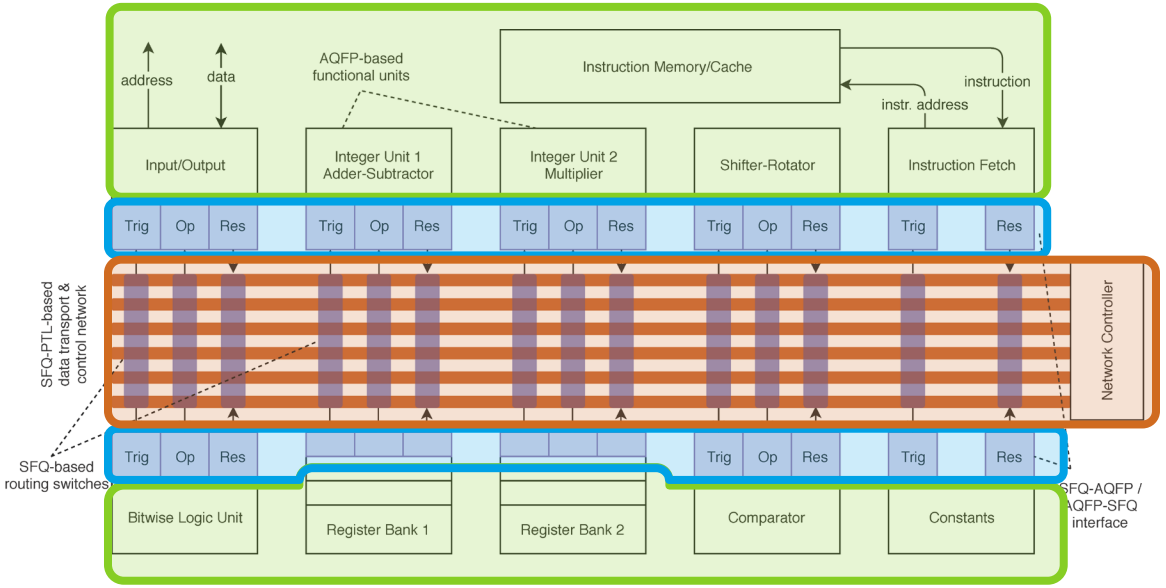
[1] F. Ke et al., 2021, DOI: 10.1109/TASC.2021.3059984
[2] L. Akçay and S. B. Ö. Yalçin, 2021, DOI: 10.3906/elk-2003-27



b=200-bit SHA3 crypto chip (1 cm x 1 cm)



RSFQ 47.8 GHz FFT processor [1]



AQFP circuits: TTA execution units and distributed registers

RSFQ<->AQFP: Interface between SFQ/AQFP circuits

RSFQ circuits: Transport network and routing

Candidate architecture for a future MANA-II processor

Summary:

- First successful demo of an AQFP SHA3 permutation unit at 7 GHz (b=25 bits)
- Insight on BER consistent with ongoing research on interconnect

Moving forward:

- Measurement of 200-bit state SHA3 AQFP chip
- Leverage FFT work for Number Theoretic Transform (NTT) for fully homomorphic encryption processing
- Consideration of Transport Triggered Architecture (TTA) -- performance/power advantage over RISC-V implementations for post-quantum cryptography [2]

Summary and next steps

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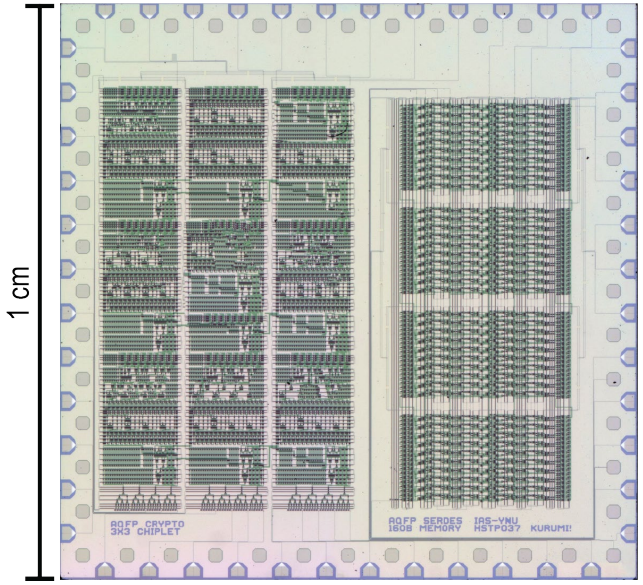

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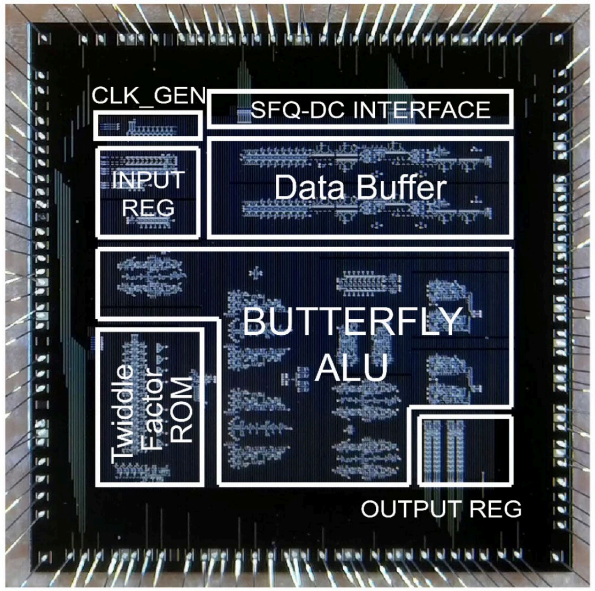

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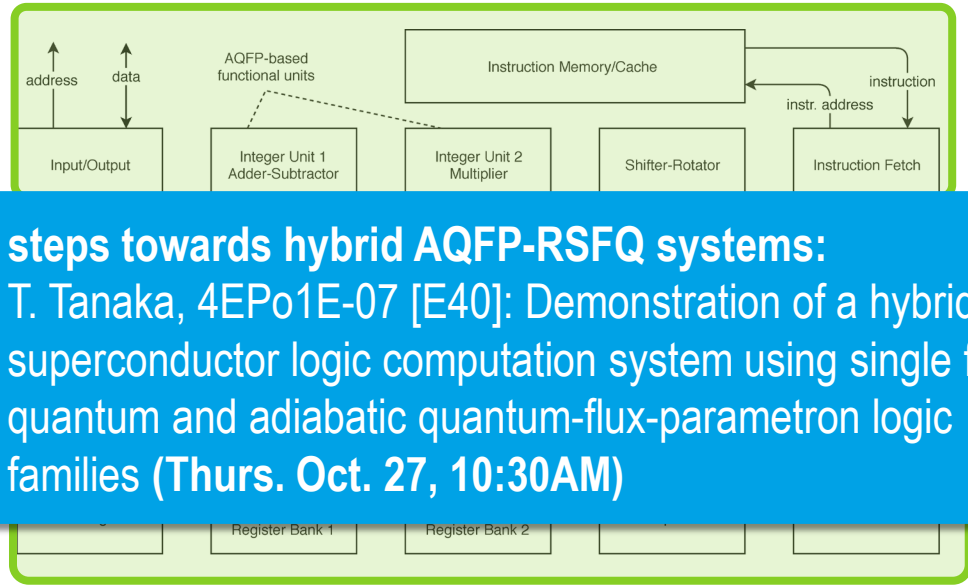

First steps towards hybrid AQFP-RSFQ systems:

- T. Tanaka, 4EPo1E-07 [E40]: Demonstration of a hybrid superconductor logic computation system using single flux quantum and adiabatic quantum-flux-parametron logic families **(Thurs. Oct. 27, 10:30AM)**

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Questions?

Thank You

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This work was also supported by the VLSI Design and Education Center (VDEC) of the University of Tokyo in collaboration with Cadence Design Systems, Inc.

The circuits were fabricated in the Clean Room for Analog-digital superconductiVITY (CRAVITY) of the National Institute of Advanced Industrial Science and Technology (AIST) using the high-speed standard process (HSTP). Circuits were also fabricated by MIT Lincoln Laboratory using the SFQ5ee process under the IARPA SuperTools program.