Recent Activities at ISTEC

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***Abstract* – This overview presents recent activities at ISTEC in Japan. ISTEC has restructured its organization in order to concentrate the efforts toward practical applications of superconducting materials and films. At SRL of ISTEC, remarkable results have been obtained in the previous NEDO projects in the fields of coated conductors and SFQ devices. These results have been inherited by new NEDO projects, which are further progressing toward the practical applications of superconductivity. The state of affairs of ISTEC and achievements of SRL/ISTEC are reviewed.**

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***Keywords* – Coated conductors, IBAD, M-PACC, NDE, PLD, SFQ, SQUID, TFA-MOD**

Abbreviations Used:

ADC:	analogue to digital converter
AIST:	National Institute of Advanced Industrial Science and Technology
CC:	Coated Conductor
HTS:	High Temperature Superconductor
IBAD:	Ion Beam Assisted Deposition
ISTEC:	International Superconductivity Technology Center
LTS:	Low Temperature Superconductor
METI:	Ministry of Economy, Trade and Industry
M-PACC:	Materials & Power Application of Coated Conductors
NDE:	Non-Destructive Evaluation
NEDO:	New Energy and Industrial Development Organization
PL:	Project Leader
PLD:	Pulsed Laser Deposition
R&D:	Research and Development
REBCO:	Rare-earth (*e.g.*, yttrium, Y) cuprate $REBa_2Cu_3O_{7-\delta}$
SFQ:	Single Flux Quantum
SMES:	Superconducting Magnetic Energy Storage
SPL:	Sub-Project Leader
SQUID:	Superconducting Quantum Interference Device
SRL:	Superconductivity Research Laboratory
TFA-MOD:	Tri-Fluoro-Acetate-Metal-Organic-Deposition
UTC-PD:	Uni-Traveling-Carrier-Photo-Diode

I. INTRODUCTION

SRL of ISTEC [1] in Japan is developing superconductivity technology since it was established in 1988. This article presents an overview of recent activities at SRL/ISTEC.

More than 20 years have passed since the discovery of HTS in 1986. In the past two decades, SRL research direction has been changed according to the development stage of the technology. In the early stage of work, efforts were focused on finding new materials and developing fundamental technologies for bulks, wires, thin films, and devices. Recently, the direction of R&D in superconductivity at SRL has been changed from basic technology development to practical applications of HTS materials. SRL is now developing high-performance coated conductors, superconducting power equipments, as well as superconducting electronic devices.

Accordingly, organization of ISTEC was fairly drastically changed in 2008. New organization aims at the development of practical technologies for industrial applications.

SRL/ISTEC is now involved in a big national project to develop superconducting power equipment including SMES, cables and transformers utilizing yttrium-based coated conductors, as well as to further improve these CCs. Main effort at SRL is directed towards the development of high-performance CCs for power equipment such as mentioned above. SRL is also developing HTS thin film devices for SQUID applications and LTS SFQ devices for high-speed system application. Detailed activities at SRL/ISTEC are described in the following.

II. NEW ISTEC ORGANIZATION

Dr. Shoji Tanaka was Director General of SRL for about 20 years, since the establishment of ISTEC. He retired from ISTEC in 2008, and Dr. Yuh Shiohara was assigned to be the new Director General. Other change in ISTEC was the unification of localized laboratories. Nagoya Coated Conductor Center in Nagoya and other laboratories located in different places were closed and combined with SRL at Shinonome in Tokyo. The headquarter office of ISTEC at Shinbashi in Tokyo also moved to Shinonome. Consequently, the whole ISTEC organization was unified at Shinonome, with exception of the Low Temperature Superconducting Device Division in Tsukuba. This Division used to be located in the NEC Laboratory campus in Tsukuba, but recently moved to the AIST campus and has been collaborating with the superconducting device group in AIST. Gathering in one place, researchers can easily concentrate their efforts aiming at practical applications.

The organization of ISTEC is shown in Figure 1. The right hand part shows the organization of SRL. SRL has four research and development divisions. They are (1) Superconducting Tapes and Wires Division, (2) Electric Power Equipment Division, (3) Electronic Devices Division, and (4) Advanced Materials and Physics Division.

The Superconducting Tapes and Wires Division has been developing practical coated conductors for superconducting power devices. The Electric Power Equipment

Division was newly established in 2008 to promote the development and insertion to the power grid of HTS electric power equipment using YBCO CCs. The Electronic Devices Division has been developing HTS and LTS thin film devices. The LTS devices are being developed in the Low Temperature Superconducting Device Division in Tsukuba. The Advanced Materials and Physics Division develops (from the scientific point of view) fundamental technologies for coated conductors, including characterization and new materials.

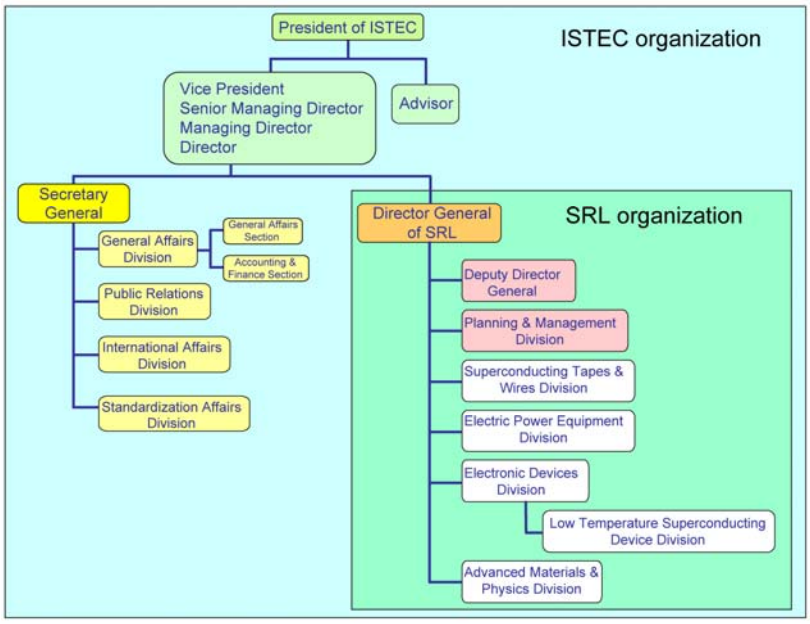


Fig.1. The ISTEC organization.

III. CURRENT PROJECTS

A. NEDO Projects

ISTEC is currently involved mainly in two NEDO projects, (1) Technological Development of Yttrium-based Superconducting Power Equipment [2], and (2) Development of Next-generation High-efficiency Network Device Technology [3]. These projects are described in this section.

B. Technological Development of YBCO-based Superconducting Power Equipment

The former 5-year NEDO project, "Fundamental Superconducting Application Technologies (Phase II)", ended successfully in March 2008. Remarkable results were obtained. One of the distinguished results is the successful development of the coated conductor fabrication technology to produce 500-m-long CCs with

300A/cm-width by using both IBAD-PLD [4] and IBAD-TFA-MOD deposition methods [5]. To build on these results, a new project started in June 2008. The project was named "Technological Development of Yttrium-based Superconducting Power Equipment", so-called M-PACC Project (Materials & Power Application of Coated Conductors Project). It is scheduled to continue till the end of FY 2012*.

The purpose of this project is to assess the prospects for practical applications of superconducting power equipments. In this project, technologies are developed for three different kinds of power equipments using yttrium-based superconducting coated conductors, including SMES, power cable, and power transformer. Higher performance coated conductors are also developed in this project in order to enhance the cost effectiveness of such equipment. Artist's conception of the urban area grid with introduction of such equipment is shown in Figure 2.

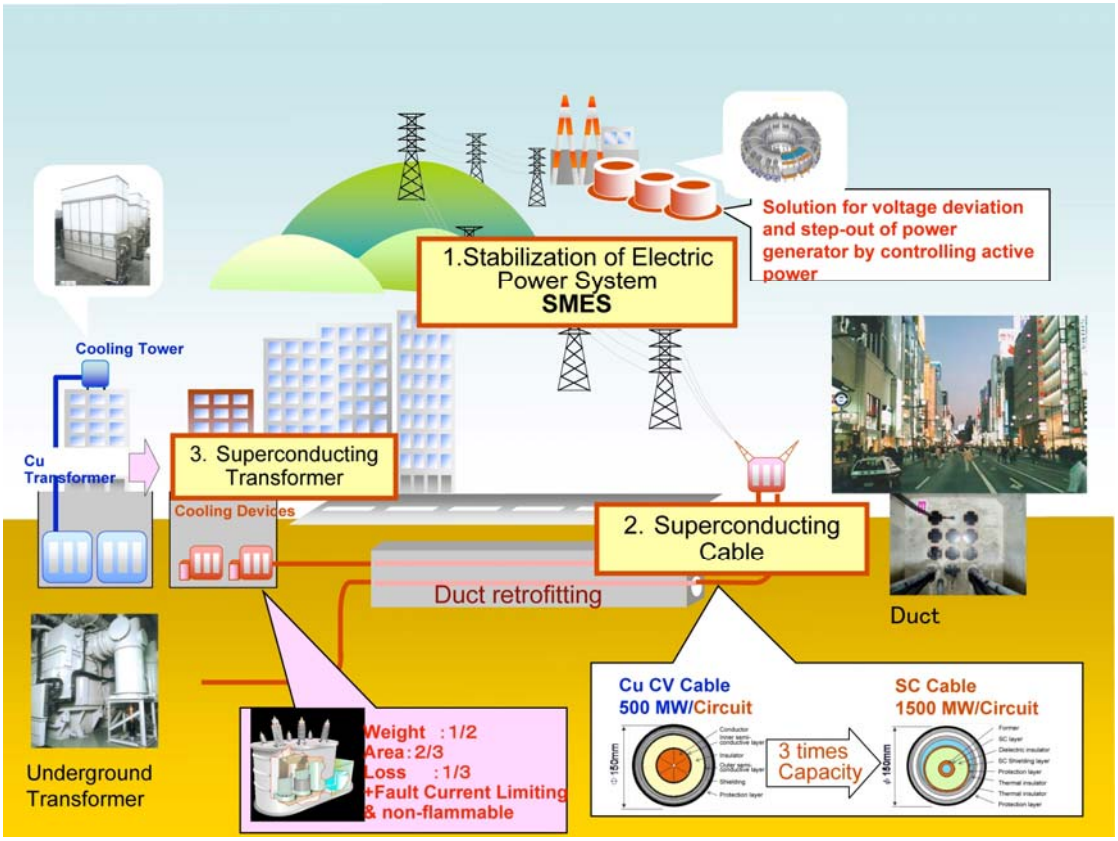


Fig.2. Artist's sketch of the conceptual design of stable large-capacity power supply system in an urban area after introducing SMES, power cable, and power transformer.

*FY: Japanese fiscal year starts at April 1st, and it ends at March 31st of the next year.

Figure 3 shows the organization of M-PACC Project. This project is supported by METI through NEDO. The PL is Dr. Yuh Shiohara, the Director General of SRL/ISTEC. This project consists of four sub-projects, SMES, Cable, Transformer, and Coated Conductors. Each sub-project is managed by a SPL. Electric power companies, cable companies, and many other companies including wire manufactures, research institutions, and universities are involved in this project as shown in Figure 3. Standardization of superconducting wires and power equipments is also promoted in this project. The project schedule is shown in Figure 4. Contents of each sub-project are described in the followings.

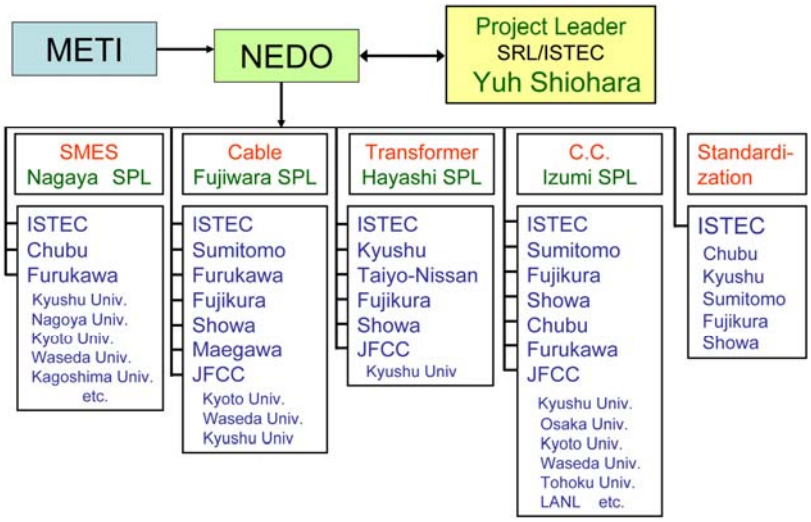


Fig.3. The M-PACC Project organization.

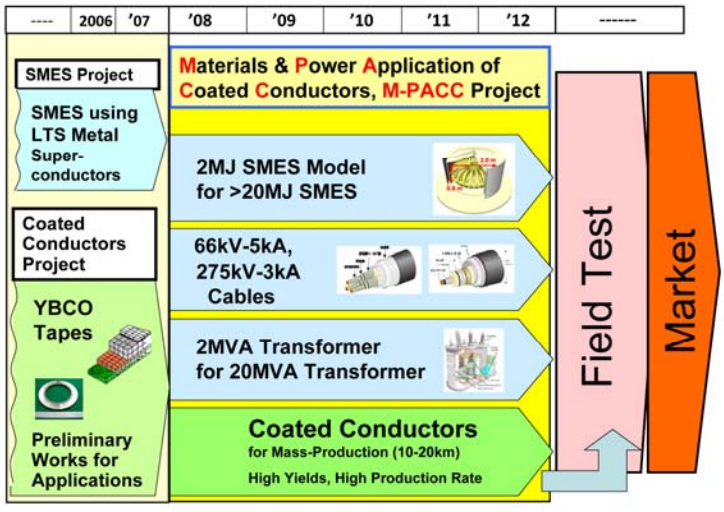


Fig.4. The M-PACC Project schedule.

C. SMES

Technology necessary for practical application to a 2 GJ-class SMES will be developed in this project. The external view (artist's sketch) of the designed 2 GJ-class SMES is shown in Figure 5.

Basic technologies for SMES were developed in the former project "Development of Superconducting Power Network Control Technology" which ended in FY2007. This project has been also called "The SMES Project". The M-PACC Project succeeded the SMES Project to further advance its results.

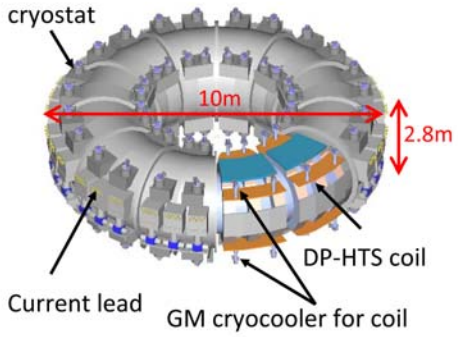


Fig.5. External view of the designed 2 GJ class SMES.

In this project, 20 MJ-class element coils will be developed to confirm the technological feasibility of the 2 GJ-class coil. Superconducting coils incorporating YBCO CCs will be developed with the 600 MPa hoop stress, over 2 kA current conduction characteristics, and over 2 kV withstand voltage, under the operating temperature ranging from 20 to 50 K attained by conduction cooling. In the last two years of the project, 2 MJ-class high-magnetic-field SMES prototype will be constructed and its performance evaluated. It will serve as a verification model system for 20 MJ- and 2 GJ-class SMES.

D. Power Cable

Superconducting power cables with higher transmission efficiency and lower transmission loss than conventional power cables will be developed. Two different kinds of cables will be developed as shown in Figure 6. One is a 66 kV/5 kA three-core high-current cable, and another is a 275 kV/3 kA single-phase high-voltage cable. Key requirements in developing these cables are: (i) a large current capability with low AC-losses, (ii) high withstand voltage capability with low dielectric loss, and (iii) high-efficiency characteristics. These cables will be compact in comparison with conventional cables. For the last two years of the project, a long-term running test will be executed to verify the grid feasibility of both cable systems.

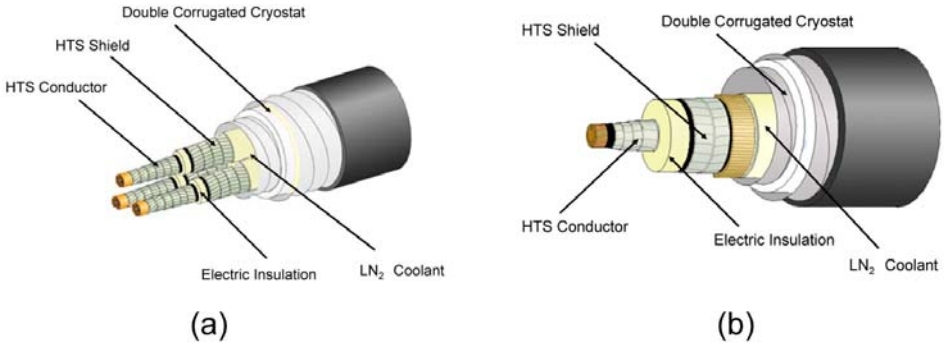


Fig.6. Superconducting power cables, (a) three-phase cable and (b) single-phase cable.

E. Power Transformer

A superconducting power transformer will be developed in this project. Its features include lower loss, higher compactness and incombustibility than those of existing power transformers. Essential technologies will be developed for realization of a 66kV/6.9kV-20MVA superconducting power transformer. A conceptual design sketch of the superconducting transformer external view is shown in Figure 7.

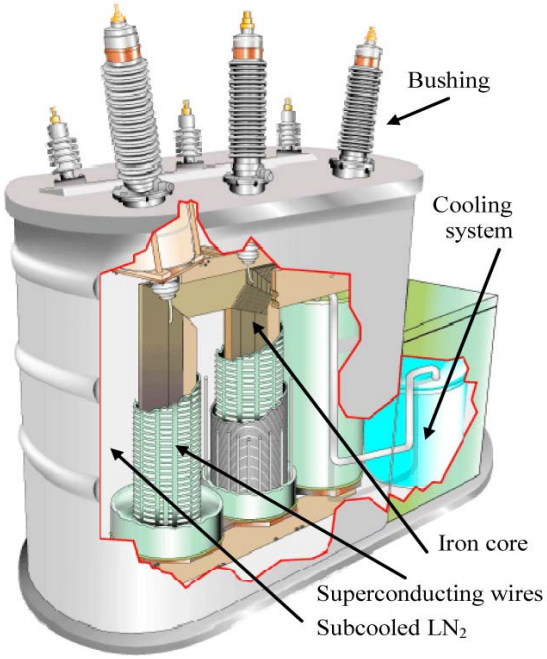


Fig.7. External view of the superconducting power transformer.

Essential technologies to be developed in this project include 2 kA-class large current coil technology, anti-short circuit coil technology, AC-loss reduction technology,

insulation technology, and cooling technology with the development of a high-efficiency Turbo Brayton cryocooler. By combining these technologies, system technology of the superconducting power transformer will be developed. In the last two years of the project, a 66kV/6.9kV-2 MVA transformer will be developed to verify the system feasibility, and also a few hundreds kVA class transformer with fault current limiter will be developed.

F. Coated Conductors

In SRL, key technologies for high-performance coated conductors have already been developed. These technologies, shown in Figure 8, were developed in the former project "Fundamental Superconducting Application Technologies (Phase II)", which is simply called here the "CC Project". Using these technologies, 500-m-long and 300 A-class wire fabrication is now possible [4], [5]. The earlier mentioned M-PACC Project builds on the results of the CC Project and it will further advance the conductor fabrication techniques and performance. In order to develop electric power equipment mentioned above, the total wire length of 20 to 30 km is needed. Thus stable mass-production technique of YBCO-coated conductors is indispensable. It is also necessary to improve fabrication yield as well as the manufacturability, performance, and reliability of wires, as appropriate for industrial products.

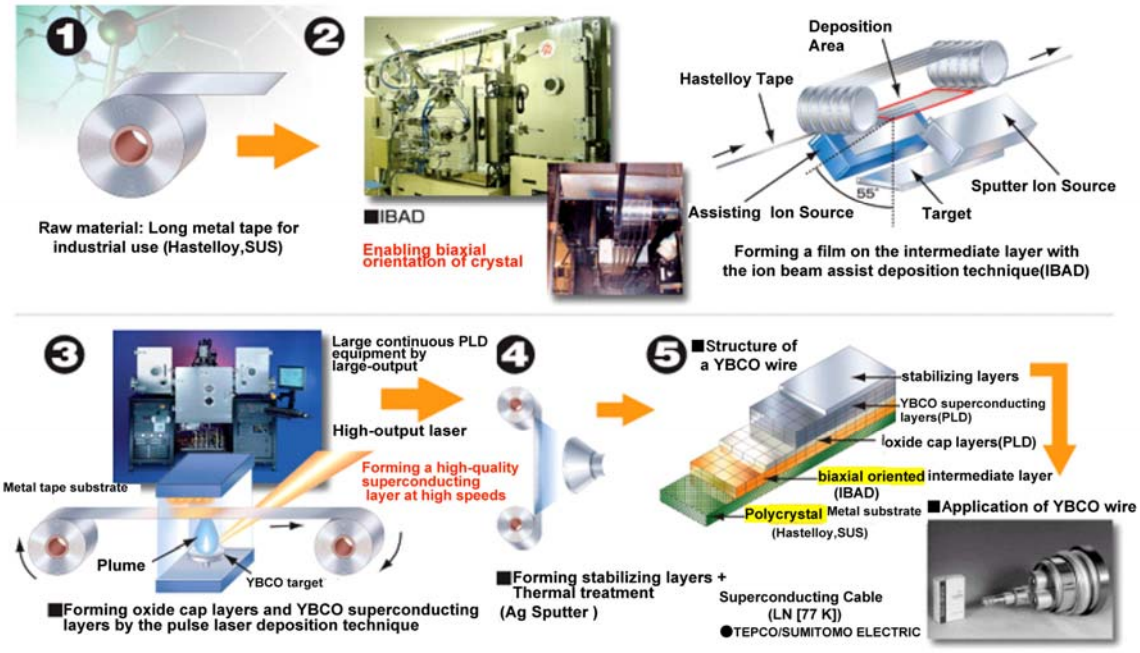


Fig.8. Integrated wire fabrication process with the IBAD-PLD technique. This process is now used in SRL/ISTEC, and key technologies in this process have been transferred to cable/wire making companies which supply coated conductors for development of the power equipments. In SRL/ISTEC, an advanced fabrication process is also being developed for conductors to be used in future power equipment systems.

Crucial for the future acceptance of HTS power equipment will be a drastic reduction of the presently high manufacturing cost, which is largely defined by the cost of CC coils. The ISTEC pursues in parallel two alternative CC fabrication routes, because it isn't yet clear which will eventually result in the overall lower cost? Although the TFA-MOD manufacturing cost per meter is low, IBAD-PLD shows excellent cost performance per ampere. Therefore, it is difficult to decide at present which technique will be more cost effective in the future - in terms of cost per ampere-meter.

F. Development of Next-generation High-efficiency Network Device Technology

Before the inception of this project, the HTS and LTS electronic devices were developed in the NEDO project "Low-power Superconducting Network Device", which continued from FY2002 to FY2006. In this project, many remarkable results were obtained in areas of both HTS and LTS devices. These results are reviewed in the next section.

Results in HTS devices are the base of the NEDO M-PACC Project, which has been described above. The HTS device integration technologies developed in the former project are applied to fabricate integrated SQUID sensors with integrated pickup coils. The inspection system utilizing such integrated SQUID is being used to find defects in coated conductors developed in the M-PACC Project.

A New NEDO project "Development of Next-generation High-efficiency Network Device Technology", which started in June 2007 bases on the results in LTS devices attained in the former project. The present project will continue to FY2011. It aims at establishing enabling technologies for the next generation high-efficiency networks. Details of the project are given elsewhere [7]. In this project, the main target is to develop highly efficient large-scale edge routers, ultra high-speed local area networks and related telecommunication systems as illustrated graphically in Figure 9. Main technologies are developed by using CMOS high-speed devices and optical I/O devices. LTS device is also included in this project. A real-time monitoring system for optical communication will be developed using LTS SFQ devices.

The Project Leader is Prof. Tohru Asami of The University of Tokyo, Dept. of Information and Communication Engineering. Project members and their missions are as follows;

OITDA (Optoelectronic Industry and Technology Development Association: Hitachi, Fujitsu, NEC, Mitsubishi, NTT): Optical device
AIST: Optical device
NHK (Japan Broadcasting Corporation): SHV (Super High Vision) system
ALAXSALA Networks Corporation: Electrical router system
ISTEC: Superconducting device.

The target of R&D at ISTEC is to develop a real-time optical waveform monitoring system using superconducting devices. The present status of LTS devices in this project will be described in the next section.

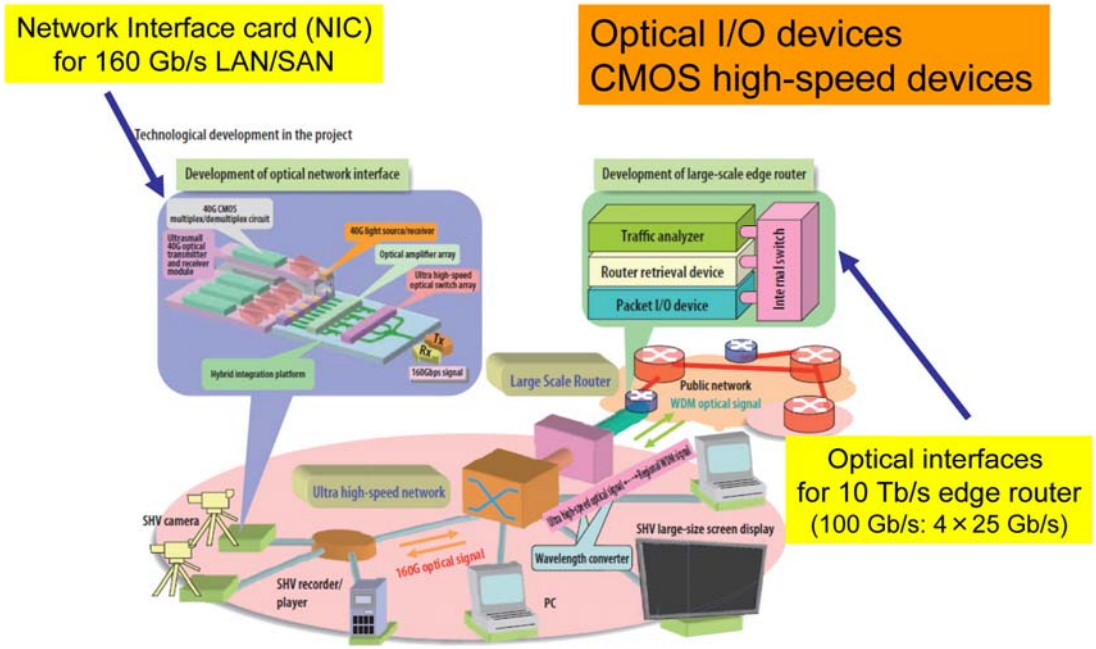


Fig.9. Technological map of the NEDO project "Development of Next-generation High-efficiency Network Device Technology" [7].

IV. ACTIVITY OF EACH DIVISION OF SRL/ISTEC

A. Superconducting Tapes & Wires Division

This division aims at research and development of the coated conductor fabrication process technology to realize superconducting wires appropriate for future power equipments. R&D themes are to attain the following performance:
(1) High-critical current (I_c) under high-magnetic fields,
(2) High-strength and high overall critical current density (J_c),
(3) Low-cost and high-yield fabrication process, and
(4) Reduction of AC loss.

The IBAD-PLD process for coated conductors has been already depicted in Figure 8. The typical architecture of a coated conductor now being developed is shown in Fig.10. Substrates with highly textured buffer layers are prepared by the combination of ultra-thin IBAD-GZO ($GdZrO_3$) or IBAD-MgO and PLD-CeO_2 cap layers. A high production rate process resulting in 5-10 m/h of tape length has been realized for well textured substrates [8]. Figure 11 shows the IBAD fabrication system which can deposit an MgO film with high in-phase grain alignment and high fabrication rate. The ion beam pictured through a window of the system is also shown in the figure.

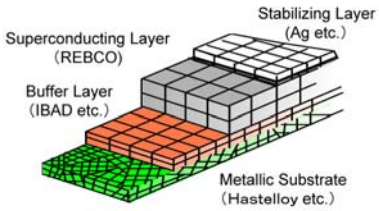


Fig.10. Basic structure of coated conductors.

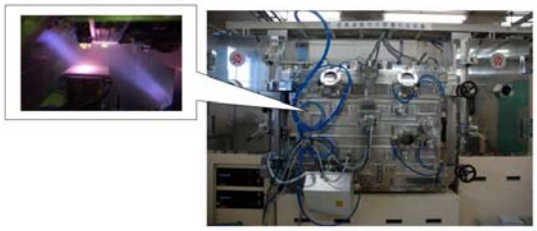


Fig.11. The IBAD system.

A superconducting layer is deposited with a PLD system as shown in Figure 12, in which a schematic illustration of multi-turn and multi-plume (MTMP) PLD is also shown. By using this system, high yields of material and a high production rate as high as 5-10 m/h for the superconducting layer has been achieved [9]. Good I_c uniformity over lengths of conductor tape have been demonstrated (see below). Development of a higher production rate with higher critical currents for further reduction of the technological cost is now being progressing.

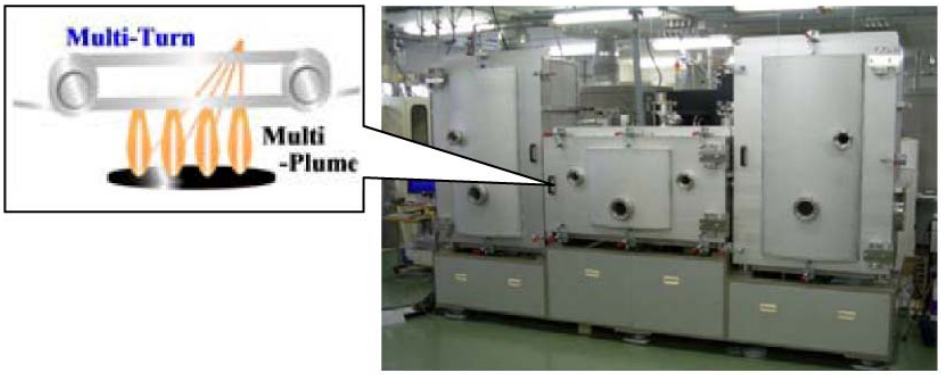


Fig. 12. The PLD fabrication system

The other method to deposit superconducting layer also investigated in the project is TFA-MOD. The fabrication equipment is shown in Figure 13. It aims at an extremely low-cost fabrication process. Controlling the starting solution in the TFA-MOD process, high critical currents reaching 735 A/cm-width were demonstrated [10]. High production rates in both calcinations and crystallization steps were realized by multi-turning systems. High uniformity in performance with high production rates has been also achieved as shown below.

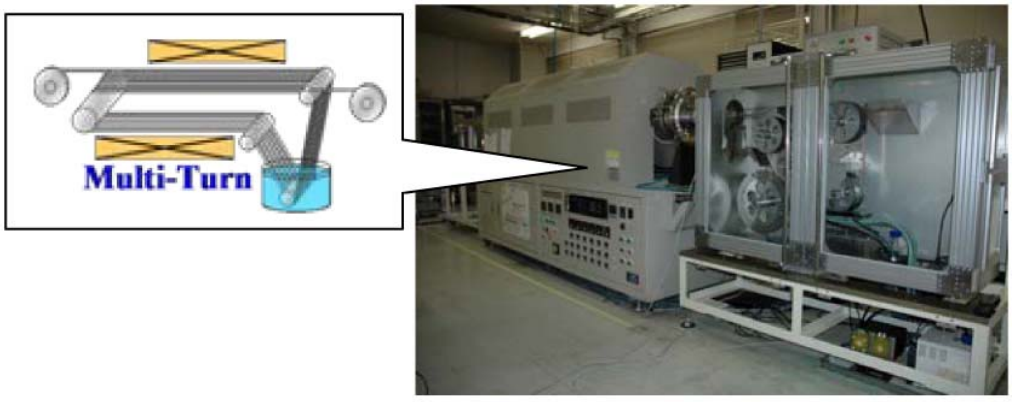


Fig. 13. The TFA-MOD deposition system

Recent Results in IBAD-PLD

A high-current long tape technology has been developed using PLD-REBCO (RE: Rare Earth) layer on IBAD-GZO substrate. Figure 14 shows an example of a 200-m-length tape of GdBCO on IBAD-GZO [9]. The end to end critical current (I_c) value was 220 A for a 1-cm-wide tape. Its angular dependence on the magnetic field direction is shown in Figure 15, which shows the dependence of I_c upon the applied magnetic field angle Θ. The angle Θ = 0° corresponds to the magnetic field H parallel to c-axis while at Θ = 90° the field H is parallel to the a-b plane. Although conventional YBCO tapes have a strong dependence on the applied magnetic field direction, a GdBCO tape has less dependence and a GdBCO with ZrO_2 admixture tape exhibits almost no dependence on the field direction. This means GdBCO with ZrO_2 tape is suitable for power equipment applications. This technology was transferred to the Fujikura Company and they have succeeded in realization of a 500-m-long, 300 A/cm-width tape [4].

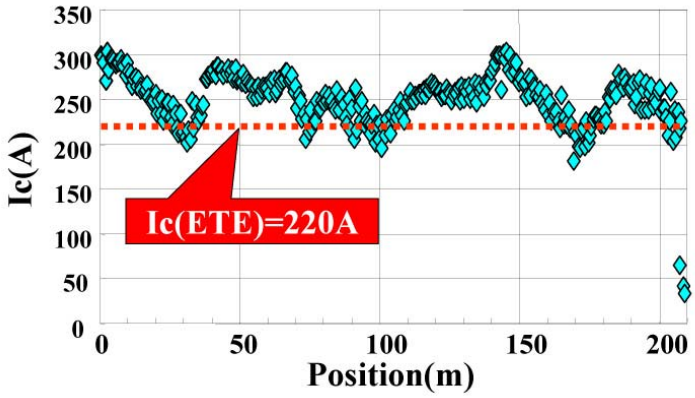


Fig.14. I_c distribution of 200 m-length PLD-GdBCO on IBAD-GZO tape.

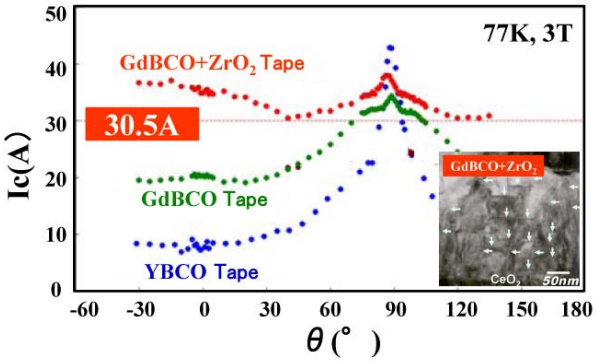


Fig.15. Magnetic field angle (Θ) dependence of I_c for three different tapes.

Recently, extremely high production rate was realized by IBAD-MgO systems for the purpose of lowering the cost of coated conductors fabricated with PLD-IBAD architecture [8]. Highly textured buffered substrate of:

$CeO_2/LaMnO_3$/IBAD-MgO/GZO/Hastelloy

could be fabricated at several tens of meters per hour. A GdBCO superconducting layer was deposited by PLD on the buffered substrate and a 45 m long coated conductor with high I_c values exceeding 500 A/cm-width was successfully demonstrated, as shown in Figure 16.

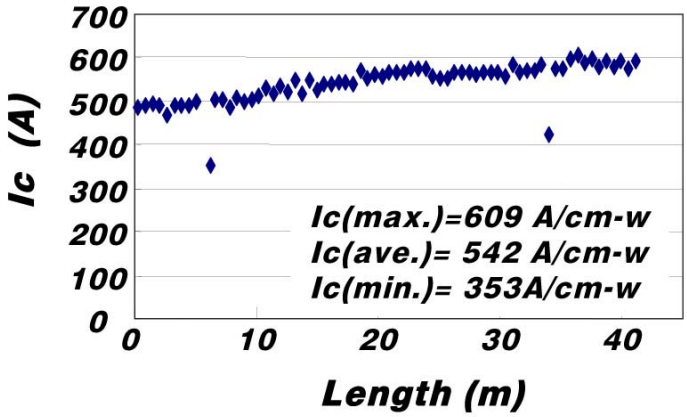


Fig. 16. I_c distribution of PLD GdBCO film on highly textured buffered substrate.

Recent Results in IBAD-TFA-MOD

A high critical current tape has also been developed with TFA-MOD REBCO films as shown in Figures 17 and 18. Figure 17 shows I_c distribution in a 90 m long TFA-MOD derived YBCO tape on IBAD-GZO with a PLD-CeO_2 cap layer. There was one point with low I_c at around the 30 m position, but other regions (56 m length) showed $I_c \geq 250$ A. Figure 18 shows YBCO film thickness dependence of I_c for three buffer layers with different degree of in-plane grain alignment angle. The critical

current of 735 A was attained by increasing the layer thickness without cracks and controlling the Ba deficiency in the composition [10].

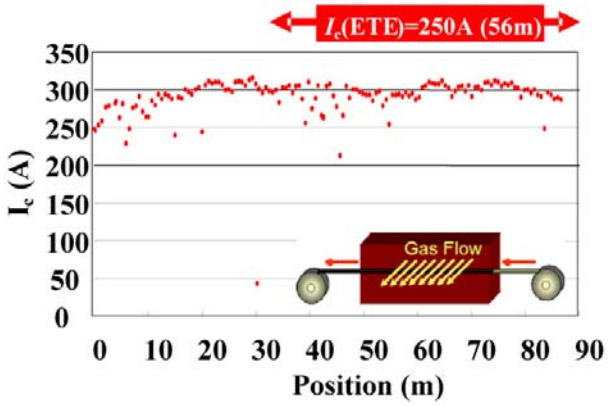


Fig.17. TheI_c distribution of TFA-MOD YBCO tape on IBAD-GZO.

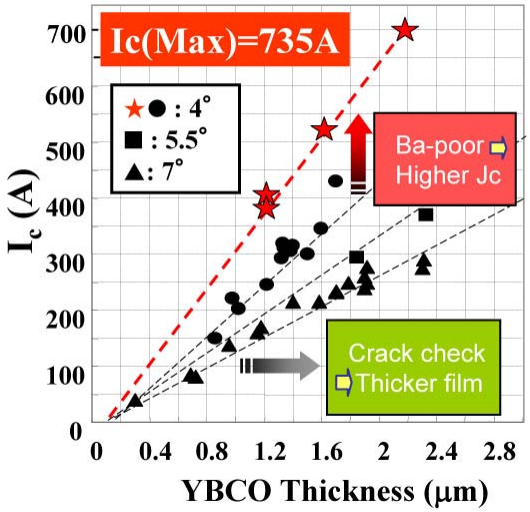


Fig.18. YBCO film thickness dependence of I_c for three buffer layers with different degree of in-plane grain alignment angle of 4°, 5.5°, and 7°.

Recently, the efforts to improve the superconducting performance under the magnetic field succeeded also in the case of TFA-MOD films. Remarkable progress was achieved through the RE mixture of Y with Gd and Zr-additions. Figure 19 shows the magnetic field angle (Θ) dependence of the critical current density (J_c) values in the films of YBCO, YSmBCO with Zr and YGdBCO with Zr. The isotropic behavior with high J_c values could be recognized in the film of YGdBCO with Zr-addition [10].

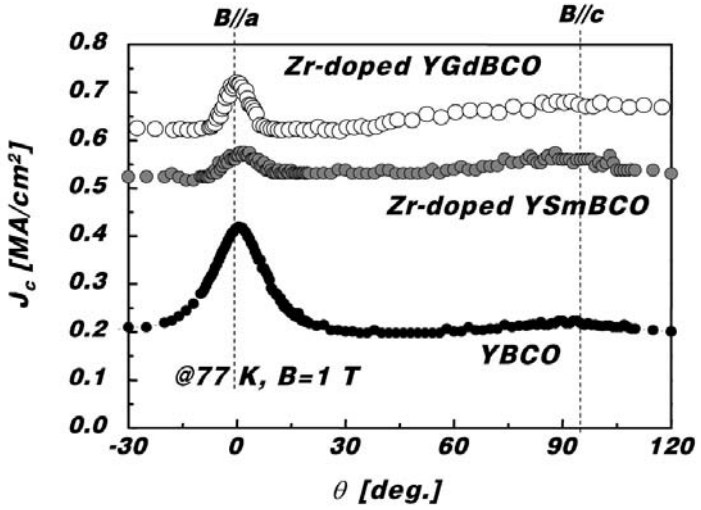


Fig.19. Magnetic field angle (Θ) dependence of J_c for three different films made by TFA-MOD.

B. Electric Power Equipment Division

This Division is closely collaborating with many companies and universities to develop the mentioned above three electric power grid components: SMES, power cables and power transformers with the attending superconducting fault current limiting function. The Division's mission is to develop all technologies necessary for such apparatus. Basic design studies are now proceeding. By the end of the project, prototypes of SMES, power cable, and power transformer will be developed.

C. Electronic Devices Division

In this division, both HTS and LTS electronic devices have been developed. LTS devices are being developed in the Low Temperature Superconducting Device Division in Tsukuba.

The following R&D themes are in progress for the HTS devices:

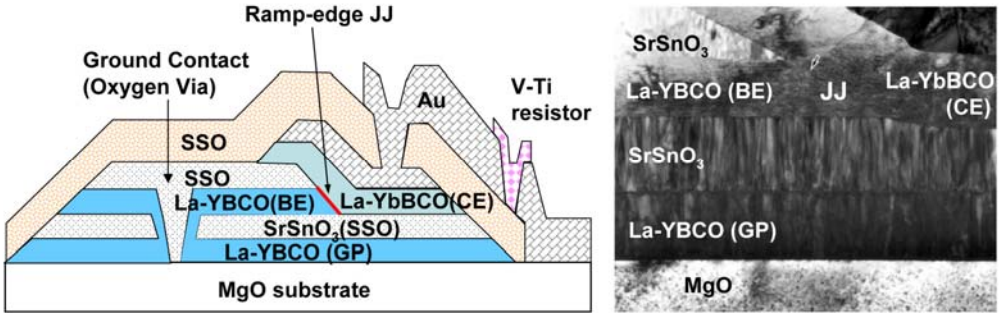
(1) Integrated fabrication process including HTS Josephson junctions,
(2) Design and fabrication of integrated SQUID,
(3) NDE system with integrated HTS SQUID, and
(4) Support for the development of power equipment and coated conductors with HTS SQUID NDE system.

Selected Results on HTS Devices

The integration technologies of Josephson devices with HTS materials have been advanced in the former project "Low-power Superconducting Network Device" [11].

Typical results are shown below.

Figure 20 shows a cross-sectional view of an HTS integrated circuit. (a) is a schematic illustration and (b) shows a cross-sectional TEM image. The main feature of this circuit is the multilayer structure including three HTS layers, SSO ($SrSn_3$) insulation layers, and a ramp-edge type Josephson junction with a minimum junction width of 2μm. By optimizing the fabrication process of each layer, functional HTS circuits have been reproducibly obtained. The standard deviation 1-σ of the critical current I_c is typically 6-10% and run to run spread of I_c is ±12 %.



(a) (b)

Fig.20. (a) Cross-sectional illustration of HTS integrated circuit, and (b) TEM image of an actually fabricated device.

This fabrication process was used to fabricate a sampler circuit. A sampling oscilloscope system has been demonstrated as shown in Figure 21. The system consists of a cooling unit, a control unit, and a PC. The size of the cooling unit is 140×150×200 mm^3 and its weight is less than 4 kg. It is a single-stage Stirling cooler with a cooling capacity of 1 W at 77 K. A typical 50 GHz waveform has been observed with this sampler system and it has been shown that it has a potential to observe signals at frequencies higher than 100 GHz.

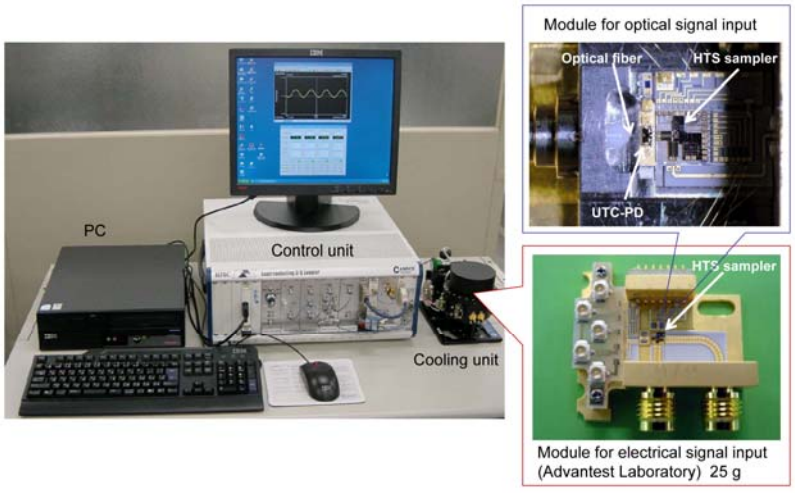


Fig.21. Sampling oscilloscope system with HTS integrated circuit.

The integrated circuit technology with HTS ramp-edge Josephson junctions was also used to a fabricate SQUIDs. Multiple SQUID sensors with pickup coils could be integrated on the same chip as shown in Figure 22. The lower right picture shows a set of a 5-channel gradiometer array while a magnified photo of one channel is shown in the left. The 3D picture of the main part of the gradiometer including a SQUID inductor and ramp-edge junctions is shown in upper right. In each sensor, the feedback coil is placed on the pickup loop. This SQUID gradiometer is robust against application of AC magnetic fields up to several mT, which is four orders of magnitude higher than that for conventional HTS SQUID made on bicrystal substrates. This is because ramp-edge junctions and pickup coils without parasitic weak links have less probability of flux trapping. Thus, this SQUID is very useful for NDE under fairly large excitation magnetic fields.

For reduction of AC losses in coated conductors, it is essential to striate them into multiple filaments. This SQUID array chip has been developed for use in NDE of striated coated conductors. Figure 23 shows a schematic illustration of a striated coated conductor with five filaments. Eddy currents in the moving coated conductor under test are excited by an external induction coil. If one of the filaments has a defect, as shown in the figure, a certain defect signal from one the five SQUID gradiometers appears when the defect passes under that gradiometer.

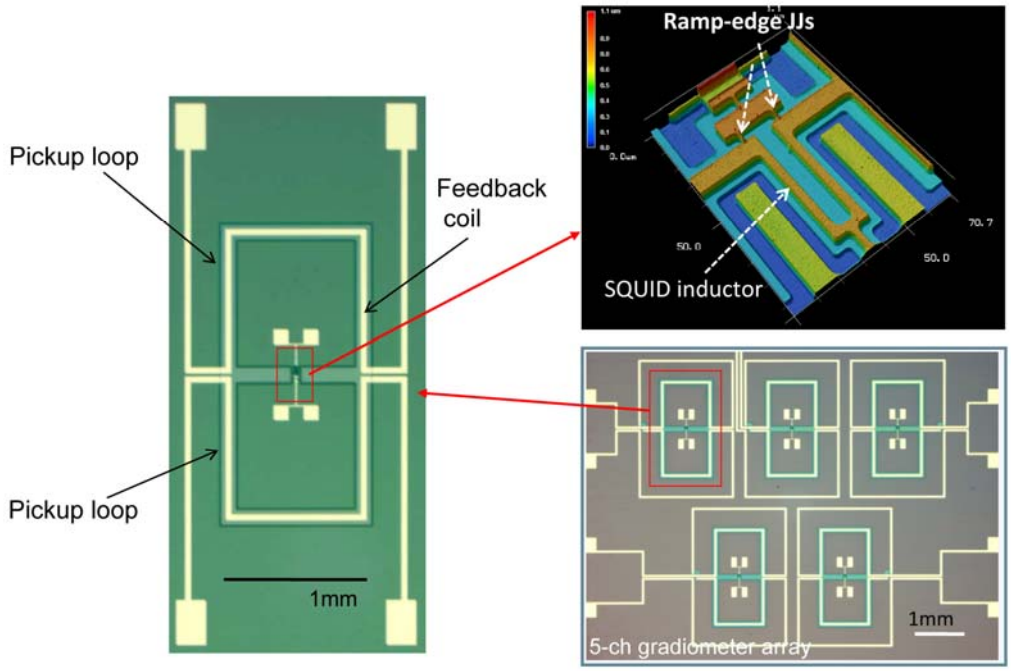


Fig.22. The 5-channel SQUID sensor chip.

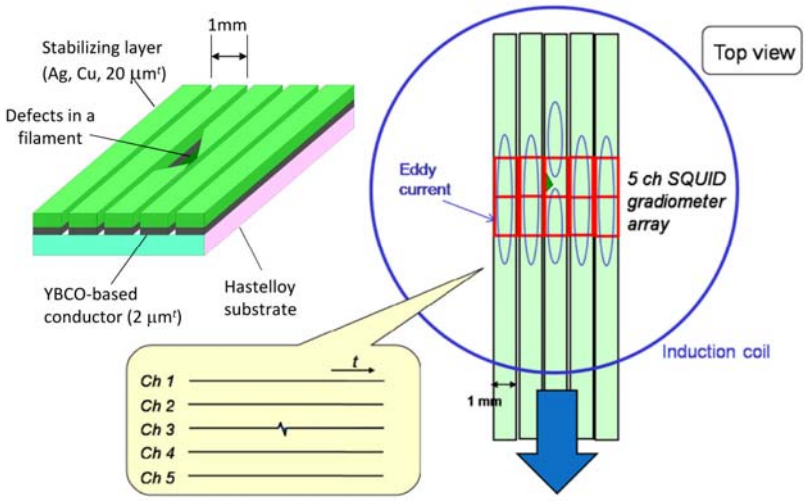


Fig.23. Schematic of defect evaluation of filamentarized wire.

A reel-to-reel NDE system for striated coated conductors has been developed by using the 5-channel SQUID gradiometer; the system view is shown in Figure 24 [12]. An example of measured data for a coated conductor before and after striation is shown in Figure 25. It is clearly seen that delaminated and/or electrically shorted regions of the filaments generate unique SQUID signals. This system is now used in the "M-PACC Project" for investigation of the coated conductors. The inspection speed of this system is about 100 m/h.

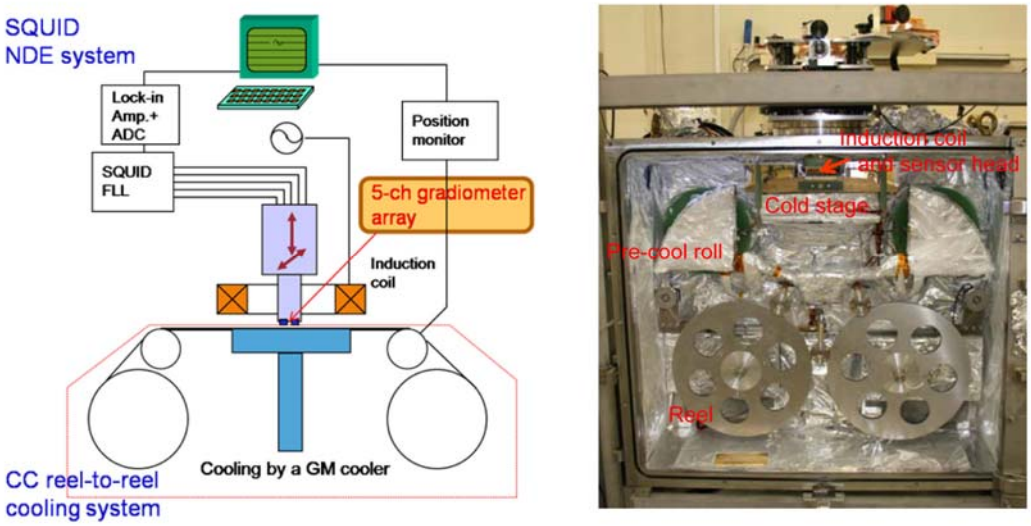


Fig.24. Reel-to-reel SQUID NDE system for striated coated conductors.

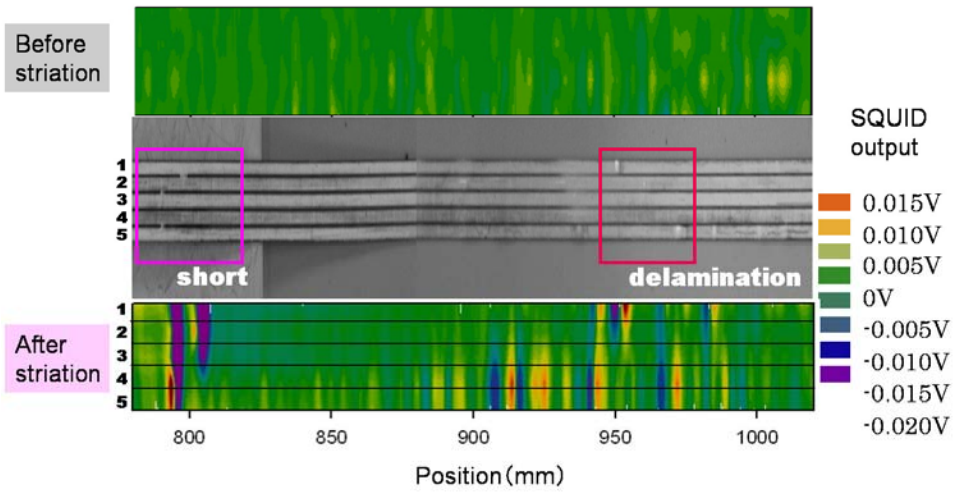


Fig.25. Defect measurement with 5-channel SQUID gradiometer. Upper and lower segments show SQUID data obtained before and after striation, and middle picture shows optical micrograph after striation.

Selected Results on LTS Devices

The results include:

(1) Integrated fabrication process with Nb/AlOx/Nb Josephson junctions and Nb wirings,
(2) Integrated high-speed circuit design,
(3) High-speed packaging operating in a cryocooler,
(4) High-speed small SFQ system, such as real-time oscilloscope, and
(5) Ultimate high-speed and low-power system.

In the former NEDO project "Low-power Superconducting Network Device", LTS SFQ circuits have progressed remarkably [13]. It has become possible to integrate 10 thousand Josephson junctions on a chip with an excellent operating chip yield as high as 10%. Josephson junctions in these SFQ circuits are made with two different fabrication processes; one is the standard process with the critical current density J_c of 2.5 kA/cm^2 and the other is the advanced process with J_c of 10 kA/cm^2. The minimum line width in circuits fabricated by this process is usually 1 micron. The next generation fabrication process with J_c of 40 kA/cm^2 is under development. SFQ processors and a switch for a router system have been developed [14], [15]. A photograph of a 4×4 switch chip is shown in Figure 26. This chip was operated with a clock frequency of 40 GHz, thus the effective 160 Gbps throughput was attained. Using the 4×4 switch chip, a video data transfer among four PCs was also demonstrated as shown in Figure 27.

In the new NEDO project "Development of Next-generation High-efficiency Network Device Technology", a real-time optical waveform monitoring system using a superconducting electronic device is now being developed. An example of the

developed device, a 4-bit ADC, is shown in Figure 28 [16]. A flash type ADC was also designed and tested. This chip is now being improved. High-speed operation with a clock frequency of over 100 GHz will be realized.

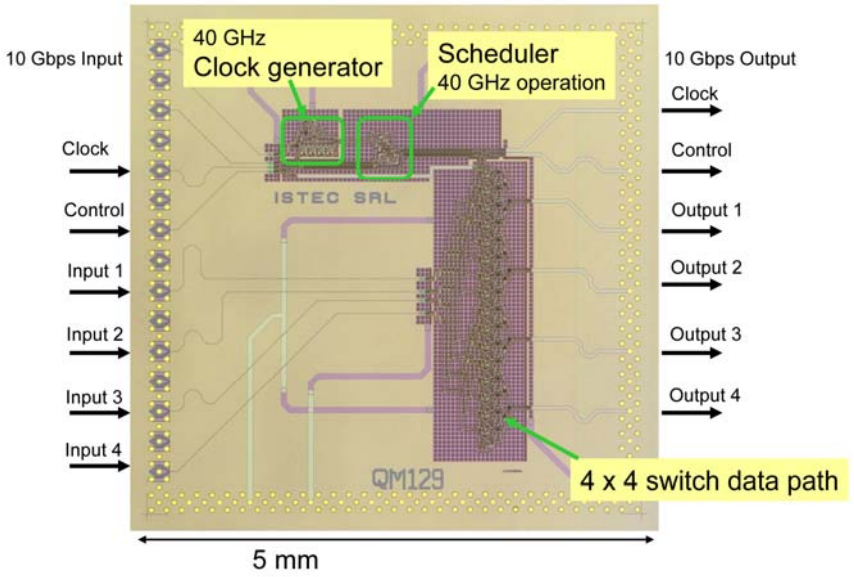


Fig.26. 4×4 switch chip.

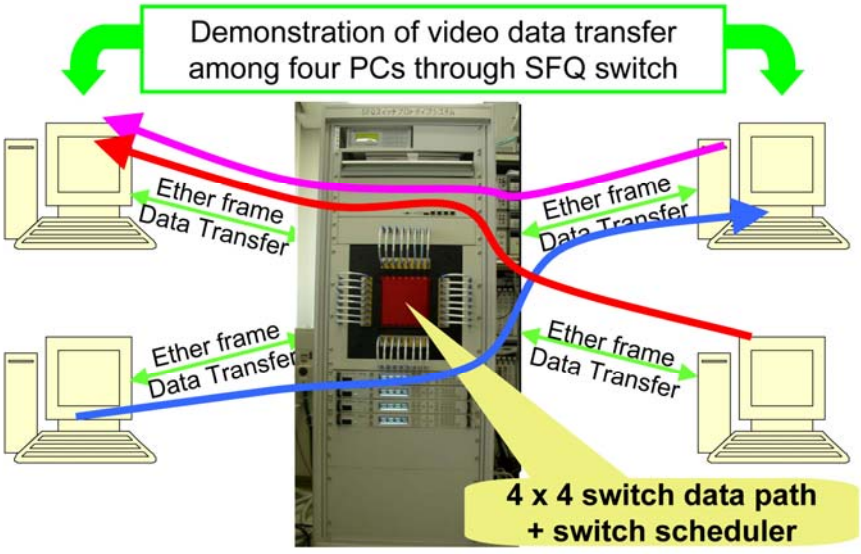


Fig.27. Vide data transfer demonstration with 4×4 switch system installed in a cryocooler).

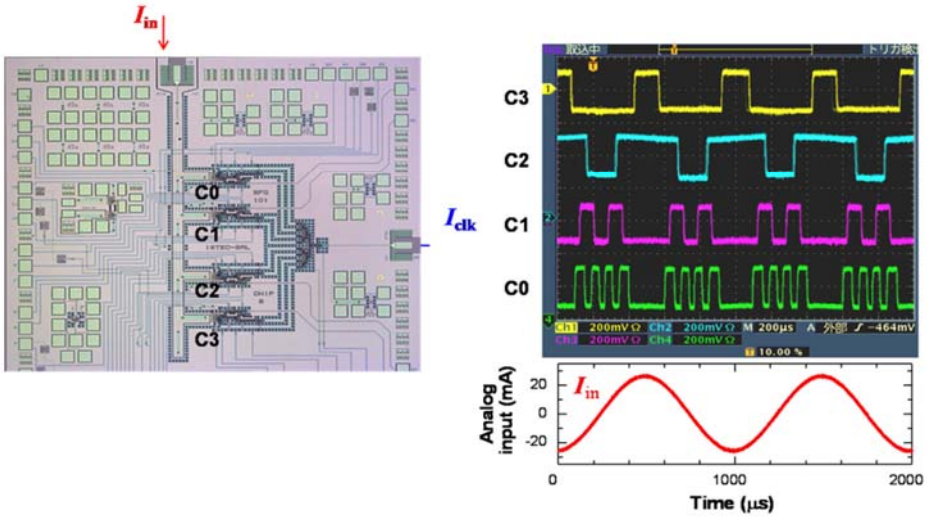


Fig.28. The 4-bit ADC chip photograph (left) and the device operation (right).

When the high-speed optical signal is monitored by a real-time oscilloscope, the first step is to convert the optical signal to the electrical signal. Thus the high speed optical input setup has been developed as shown in Figure 29 [17]. The optical input signal is converted to electrical signal with a UTC-PD cooled at 4 K and its signal is applied to the SFQ circuit. In the preliminary experiment, UTC-PD and 1:2 SFQ DEMUX (demultiplexing) circuits have been installed in the cryocooler which was used to cool the 4×4 switch system shown in Figure 27. It was confirmed that the bit error rate was less than 10^{-12} for the 40 GHz clock operation.

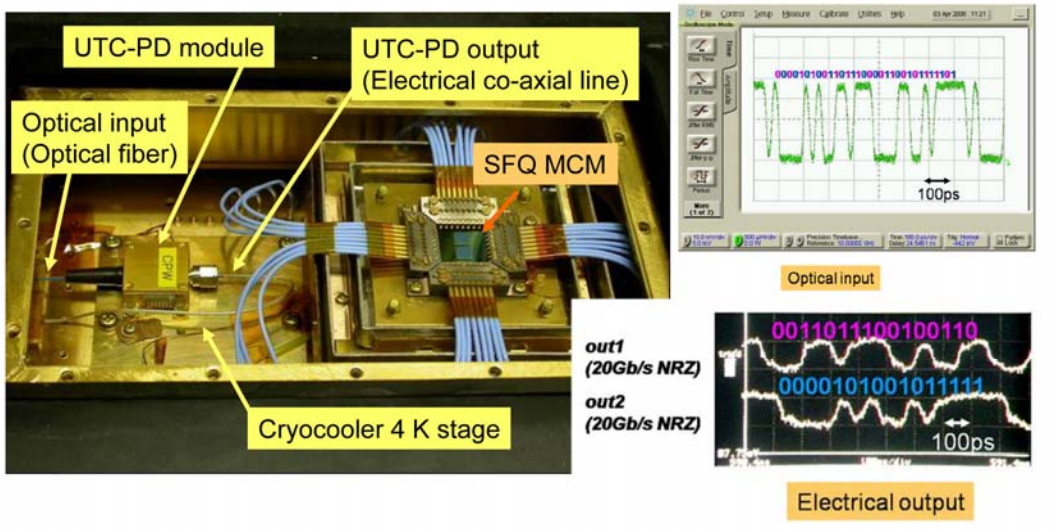


Fig.29. Optical input setup and its operation.

D. Advanced Materials and Physics Division

The R&D themes addressed by this division are as follows.
(1) Search for advanced superconducting materials with higher irreversibility field,
(2) Understandings of flux pinning mechanism and development of superconducting materials with higher critical current density (J_c) in magnetic fields,
(3) Development of characterization methods for coated conductors and of a method suitable for testing of long-term stability, and
(4) Development of reliable filamentarization, conductor joining and repair processes for coated conductors.

One of the achievements is a reel-to-reel filamentarization (striation) process for coated conductors. It is very important to filamentarize the coated conductor for the reduction of AC losses. By developing the striation process consisting of laser scribing and chemical etching it has become possible to filamentarize a long-length wire. Figure 30 shows an optical photograph of 30 m-long and 5 mm-wide coated conductors with three filaments fabricated by this process.

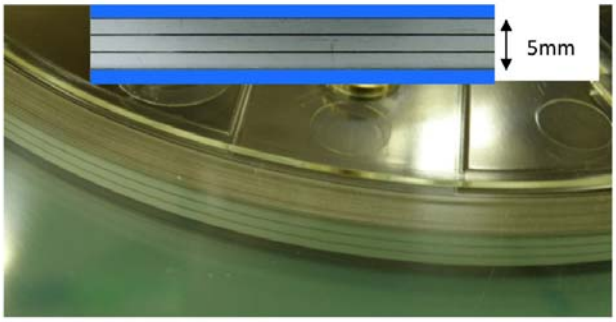


Fig.30. Filamentarized wire on a reel and its magnified picture (upper inset).

Another important technology for the coated conductor is to join two conductors or to repair a defective region of the conductor. The repairing technology has been developed [18]. Figure 31 shows a schematic illustration of the experiment (upper drawing) and experimental results (lower plot). After measuring the I_c, a coated conductor with a silver top layer was scratched and the I_c was measured again. A piece of coated conductor was spliced on the scratched part, and the coated conductor with a splice was annealed at the predetermined temperature for several minutes. The purpose of annealing is to diffuse a vacant lattice on the surface of the splice into the coated conductor. Lastly I_c was measured. It can be seen in Figure 31 that I_c recovers to almost the initial value, although a slight resistance (in this case on the order of 0.01 Ω) is added in series. This technology is very important for the connection and repairing of coated conductors.

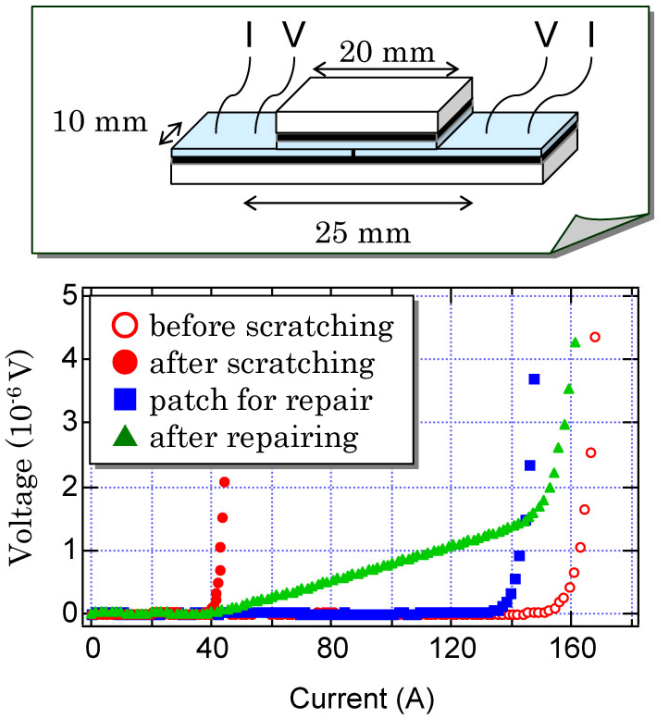


Fig.31. Experimental setup (upper) and measured current-voltage (*I*-*V*) characteristics.

V. CONCLUDING REMARKS

The current organization of ISTEC and activities of SRL have been reviewed. In the past several years, technology development at SRL/ISTEC has progressed remarkably for coated conductors and electronic devices. Recent achievements are directly aiming at practical applications. Indeed, key technologies have been already developed for coated conductors and electronic devices thus enabling the development of prototype systems. Although other important issues, such as reliability and cost reduction, must still be improved, these issues will be addressed and solved with other problems arising from the development and field testing, *etc*., of prototypes.

One can argue that the superconducting wire technology at ISTEC and collaborating companies is now ready to jump over the "Death Valley" by applying the coated conductors to various prototype systems. This "Death Valley" consists of the difficulty to realize a prototype in order to demonstrate the excellence of basic idea. The device technology is also ready for HTS SQUID systems and LTS high-speed measurement systems. The current status gives us a premonition of an approaching big dawn of superconductivity technology to be applied for human welfare by solving environmental and energy problems.

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