Recent Progress in Superconductive Digital Electronics

Part II - Japanese Contributions

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***Abstract* – This overview (Part II) contains highlights of articles contributed by Japanese authors to the Special Section of IEICE Transactions on Electronics, vol. E91-C (March 2008). We focus on the project developments performed by several research groups in Japan under projects sponsored by NEDO. A new generation of RSFQ related research projects was launched there in 2006/07. Very important steps towards the future application of RSFQ circuits were; (a) the demonstration of cryocooled systems with high-speed I/O interface and MCM carrier in the past network project, and (b) the wideband hybrid ADC system. The design capabilities demonstrated with the CORE1 microprocessor are developed to a VLSI level and demonstrate the transition from analog circuit design towards automatic integrated circuit design based on hardware description languages.**

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I. INTRODUCTION

The Japanese New Energy and Industrial Technology Development Organization (NEDO) managed the past network projects for both LTS and HTS technology. One small part of the Superconductor Network Device Project was the development of a high-T_c fabrication process based on ramp-edge Josephson junctions with interface-modified barriers. The aim of this technology development described by K. Tanabe *et al.* in [1] was the subsequent demonstration of their performance in small-scale circuits (less than 100 junctions) with compact cryocoolers. Examples of such circuits were elements of analog-to digital converters, and a sampler incorporated into a desk-top compact system.

The central Japanese fabrication process is the niobium-based "Standard Process" (SDP) characterized by the Josephson junction critical current density of 2.5 kA/cm², which was developed and improved during the project completed in 2007. Wafers were fabricated routinely at the International Superconductivity Technology Center (ISTEC) in Tsukuba, Japan. The ISTEC designers as well as the collaborators at Nagoya University, Yokohama National University and the National Institute of Information and Communication Technology developed and tested a mature cell library for this process, with over 200 different cells included. Within the new, current term of superconducting digital electronics (SDE) project funding in Japan, all projects utilize exclusively the niobium technology and

focus on the improvement of VLSI design capabilities for complex general-purpose digital computation systems and high-speed optical and electrical data switches.

II. FABRICATION PROCESS

During the last few years, the ISTEC foundry at NEC fabricated about ten wafers per month using SDP. An automatic probe system enables the control of process parameters during the fabrication process by testing various room-temperature device properties on each chip. Independent of the monitoring of physical parameters during the production process, an extensive digital testing of elementary logic gates and 80-bit shift registers has been performed at ISTEC foundry for every wafer since May 2006. If one of the proven circuits with up to 1800 Josephson junctions shows a false operation, it is a clear sign for a process defect. The review article by M. Hidaka *et al*. [2] gives a detailed overview of the process yield and its statistical improvement in time.

The SDP is characterized by 4 niobium layers, one for ground plane, two wiring layers for base and top electrode of Josephson tunnel junctions and a fourth electrode for wiring and shielding purposes. The most complex circuit designed and fabricated using this process is the CORE1γ microprocessor with 22.302 Josephson junctions [3]. The statistical process defect rate is about one defect junction per 10.000, which leads to the current limitation in the circuit complexity. This junction yield seems to be a universal feature of the present Nb-Al_2O_3 fabrication process.

From the design point of view, the most important improvement was the consequent implementation of bias line shielding. It was the key to enabling complex circuits such as CORE1γ, with large, about 3 ampere, supply current. The circuit complexity was reduced by the wide application of passive transmission lines (PTL) for on-chip interconnects.

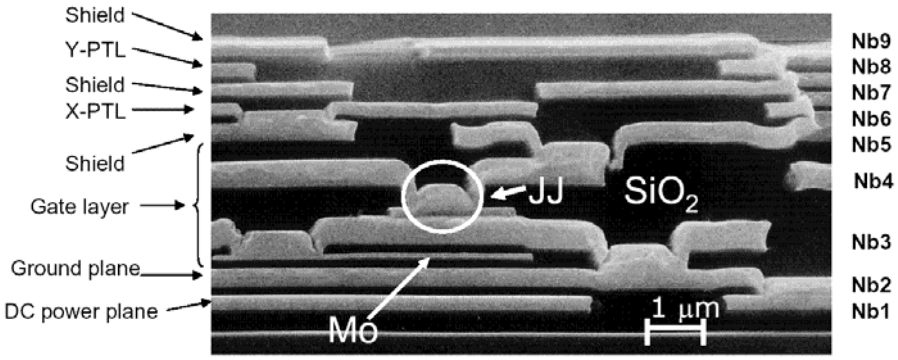

Fig. 1. Cross section of the advanced fabrication process as described in [2]. Beside the four layers from the standard process (Nb2 - bottom ground plane, Nb3 - base electrode, Nb4 - counter electrode, Nb5 – top ground plane), the layer package includes additional layers for dc power supply and for strip-line interconnects in both x- and y-direction (photo - courtesy of M. Hidaka).

During the last 5 years, the advanced fabrication process (ADP) with a Josephson junction critical current density of 10 kA/cm² has been developed in parallel to the SDP. The targets of the process development were additional niobium layers and a higher integration density. The key improvement allowing introduction of these additional layers was the newly developed *Caldera* planarization method [4]. The ADP allows 9 Nb layers with special assignment for shielding and for passive interconnects in x- and y-direction. Some test circuits were designed for the ADP and the process was demonstrated to be suitable for small circuits (an 8-bit shift register) operating up to 120 GHz [5]. The ADP is the technology base for the new Japanese projects and is still under development. As soon as the layer assignments and process parameters are fixed, the *Connect* cell library will be transferred from the SDP to the ADP.

III. SYSTEM INTEGRATION

For a few years, the first RSFQ electronic demonstration systems have been operated in a cryocooled environment provided by a 1 W Gifford/McMahon cryocooler (Sumitomo RDK 408D). The packaging demonstrated by Y. Hashimoto *et al*. [6] is a very flexible high-speed set up with 32 I/O lines. The demonstration vehicles were (1) a 4:1 multiplexer and 1:4 demultiplexer, and (2) a 2 x 2 switch system. One possible solution to overcome the defect density mentioned above as well as the problems with bias currents larger than a few amperes was the introduction of multi-chip-module (MCM) technique. The high-speed MCM interconnects as well as the low bit-error-rate room temperature data link have been demonstrated for a speed up to 12 gigabit per second (Gbps), per channel. The whole switch system operated correctly up to 47 Gbps.

A special superconductive voltage driver consisting of a dc-biased 16 SQUID stack connected to a cryogenic GaAs amplifier was the key circuit for high-speed communication between RSFQ and room-temperature electronics. While these special cryogenic semiconductor amplifiers were used for the demonstration of the 2 x 2 network switch, all data I/O lines could be handled with commercial microwave equipment.

For optical input interfaces InP/InGaAs photodiodes were used. As a further improvement, the interface will utilize metal-semiconductor-metal diodes (MSM, already demonstrated by others) for the generation of the input signals. Optical output interfaces are much more difficult since the output energy of SFQ circuits is not high enough for driving optical diodes directly. This is still an unsolved problem, which requires a technological breakthrough.

IV. NETWORK SWITCH

The demonstrator for the past network project in Japan was the 4x4 SFQ network switch described by Y. Kameda *et al*. in [7]. Its successful demonstration was made possible by the very high-quality fabrication process as well as by the above mentioned MCM concept for packaging superconducting electronics. The demonstrated network switch consists of a MCM module with a switch chip fabricated in the SDP and a special voltage driver chip fabricated in the same process, but with critical current density increased to 10 kA/cm². Each chip comprises about 2.200 Josephson junctions and requires about 0.6 mW electrical power. With this system demonstration, the ISTEC group could also demonstrate the connectivity between RSFQ circuitry and commercial electronic devices.

The group implemented a four-port Ethernet switch connected to four commercial personal computers forming a local area network. This prototype was the base for the NEDO Optical Network project. The expected main application field will be the routing of data in future communication network systems, where the expected bottleneck will be the data throughput between different nodes. Another possible application field for such routers could be the back-end of high-performance multi-CPU supercomputers, such as the new “Roadrunner” with 16.000 CPUs [8].

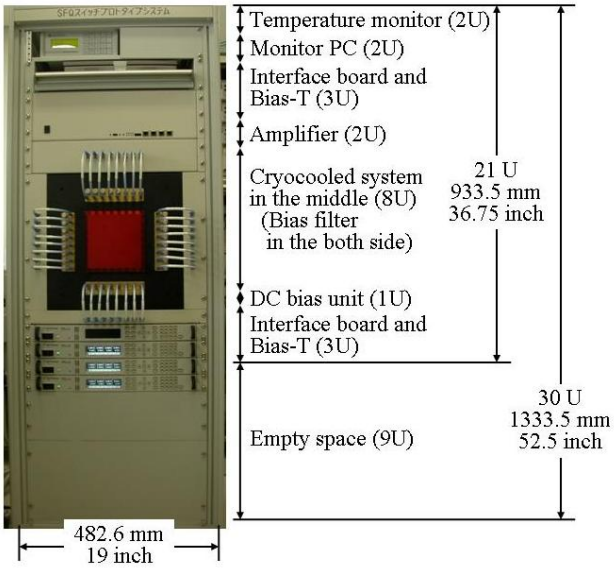

Fig. 2. The cryocooled network switch installed in a 19 inch rack (photo – courtesy of Y. Kameda).

V. MICROPROCESSOR

Since the first overview article on RSFQ [9], the goal was the exploitation of the ultra-high switching speed for high-performance computing. The development of the CORE microprocessor in Japan is a study towards a general-purpose computing system based on RSFQ electronics. All the best technologies concerning SFQ integrated circuits have been assembled and the worldwide most advanced design environment was established to allow the cell-based HDL design of a CPU described by A. Fujimaki *et al.* in [3]. On-chip high-speed tests of all the components of the processor showed relatively large margins. Unfortunately, these margins did not overlap so that the demonstration test of the whole processor was not yet possible.

The high-speed nature of RSFQ circuits is used in the CORE1 microprocessor for reducing the circuit complexity. The bit-serial architecture allows a very compact implementation of the arithmetic logic unit and reduces the number of interconnects. A microprocessor design is one of the most complex tasks for circuit designers and, in our opinion, the most important Japanese development in this sense is the capability of Yokohama National University and Nagoya University to be able to design any complex digital SFQ systems very fast. The complete design and cell placement process for the CORE1 can be performed in less than three weeks.

The new microprocessor project is based on the reconfigurable data path (RDP) concept to allow ultra-fast pipelined computation based on a hardware grid of arithmetic logic units and an intelligent control circuit. Integer and floating point units as well as switching nodes are the current key issues for the implementation of a first demonstrator. If such a concept, proposed by N. Takagi et al. in [10], will become very complex, the development of large MCM will be the key issue to reach the target of 10 TFLOPS with a total junction count of 650 million on 128 chips and a total power consumption of 7.7 Watts. This cooling power is still available with refrigerators with an input power of approximately 8 kW. The RDP microprocessor project points in the direction of high-performance computing and will address tasks similar to those proposed by the Superconducting Technology Assessment of National Security Agency (NSA) in the US [11]. The proposed concept uses the unique feature of ultra-high throughput in SFQ circuits and, therefore, does not require high-speed memories.

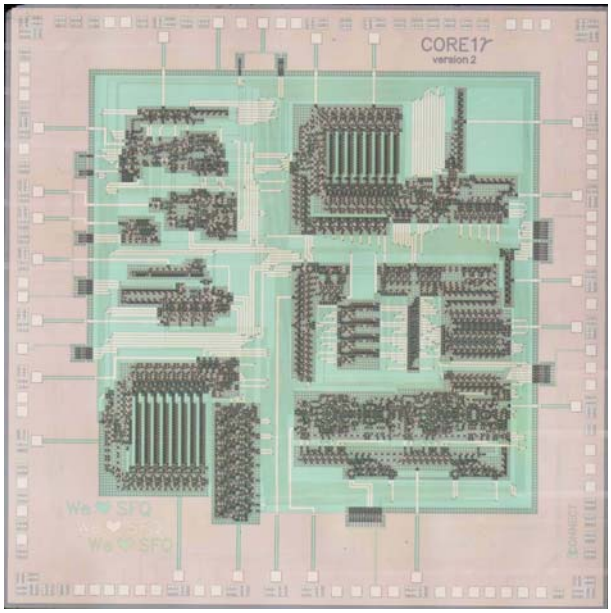

Fig. 3. Photograph of the 8 bit serial microprocessor Core1γ (photo - courtesy of A. Fujimaki).

VI. ANALOG-TO-DIGITAL CONVERTER

The utilization of RSFQ electronics for ultra fast, low-noise and low-power consumption analog-to-digital converters (ADC) has been proposed by Likharev and Semenov already in the early days of this technique [9]. Superconductor ADC systems are typically based on an over-sampling sigma-delta converter scheme utilizing a Josephson comparator connected to an integrating *RL* circuit. The complete system demonstration reported by F. Furuta *et al*. in [12] is an excellent example for such a high-throughput real-time ADC system. The interface concept developed for this system provides 4 channels with 5 Gbps per channel. After a 4-to-64 demultiplexer, the 64 bit parallel data streams at a frequency of 313 MHz are fed into a DSP based decimation-filter. This ADC could demonstrate a bandwidth of 9.1 MHz and 13.8 bit resolution, in which the-post processing exceeds the limits of state-of-the-art CMOS electronics. This architecture, developed by Hitachi Ltd., ISTEC-SRL and Yokohama National University focused on the reduction of the number of Josephson junctions in the front-end circuit to only 490. Exploiting the experience of ISTEC-SRL in superconducting amplifiers for high-speed digital interfaces, a 4-channel interlink with 20 Gbps has been successfully implemented into the system. The next generation communication systems require ADCs with a bandwidth of 500 MHz in the baseband or in the 10-30 GHz carrier frequency range. This specification imposes an output sampling rate of 1 Gsample per second with 10-14 bit resolution. This total data throughput of 14 Gbps implies the application of on-chip RSFQ decimation filters, to meet future targets of software-defined radio.

VII. CONCLUSION FROM THE EUROPEAN VIEWPOINT

In recent years, the progress attained by Japanese groups in fabrication technology and circuit design for superconducting electronics has been very impressive, indeed. The capability to solve all technical issues has been demonstrated thus opening the age of engineering quantum electronics to blossom in the near future. Japanese colleagues succeeded in the transfer from physics-oriented research to engineering of applicable single flux quantum electronics. The availability of the worldwide most advanced foundry process for digital superconducting

electronics, and the mature level of a digital cell library were essential for all the recent circuit demonstrations in Japan. Besides ISTEC foundry at NEC in Tsukuba, Japan, there are only two other active SDE foundries worldwide, namely that of HYPRES Inc. [13] in Elmsford, U.S.A. and the FLUXONICS Foundry [14] at IPHT in Jena, Germany. Within the new research project in Japan, the development of circuit architecture is turned towards applications which may benefit the most from the ultra-high throughput and the intrinsic quantum accuracy in counting digital flux quanta.

The European SDE activities enjoy only a modest support. The most prominent of European project has been that on baseband digital signal processing highlighted in Part I of the overview of the IEICE Special Section on progress in SDE. The aim of the new European project S-PULSE [15] is to monitor all developments in this field and to make the technology accessible to researchers and industries potentially interested in the application of RSFQ and capable of developing the enabling non-superconducting technologies.

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