Opto-electrical Data Transfer from Room Temperature to 4K for Superconducting Quantum Computing

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Outline

- **Introduction**
- **Link Architecture**
- **Prototype Implementation**
  - Analog Front-End
  - CPLD-based CDR
  - Qubit Controller ASIC
- **Measurement Results**
- **Conclusions & Future work**

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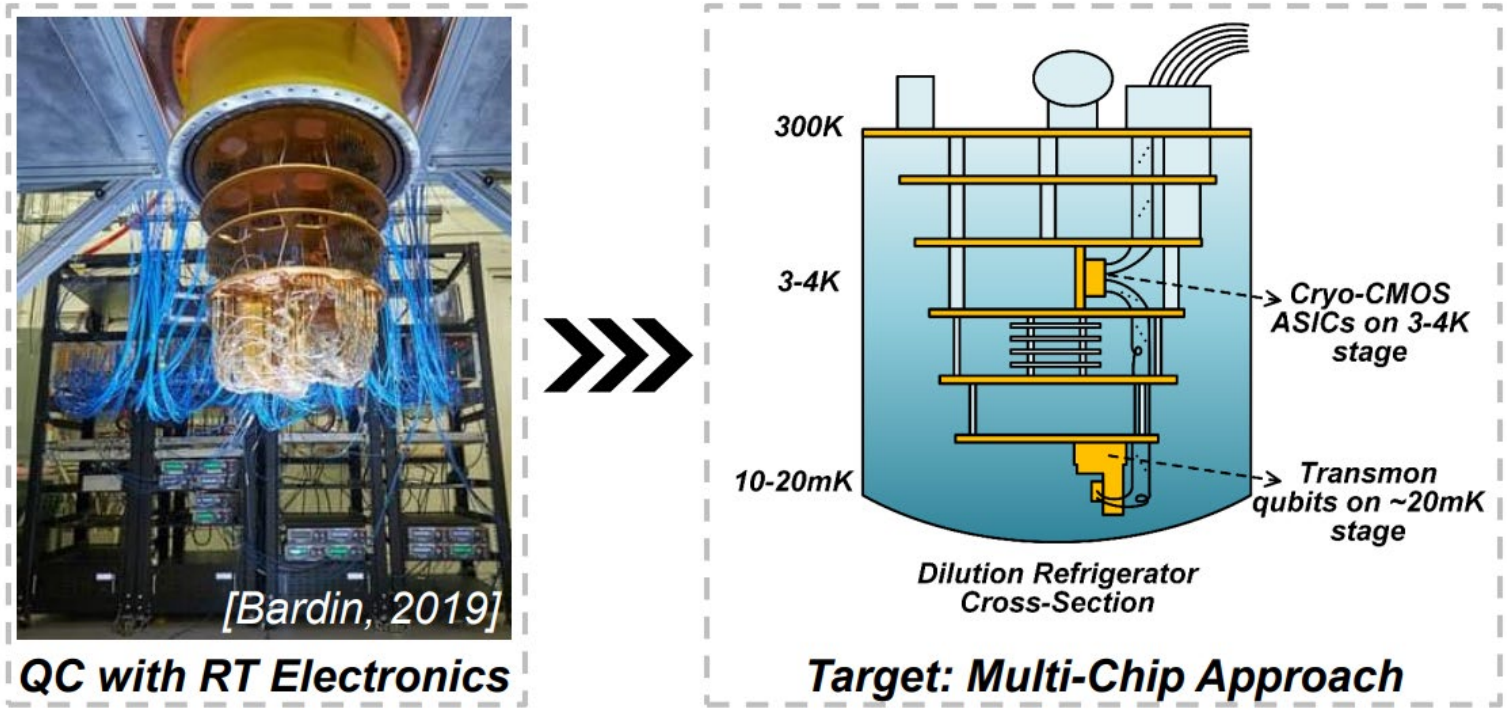
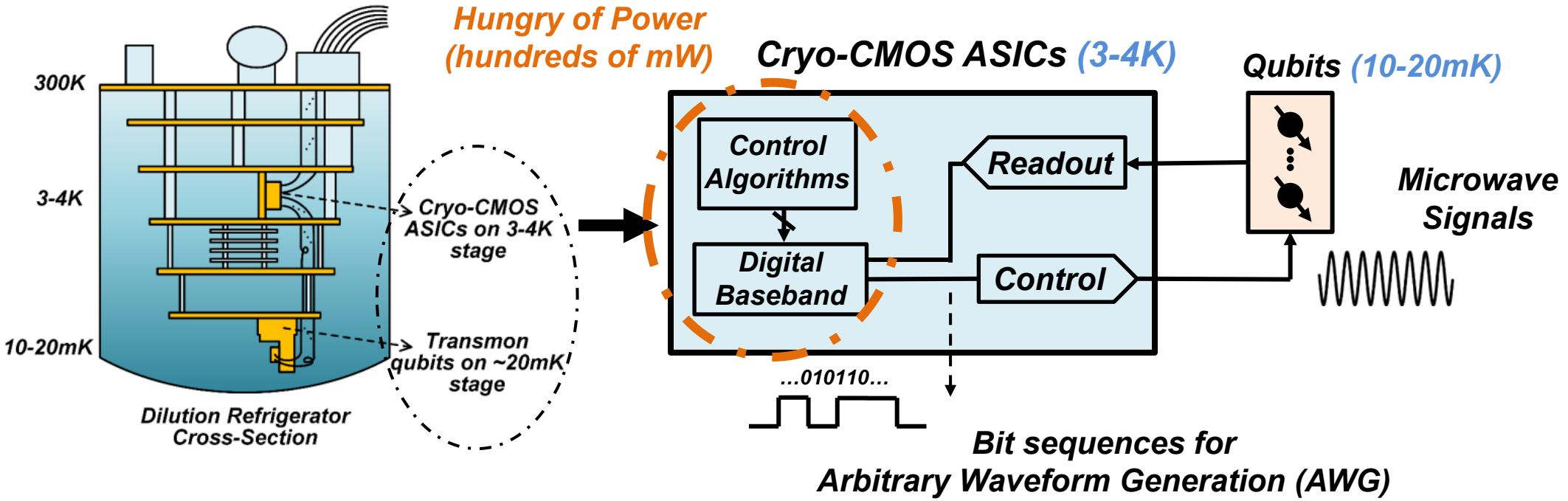
Cryo-CMOS ASICs Speed Up Large-Scale QC



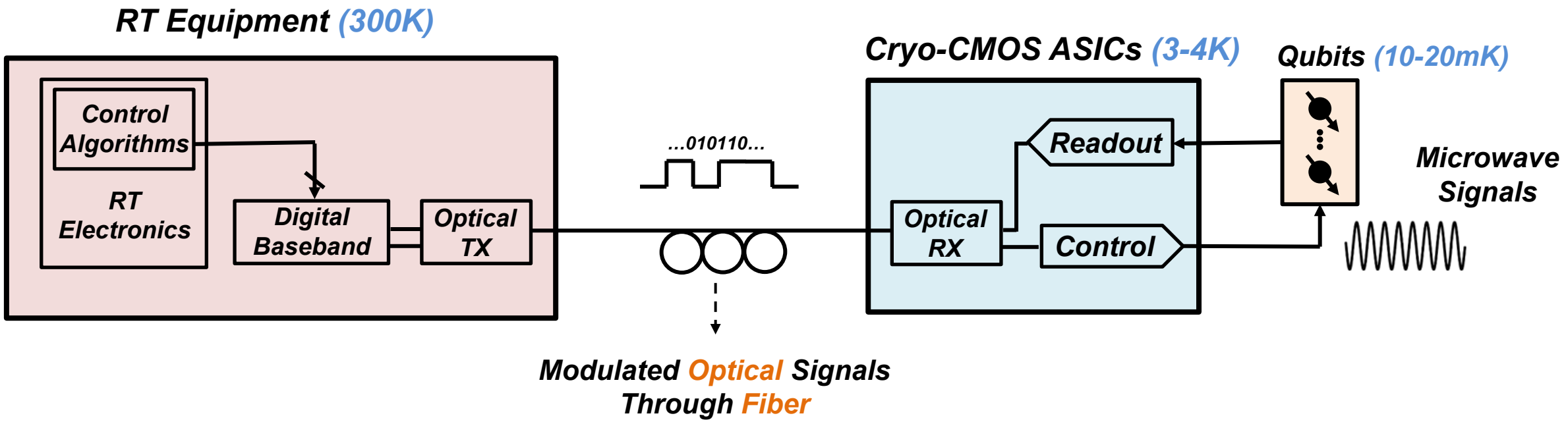
- **Cryo-CMOS interface circuits at 3-4K for quantum computing**
  - Avoiding huge amounts of cables between qubit devices and 300K
  - Scaling down of the size of QC platform

Need of Data Links between 300K and 3-4K



- **Data Transfer between 300K and 3-4K**
  - Data are required for AWG for real-time control microwave generation
  - Digital logic and baseband (BB) consume huge power and are preferred to be place at 300K → **Need of data links between 300K and 3-4K**

Proposed 300K-to-4K Opto-Electrical Data Link



- **Features:**
  - **More power budget** for ASICs at 4K
  - Compared with electrical link based on coaxial cables
    → **Better thermal isolation & Higher energy efficiency**

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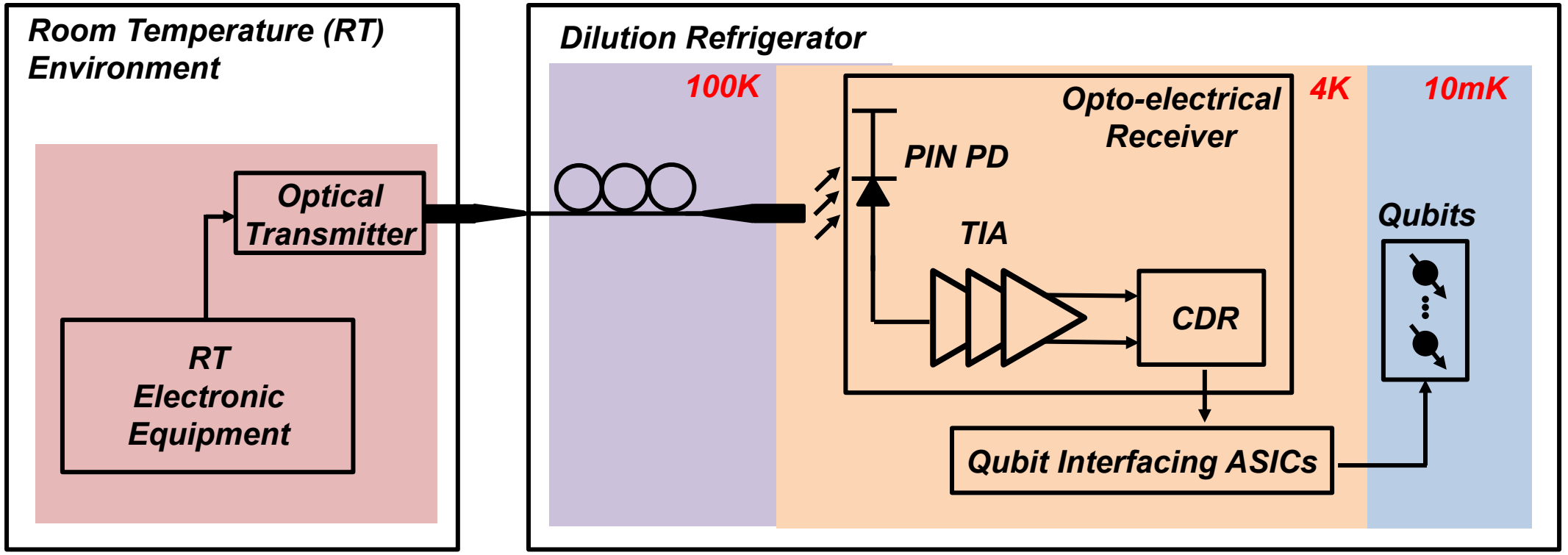
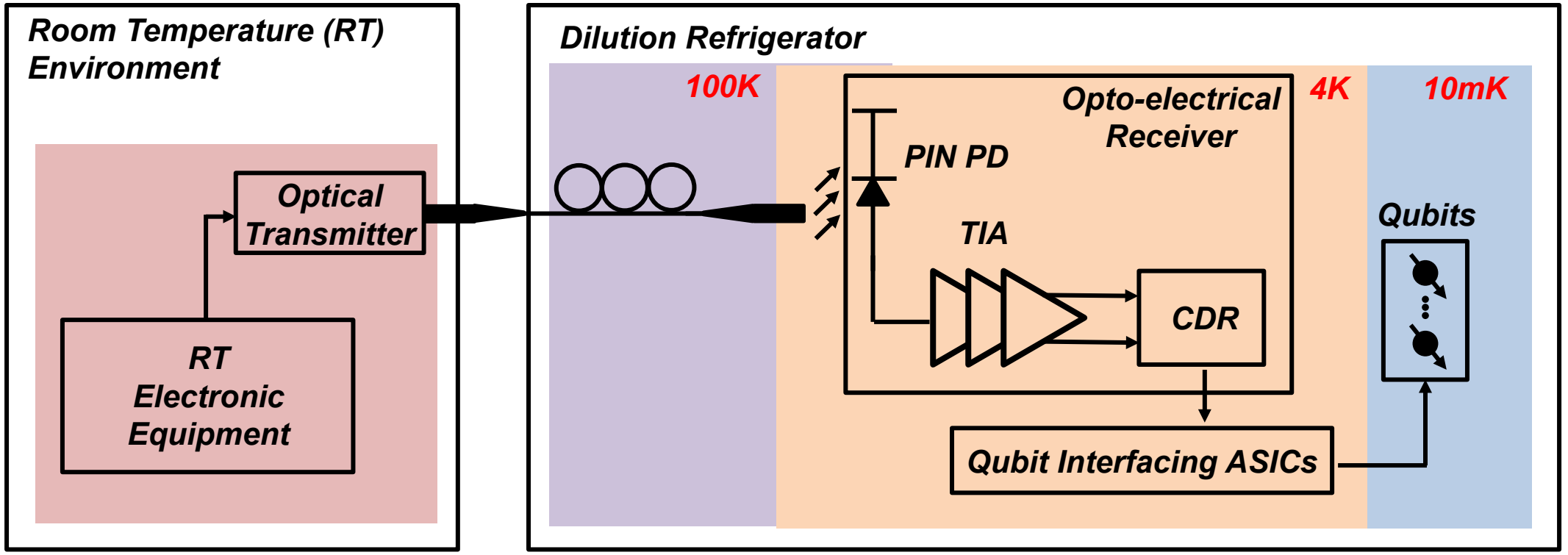
Link Architecture



- Modulated optical signal is sent from RT to 4K through a fiber
- Opto-electrical receiver at 4K followed by qubit interfacing ASICs

Link Architecture



- **Opto-electrical receiver at 4K followed by qubit interfacing ASICs**
  - A photodetector (PD)
  - A transimpedance amplifier (TIA)
  - A clock-data-recovery (CDR)

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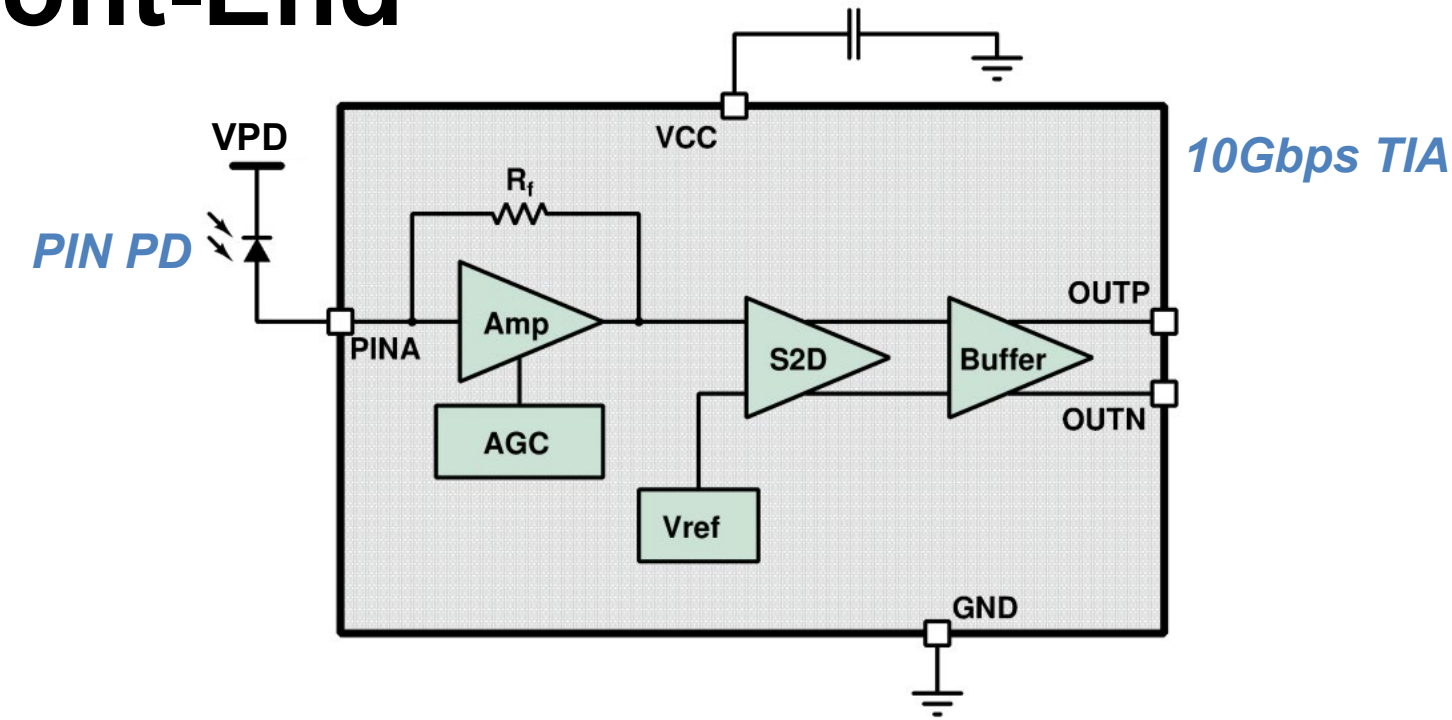
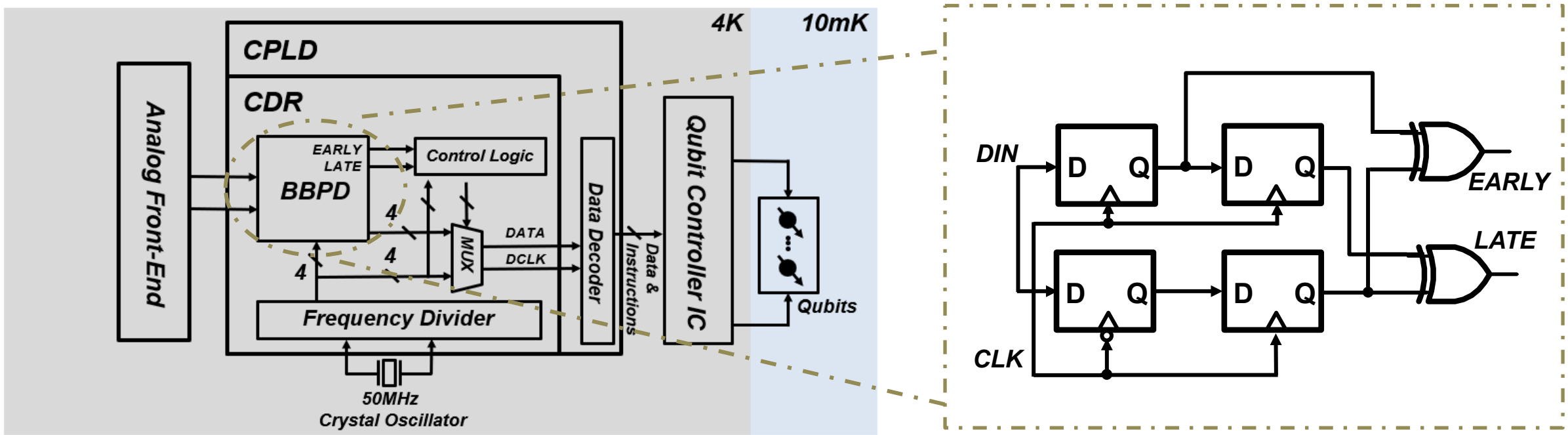
Analog Front-End



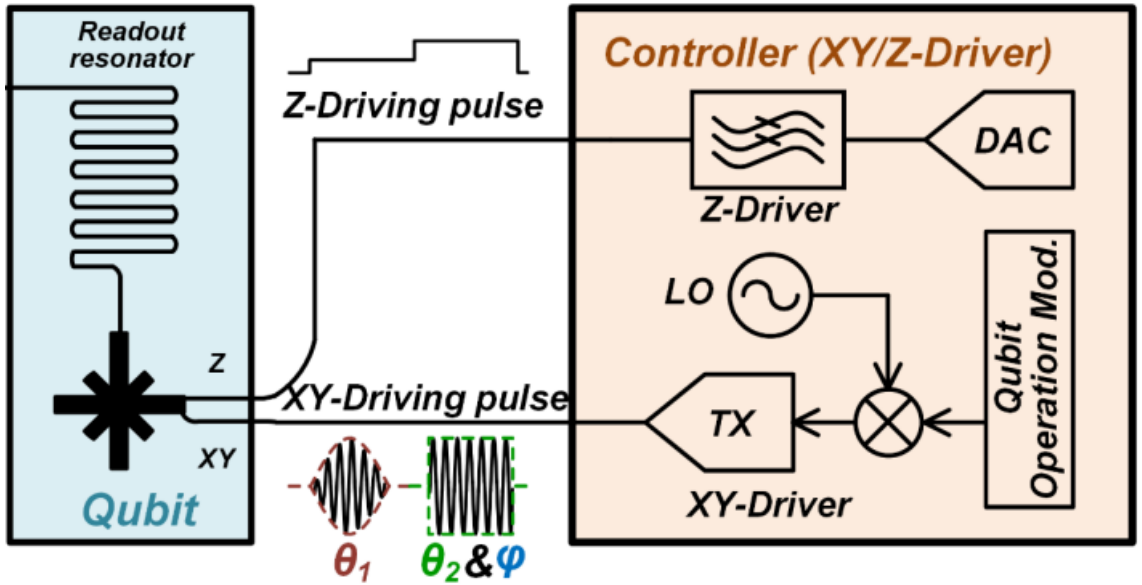
- **An off-the-shelf 10G PIN PD**
- **A monolithic 10Gbps TIA manufactured by Siboard Inc.**
  - An amplifier with auto gain control (AGC) circuits
  - A single-to-differential (S2D) amplifier
  - An output buffer for better drive capacity

CPLD-based CDR



- Based on 4-phase **12.5MHz** clock signals divided from a **50MHz** oscillator
- A Bang-Bang Phase Detector to figure out if the clock is **Early** or **Late**
- A control logic to decide whether to switch the clock
- A 4-1 multiplexer to selects the correct clock and data signals
- A data decoder to decode control bits for AWG from data bag

Qubit Controller ASIC *(Prior work)*



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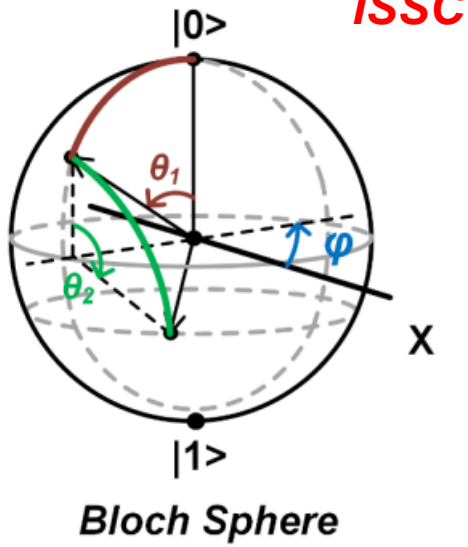

- **Transmon qubit controller ASIC in our prior work**
  - XY-Driver & Z-driver
  - Center frequency of XY-driving pulse = Qubit frequency f_q
  - Pulse energy (amplitude × duration) ∝ Qubit Phase rotation θ
  - Pulse phase ∝ Qubit axis rotation φ

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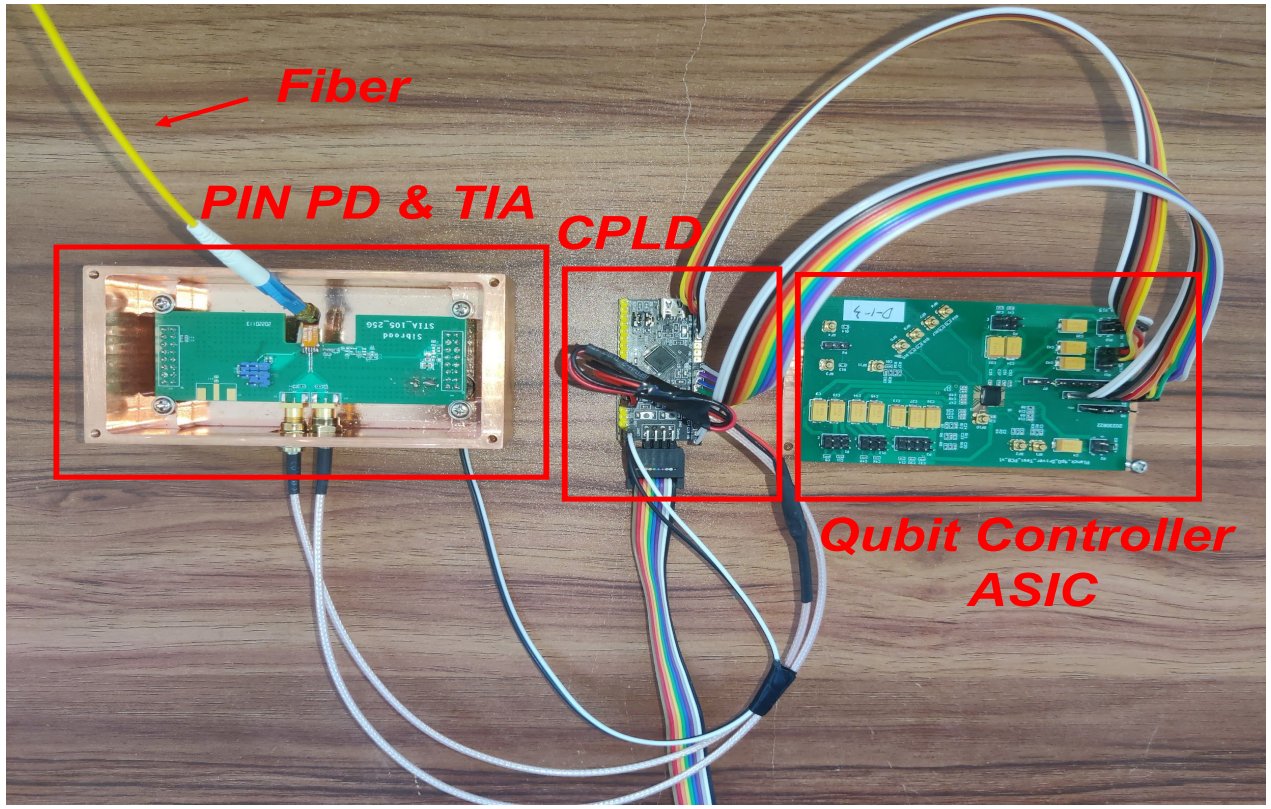
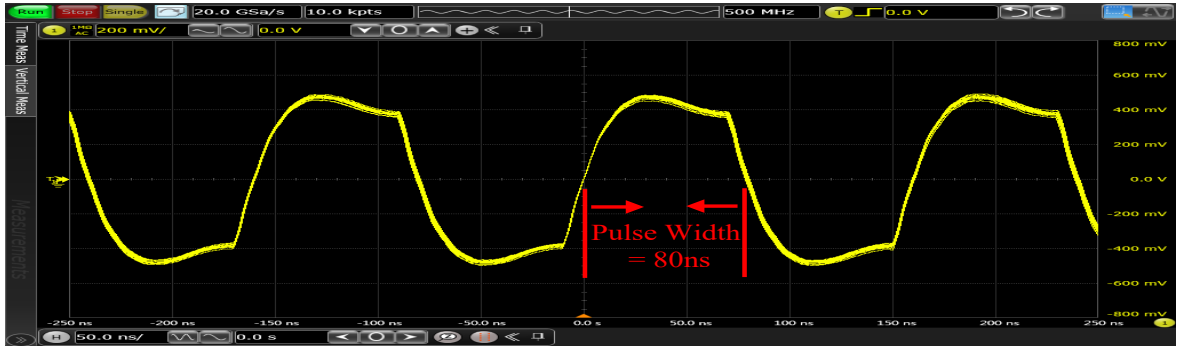
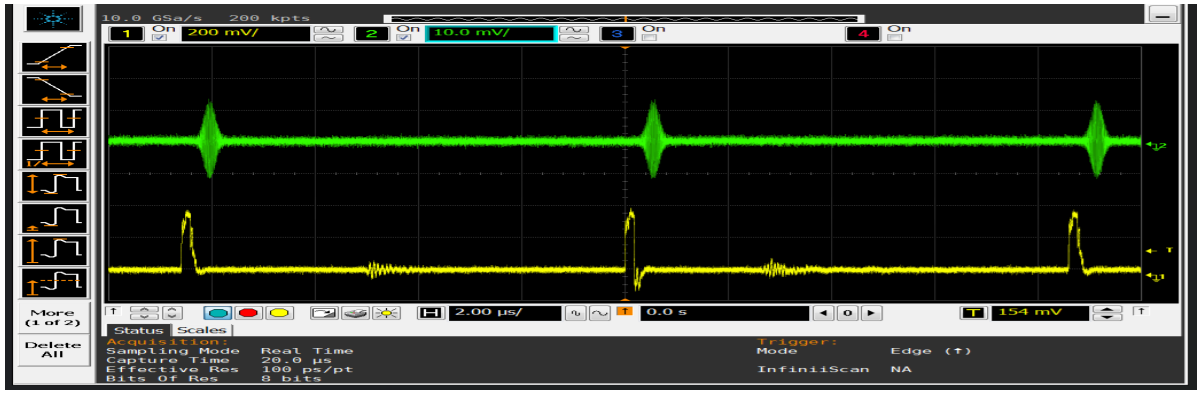
Prototype Photo and Measurement Setup



- The prototype link has been tested at the 4K temperature plate within a dilution refrigerator (DR)

Measurement Results





TIA output waveform

- Input optical power = -5dBm
- Measured Voltage amplitude is 1Vpp
- Pulse width = 80ns

CDR output waveform

- High Threshold BBPD → low jitter
- Crystal oscillator's frequency is 50MHz
- Data recovered at 12.5Mbps

Qubit control pulse

- Measured output of qubit controller ASIC
- XY-Driving pulse (Green) and trigger pulse (yellow) generated based on instructions from 300K

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Conclusions & Future Work

- **We propose a novel link for data transfer from RT to 4K**
  - An **opto-electrical** data link based on a single fiber and a cryo-receiver
  - Capable of data transfer for AWG required for superconducting QC
  - **Avoiding the heat-conduction effect** associated with coaxial cables

- **Validated by a prototype cryogenic opto-electrical receiver**
  - Demonstrated data speed of 12.5Mbps from RT to DR's 4K plate
  - Data link speed is limited by IO speed of CPLD

- **Future work: Replace CPLD-based CDR with a CDR ASIC**
  - Capable of **tens of Gbps** data link speed

Acknowledgement

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  - Associate Researcher Tiefu Li, (litf@tsinghua.edu.cn), School of Integrated Circuits, Tsinghua University

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Thank you very much for your attention!

Q&A