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Superconducting quantum computing technology roadmap: First cut

D. Scott Holmes
International Roadmap for Devices and Systems (IRDS)
2022-10-27 ASC 4EOr1C-01

Superconducting quantum computing technology roadmap: First cut

Abstract

Superconducting circuits are a promising approach to quantum computing. Both IBM and Google have presented timelines with goals of one million physical superconducting qubits. Key technologies to achieve this goal include physical qubits with sufficiently low error rates, an efficient error-correction scheme, error-corrected logical qubits, and control systems that don't exceed available refrigeration capacity. A roadmap for the key technologies is presented and assessed for feasibility.

Presenter: D. Scott Holmes

Applied Superconductivity Conference

2022 October 24–28, Honolulu, Hawaii, USA
https://www.appliedsuperconductivity.org/asc2022/

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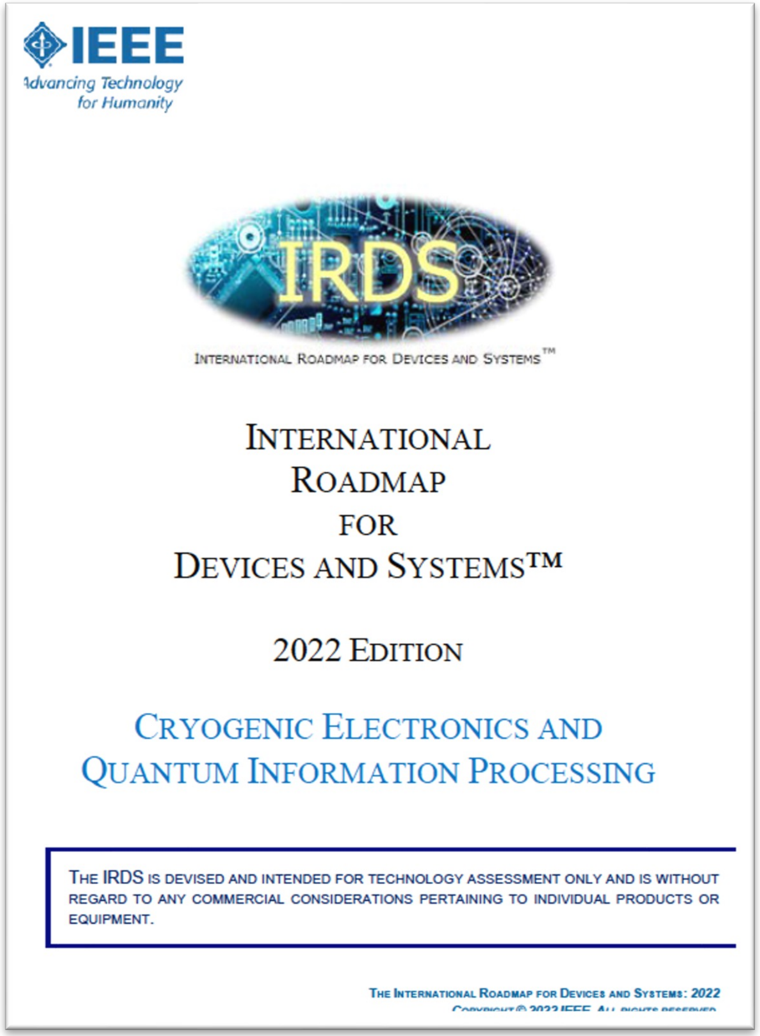
2022 IRDS CEQIP summary

- Coverage
    - Superconductor Electronics (SCE)
    - Cryogenic Semiconductor Electronics
    - Quantum Information Processing (QIP)
- Key Messages from the 2022 report
    - SCE: Partial roadmaps
    - QC: Not yet ready for roadmaps
- Summary slides:
    - Difficult Challenges
    - Technology Requirements
    - Potential Solutions
- Updates
    - New Technology Requirements
    - Breakthroughs in Technology, Research
    - New Disruptors
    - Potential Solutions
- Conclusions and Recommendations

Available:
https://irds.ieee.org/editions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IRDS
INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

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2022 EDITION

CRYOGENIC ELECTRONICS AND QUANTUM INFORMATION PROCESSING

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THE INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS: 2022

2023 CEQIP Members

Name	Area	Organization	Region
Byun, Ilkwon	Cryo-Semi, QIP-QC	Seoul National University, Korea	Asia
Cuthbert, Michael	Cryo, QIP	National Quantum Computing Centre, UK	Europe
DeBenedictis, Erik	QIP-QC	Zettaflops, USA	Americas
Fagaly, Bob	SCE-App	Honeywell (retired), USA	Americas
Fagas, Giorgios	QIP	Tyndall National Institute, Ireland	Europe
Febvre, Pascal	SCE-Fab	Université Savoie Mont Blanc, France	Europe
Filippov, Timur	SCE-Log	Hypres, USA	Americas
Fourie, Coenrad	SCE-EDA	Stellenbosch University, South Africa	Africa
Frank, Mike	SCE-Log, -Rmap	Sandia National Laboratories, USA	Americas
Gupta, Deep	SCE, Cryo-Semi	SEACORP, USA	Americas
Herr, Anna	SCE-Logic, -Rmap	IMEC, Belgium	Europe
Holmes, D Scott [Chair]	SCE, Cryo-Semi, QIP	Booz Allen Hamilton, USA	Americas
Humble, Travis	QIP-QC	Oak Ridge National Laboratory, USA	Americas
Leese de Escobar, Anna	SCE-App, -Bench	Navy NIWC-PAC, USA (retired)	Americas
Min, Dongmoon	Cryo-Semi, QIP-QC	Seoul National University, Korea	Asia
Mueller, Peter	QIP-QC-SC	IBM Zürich, Switzerland	Europe
Mukhanov, Oleg	QIP-QC, SCE-Log	Seeqc, USA	Americas
Nemoto, Kae	QIP	The National Institute of Informatics (NII), Japan	Asia
Papa Rao, Satyavolu	SCE-Fab, QIP	SUNY Polytechnic, USA	Americas
Pelucchi, Emanuele	QIP-QC	Tyndall National Institute, Ireland	Europe
Plourde, Britton	QIP	Syracuse University, USA	Americas
Soloviev, Igor	SCE	Lomonosov Moscow State University, Russia	Europe
Tzimpragos, George	SCE-Logic, -Metrics, -Rmap	University of Michigan, USA	Americas
Vogelsang, Thomas	Cryo-Semi	Rambus, Inc., USA	Americas
Weides, Martin	SCE, QIP	University of Glasgow, UK	Europe
Yoshikawa, Noboyuki	SCE-Log, -Bench	Yokohama National University, Japan	Asia
You, Lixing	SCE	SIMIT, CAS, China	Asia

Additions for 2023

13: Americas
9: Europe + Africa
5: Asia

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2022 Report: Quantum Information Processing (QIP)

2022 Difficult Challenges (Near-term) for QC

Technology roadblocks, gaps, and possible disconnects within the roadmap

Near-Term Challenges: 2022–2029	*Summary of Issues (why is it a challenge?)*
Physical qubits	• Design and fabrication of qubit devices with enhanced qubit coherence times and gate fidelities
Logical qubits	• Implementation of fully error-corrected logical qubits and protected gate operations
Readout of qubits	• Development of scalable, cryogenic qubit readout hardware
Interconnects, cryogenic to room temperature	• Development of low thermal conductance and high bandwidth interconnects between different temperature stages of cryogenic- and room-temperature electronics
Control electronics	• Location close to the qubits has the lowest latency but too close can disturb the qubits. Operating environments close to the qubits can be challenging (e.g., cryogenic, high vacuum).

- We still don't know how to build a full-scale quantum computer.

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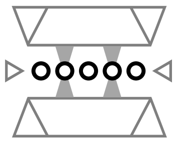
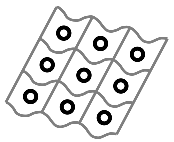
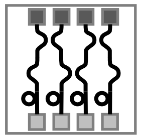
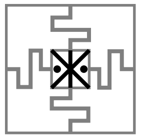
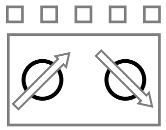
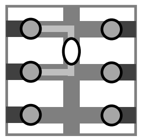
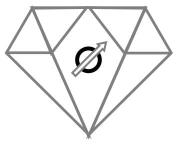
Quantum computing: Still a race with several contenders

	Natural qubits			Synthetic qubits			
							
Qubit:	**Trapped ion**	**Neutral atom**	**Photonic**	**Superconducting**	**Quantum dot**	**Topological**	**N-V diamond**
Basis	Electron spin of ionized atoms	Internal states of atoms trapped in an optical lattice	Optical photons in waveguides	Nonlinear oscillator circuits containing Josephson junctions	Impurity dopants in a semiconductor	Majorana particles in nanowires	Spin state of N atom + vacancy defect in diamond
$E_{transition}$ (= hf, $k_B T$)	1 – 700 THz 50 – 30,000 K	~ 4 MHz ~ 200 μK	100 – 200 THz 4,800+ K	2 – 10 GHz 0.1 – 0.5 K	10 – 50 GHz 0.5 – 2.5 K	?	300 – 800 THz 15,000+ K
T_{system}	1 – 300 K	4 – 300 K	1 – 300 K	0.01 – 0.05 K	0.1 – 1 K	?	1 – 300 K
Pros	Long lifetime, low gate error	Many qubits, 2D, maybe 3D	Linear optical gates, photonic IC	Fast gates, adjustable, easy fabrication size	High density, CMOS compatible	Lower errors	Room temperature operation?
Cons	Slow gates, vacuum, many lasers	Hard to control individual qubits, noise, high errors	Superconducting single photon detectors	T noise, variability, large size, mK temperatures	T noise, low temperatures, high errors	Device? Magnetic field?	Variability, detector?

System temperatures vary by approach

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Gate-Based Quantum Computing Status Summary

Early attempt at comparisons

- The overall picture is that no approach has emerged as most likely to scale to the millions of qubits needed.

Qubit type	*Quantum volume*	*Qubit count*	*Qubit connectivity*	*2-qubit gate depth*	*Quantum teleportation*	*Qubit function*	*System scalability*
Superconducting	512	127	3.25	667	0.42 m	fair	fair
Trapped ion	4096	32	10	> 100,000	yes	fair	fair
Quantum dot	—	4	1	104	-	poor–fair	fair–good
Photonic	—	4			1400 km	poor	fair

2022 Table CEQIP-23

Quantum volume metric: https://en.wikipedia.org/wiki/Quantum_volume
2-qubit gate depth: ratio of coherence time divided by 2-qubit gate time (T_2^*/t_{2q})

- Better method needed!

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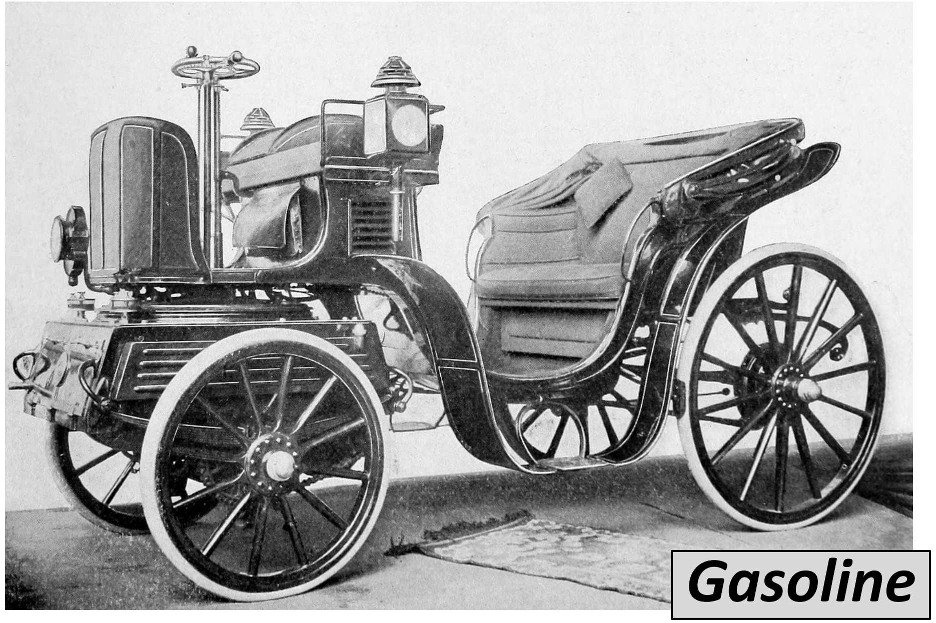
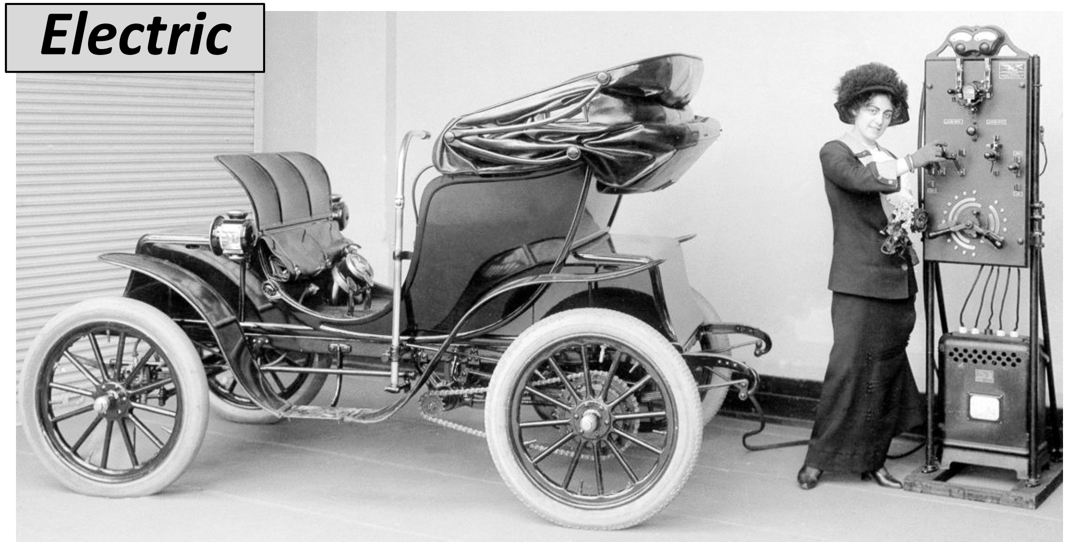
Searching for a winning combination (QC edition)

Automobile analogy, circa 1900



Gasoline

Electric



Steam

- The eventual winner was not obvious at the time.

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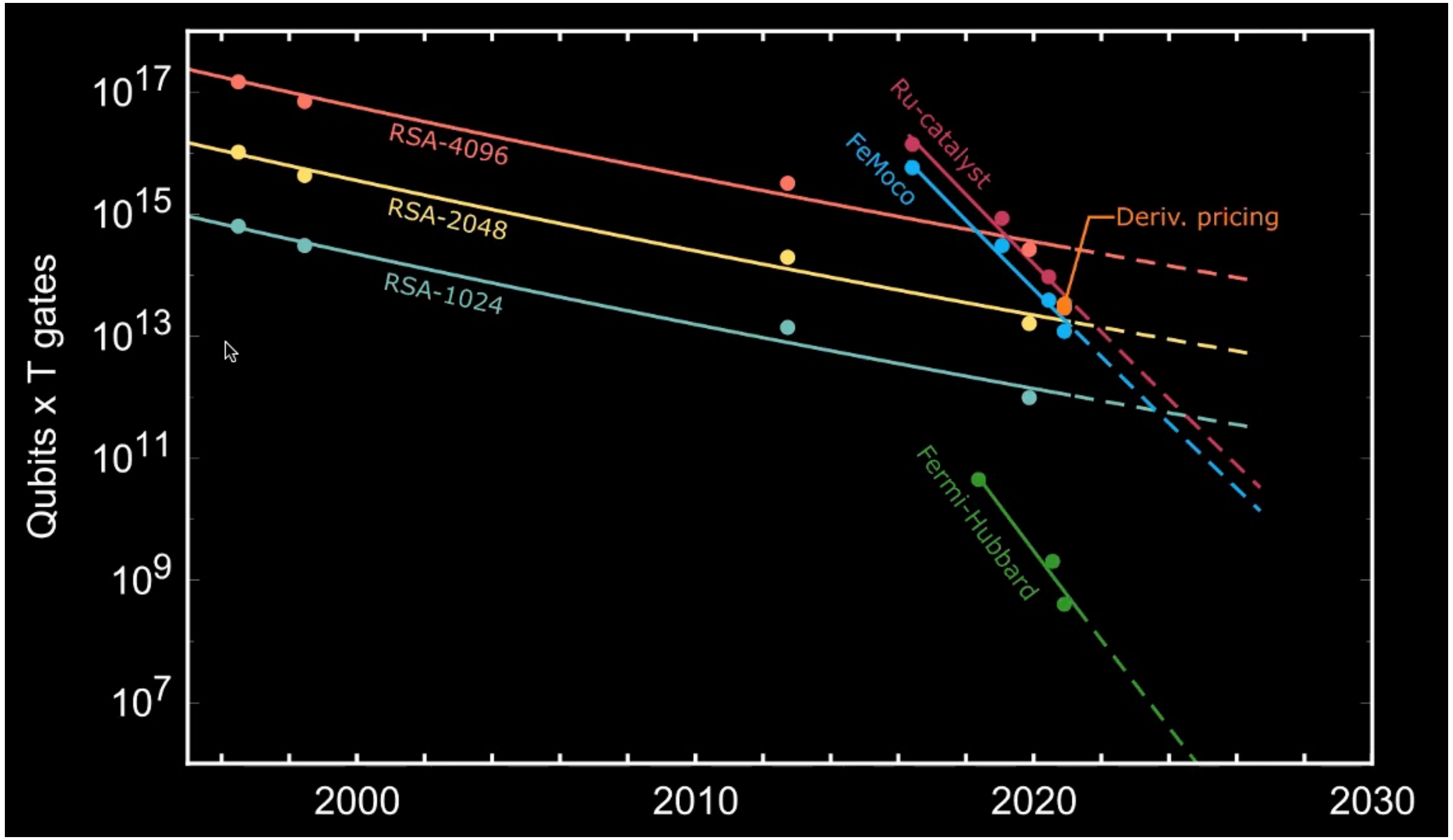
Application Requirements

Billions of quantum gate operations are required for key applications

- **Derivative pricing**: Financial market pricing of options
- **FeMoco**: Find the complex chemical process behind nitrogen fixation
- **Fermi-Hubbard**: model for strongly-correlated electronic systems
- **RSA**: Breaking RSA encryption (Rivest–Shamir–Adleman) with the indicated number of bits
- **Ru-catalyst**: Understand and possibly replace the Ru catalyst used in the Haber-Bosch process to produce ammonia



T gate: $\pi/4$ rotation around Z axis on the Bloch sphere

Credit: Mercedes Gimeno-Segovia (PsiQuantum) QCE22, 2022-09-20

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Quantum Computing Process Overview

Gill +, "Quantum computing: A taxonomy, systematic review and future directions", 2022, doi: 10.1002/spe.3039

- Optimize the complete system!

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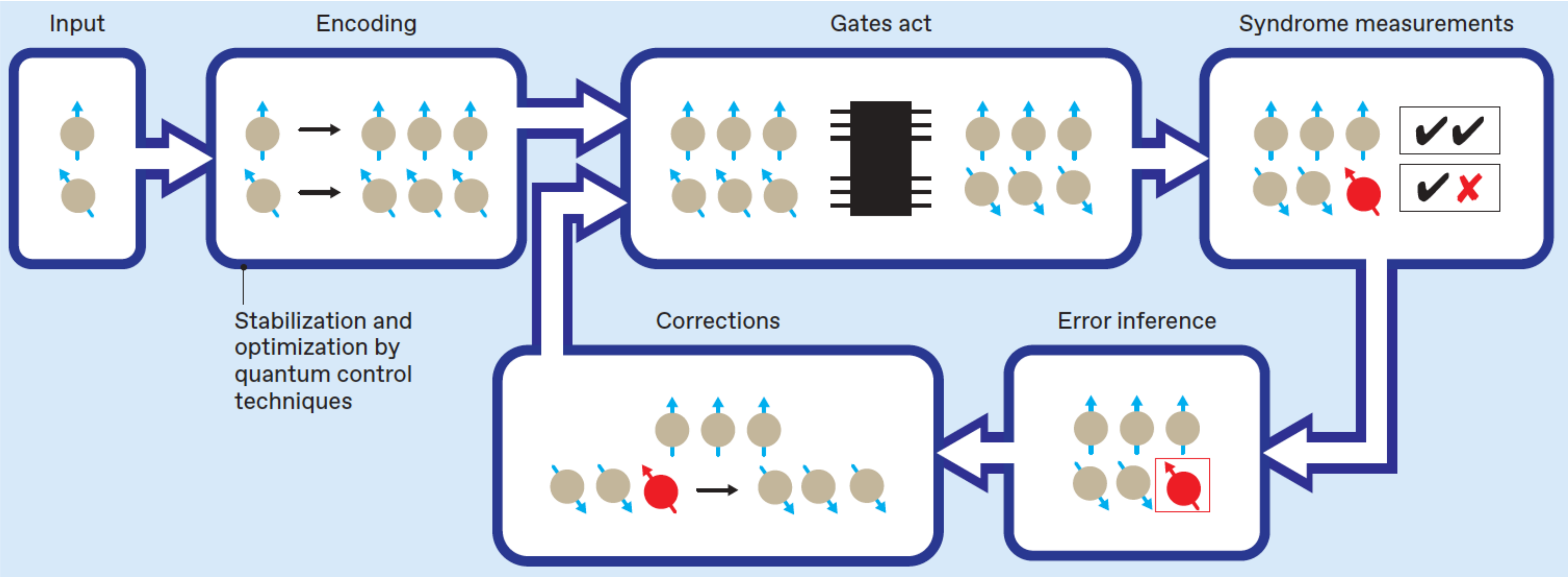
Gate Operation Cycle in Quantum Computing

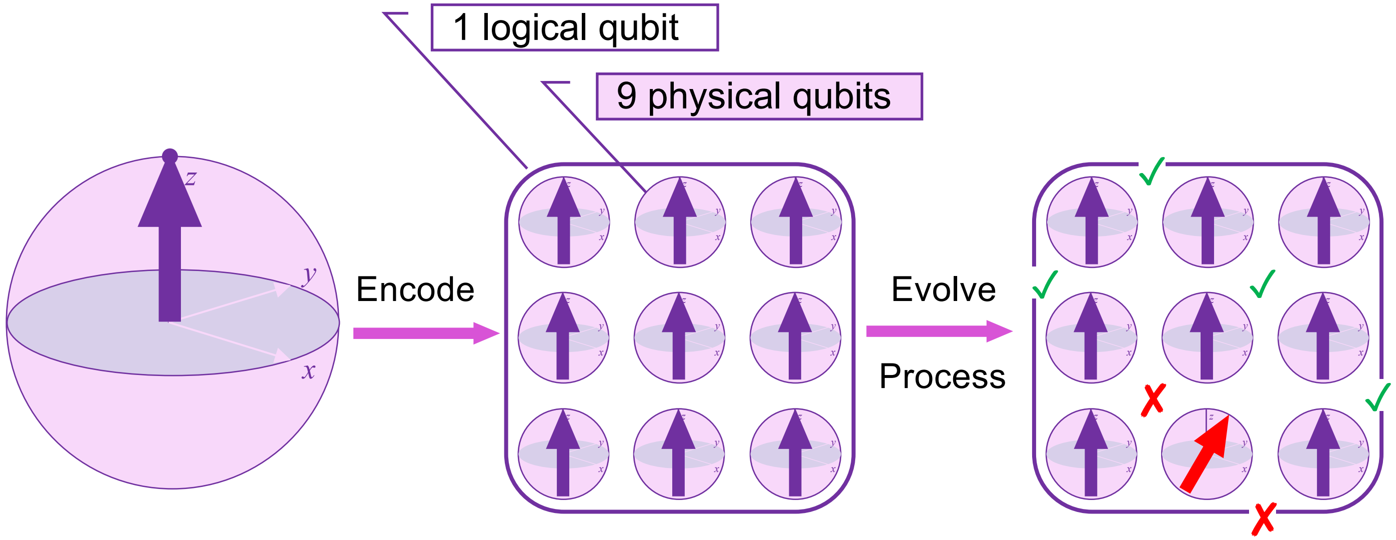


Biercuk and Stace, "Quantum error correction at the threshold," *IEEE Spectrum*, 2022, doi: 10.1109/MSPEC.2022.9819881

Logical and Physical Qubits

Making one stable qubit from many less-stable qubits

1. Create a **logical qubit** with information encoded (spread) onto a highly-entangled state of multiple **physical qubits**
2. Evolve process
3. Syndrome measurements on sets of physical qubits (even parity: ✓, odd: ✗)
4. Use syndrome pattern to determine error location and type



Note: Encoding is not cloning!

Note: Syndrome measurements (✓, ✗) do not collapse the qubit states

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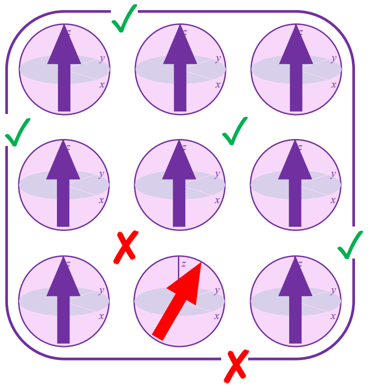
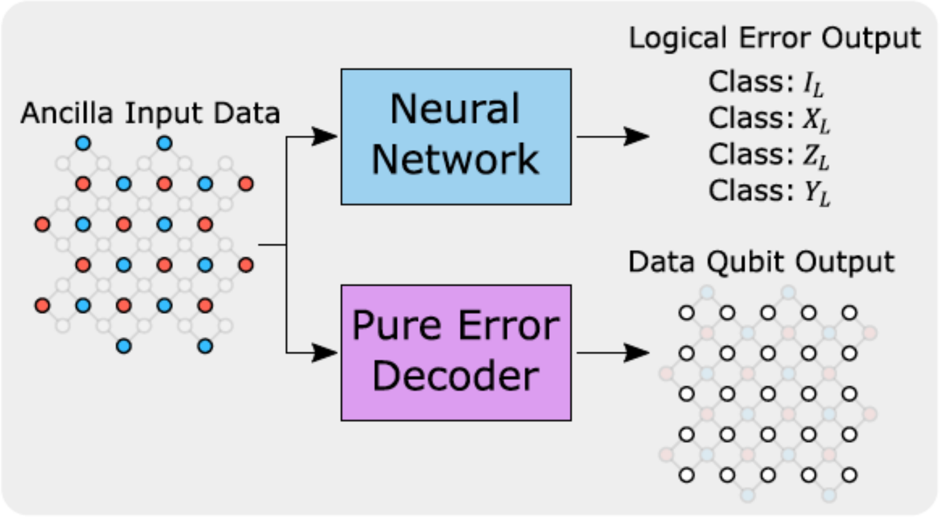
Error Inference

Use syndrome pattern to determine error location, type

- Error types
  - Bit flip errors
  - Phase slip errors
  - Measurement errors
- Limited number of correctable errors
  - Surface code = (d – 1)/2
  - Depends on the EC code
- Computation by
  - Classical, digital processing (supercomputer?)
  - Neural network
  - Quantum processing (?)





Overwater +, "Neural-network decoders for quantum error correction using surface codes," 2022, doi: 10.1109/TQE.2022.3174017

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Error Correction: Surface Codes

Commonly used with superconducting qubits

- 2-D architecture
  - Planar qubit lattice
  - Topological code needing only local operations for error correction
- High error threshold ($p_{th} \approx$ 1.E−2)
  - Logical qubit error probability per EC cycle

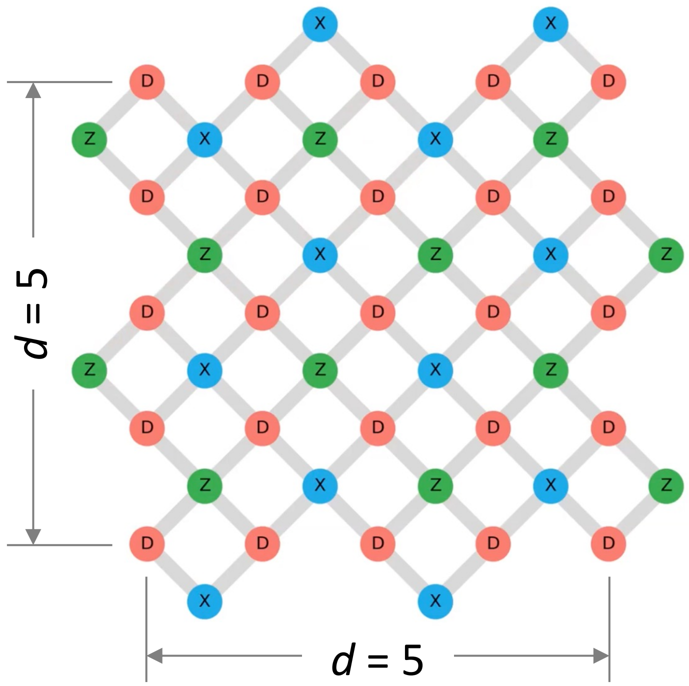
$$p_L \propto (p_p/p_{th})^{(d+1)/2}$$

$\boldsymbol{p_p}$: physical qubit error probability per cycle
(~ $\boldsymbol{p_{2Q}}$ error per 2 qubit gate operation)

$\boldsymbol{p_{th}}$: threshold error probability per cycle

d : distance of the code (bigger is better!)

- Number of correctable errors = $(d – 1)/2$



D Data qubits (d×d grid)
X X-type auxiliary qubit (phase slip errors)
Z Z-type auxiliary qubit (bit flip errors)
25+12+12 = 49 qubits

Fowler +, "Surface codes: Towards practical large-scale quantum computation," 2012, doi: 10.1103/PhysRevA.86.032324

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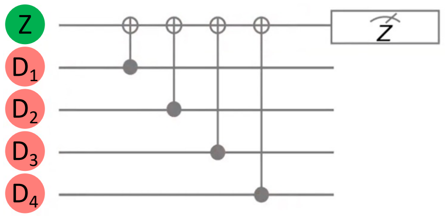
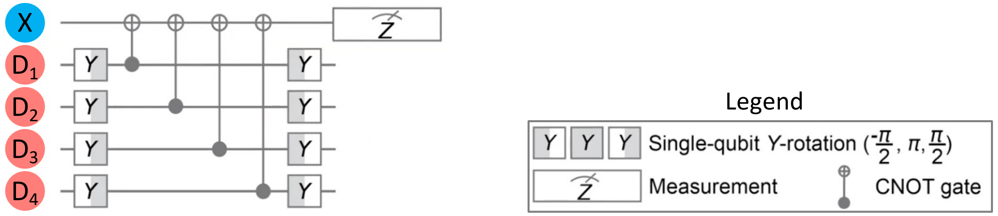
Surface Code Syndrome Measurements

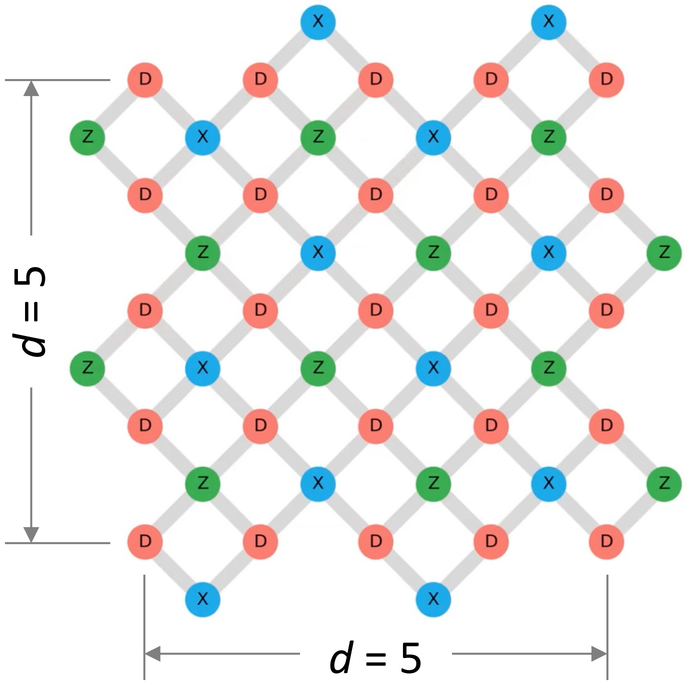
- Stabilizer parity measurement using auxiliary qubits
  - $Z_1Z_2Z_3Z_4$ (or Z_1Z_2 at edges) for every Z qubit



  - $X_1X_2X_3X_4$ (or X_1X_2 at edges) for every X qubit



- Requirements:
  - Gate operations with low error (*p*)
  - Fast, low-error ancilla qubit measurements
  - Low readout crosstalk between ancilla and data qubits
  - Ability to perform repeated gates and measurements



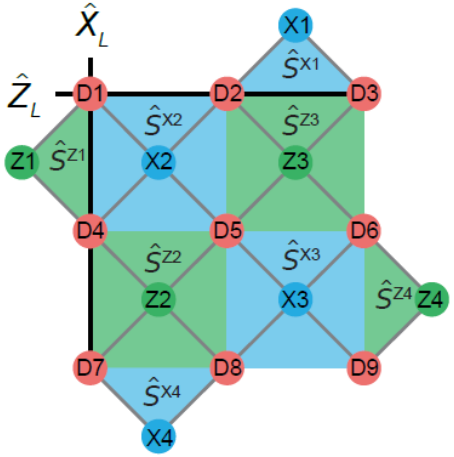
- D Data qubits (*d*×*d* grid)
- X X-type auxiliary qubit (phase slip errors)
- Z Z-type auxiliary qubit (bit flip errors)
- 25+12+12 = 49 qubits

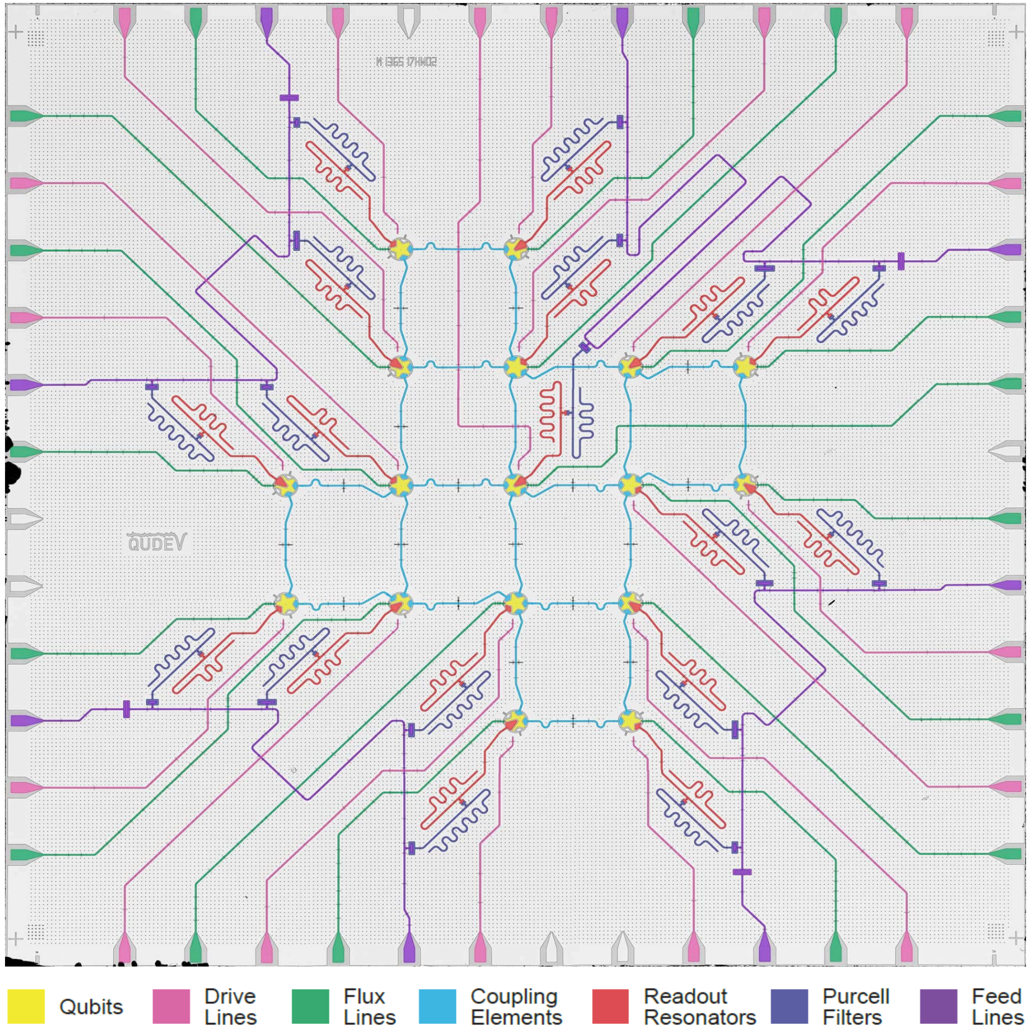
Versluis +, Phys. Rev. Appl., **8**, 034021 (2017)

Krinner +, Nature, **605**, 669 (2022)

Distance-3 Surface Code Qubit Chip

- Chip size ~ 15 mm × 15 mm
- Qubits are too small to see!
  - D 9 Data qubits (3×3 grid)
  - X 4 X-type auxiliary qubits (phase slip errors)
  - Z 4 Z-type auxiliary qubit (bit flip errors)
  - 9+4+4 = **17** qubits total
- Plenty of space for control line connections (low overall circuit density)
- Logical qubit error probability was only slightly worse than the physical qubit error probability, indicating progress towards error reduction



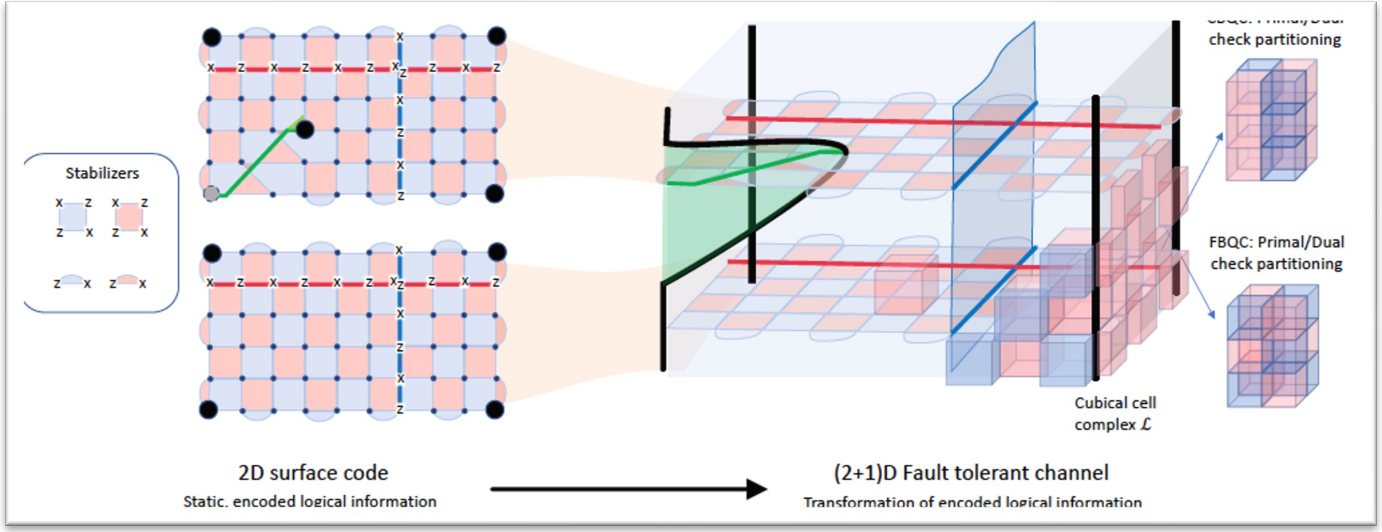


Krinner +, "Realizing repeated quantum error correction in a distance-three surface code", 2022, doi: 10.1038/s41586-022-04566-8

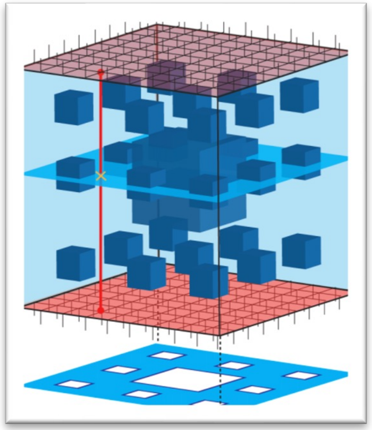
Error Correction: Alternatives to the Surface Code

There is more than one way to skin a qubit!

- Low-density parity check (LDPC) codes [1]
  - 2D, 4D hyperbolic codes
  - Freedman-Meyer-Luo codes
  - Tensor products
  - Fibre bundle codes
  - Lifted product codes
  - Balanced product codes
- Logical blocks [2]
- Fractal and topological codes [3, 4]



Logical block formation [2]



3D fractal surface code [3]

[1] Breuckmann +, "Quantum low-density parity-check codes," 2021, doi: 10.1103/PRXQuantum.2.040101
[2] Bombin +, "Logical blocks for fault-tolerant topological quantum computation," 2021, arXiv:2112.12160
[3] Zhu +, "Topological order, quantum codes, ... fractal geometries," 2022, doi: 10.1103/PRXQuantum.3.030338
[4] Kubica +, "Single-shot quantum error correction ... toric code", 2022, doi: 10.1038/s41467-022-33923-4

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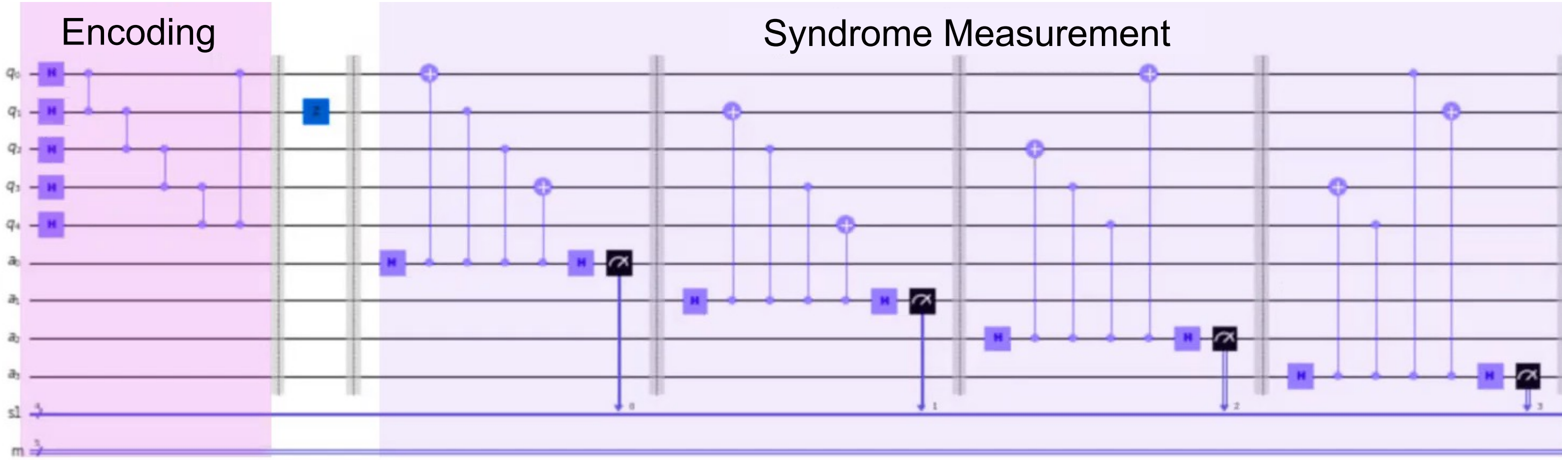
Error Correction Codes: Summary

What does it take to reduce the error?

- Error correction codes can require hundreds of operations
  - Comparing distant qubits can require information movement (swap gates)
- Each operation has a finite probability of error *(p_e) and* $p_p = \sum p_e$
- Threshold theorem:

  if $p_p < p_{th}$

  then $p_L < p_p$
- Threshold depends on the error correction code



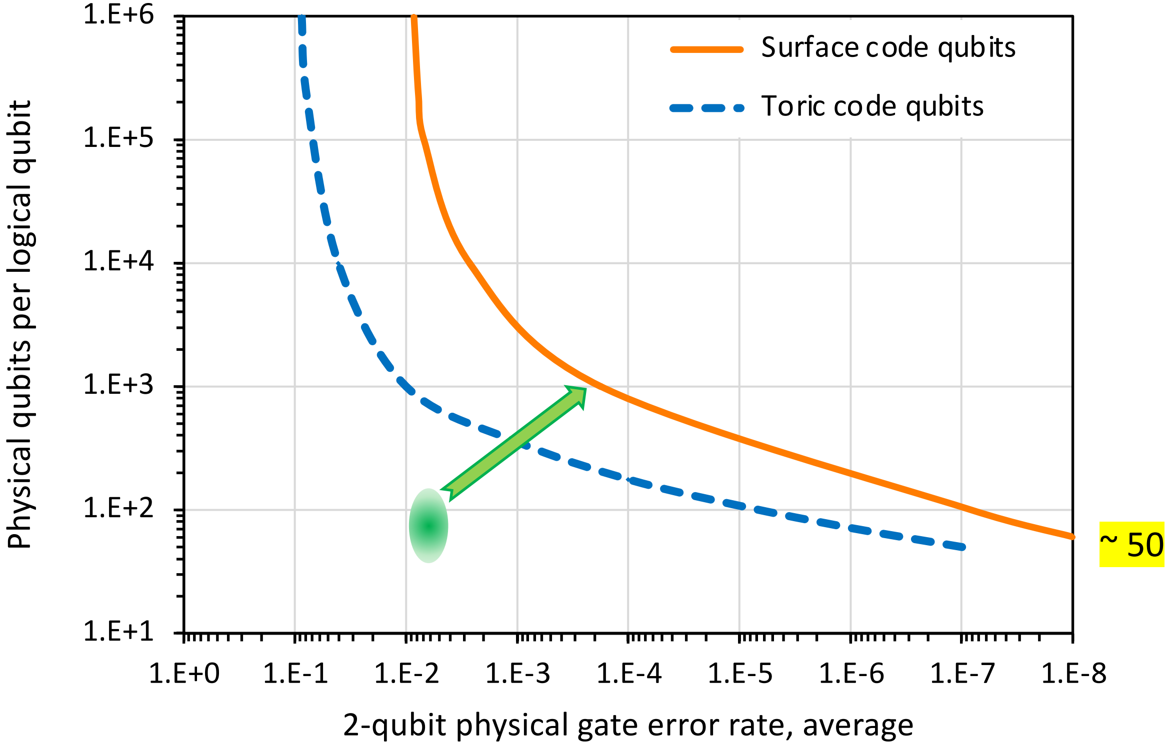
5-qubit quantum error correction code

Credit: Michael Biercuk (Q-CTRL) QCE22, 2022-09-20

Error Correction Resources

Number of physical qubits per logical qubit depends on several factors

- Examples:
  - Surface code [1] with $p_{th} \approx$ 1.E−2, Perfect decoder, Logical error: p_L = 1.E−18
  - Toric code [2] with $p_{th} \approx$ 1.E−1, Perfect decoder, Logical error: p_L = 1.E−15
- Needed:
  - Better EC codes (high threshold)
  - Hardware to implement the EC code
  - Lower gate error rates (~ 100× below threshold)



[1] Sevilla and Riedel, "Forecasting timelines of quantum computing," Dec. 2020. arXiv:2009.05045
[2] Biercuk, QCE, 2022-09-20; extrapolation based on: Watson +, New J. Phys. 16, 093045 (2014)

Qubit Control (and Readout)

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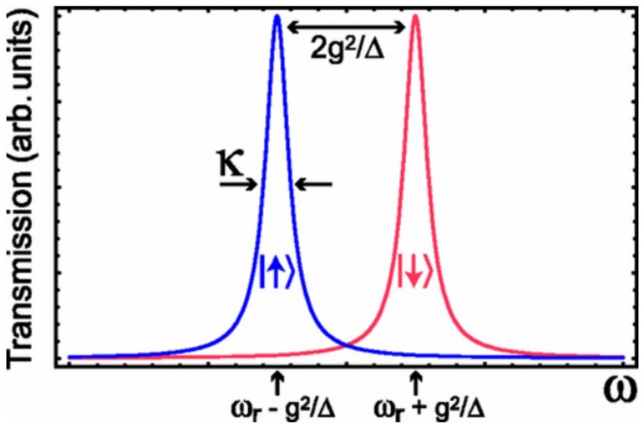
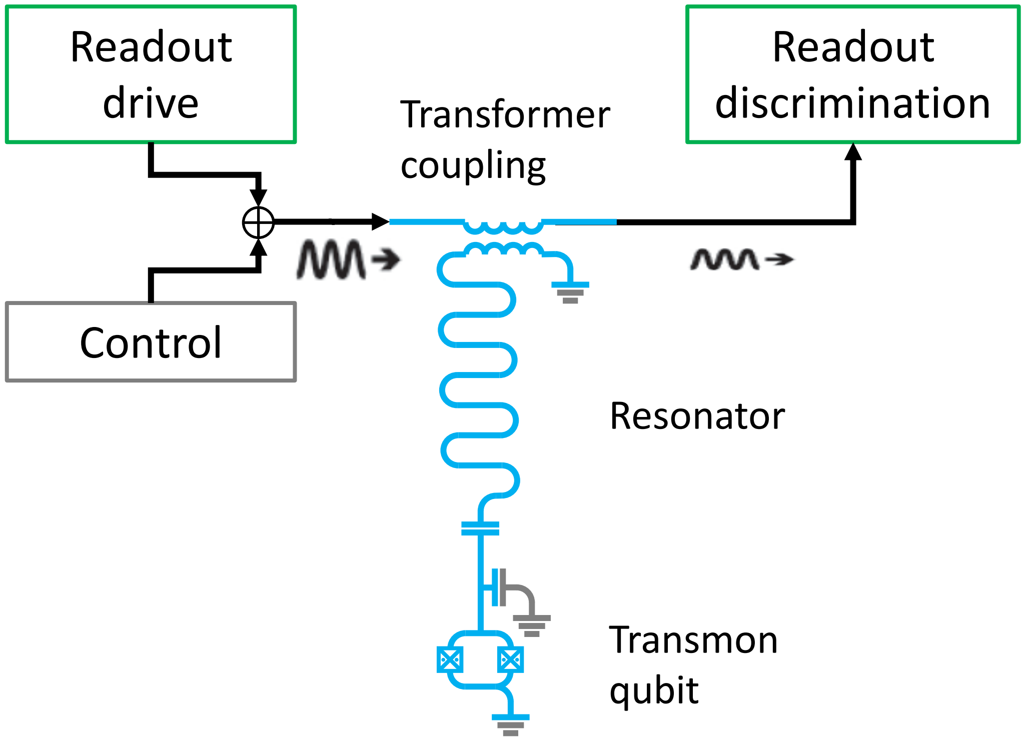
Qubit Control: Basics

Microwave engineering

- **Control**: Microwave signals change the qubit state
- **Readout**: Microwave transmission depends on qubit state



Blais +, 2004, doi: 10.1103/PhysRevA.69.062320



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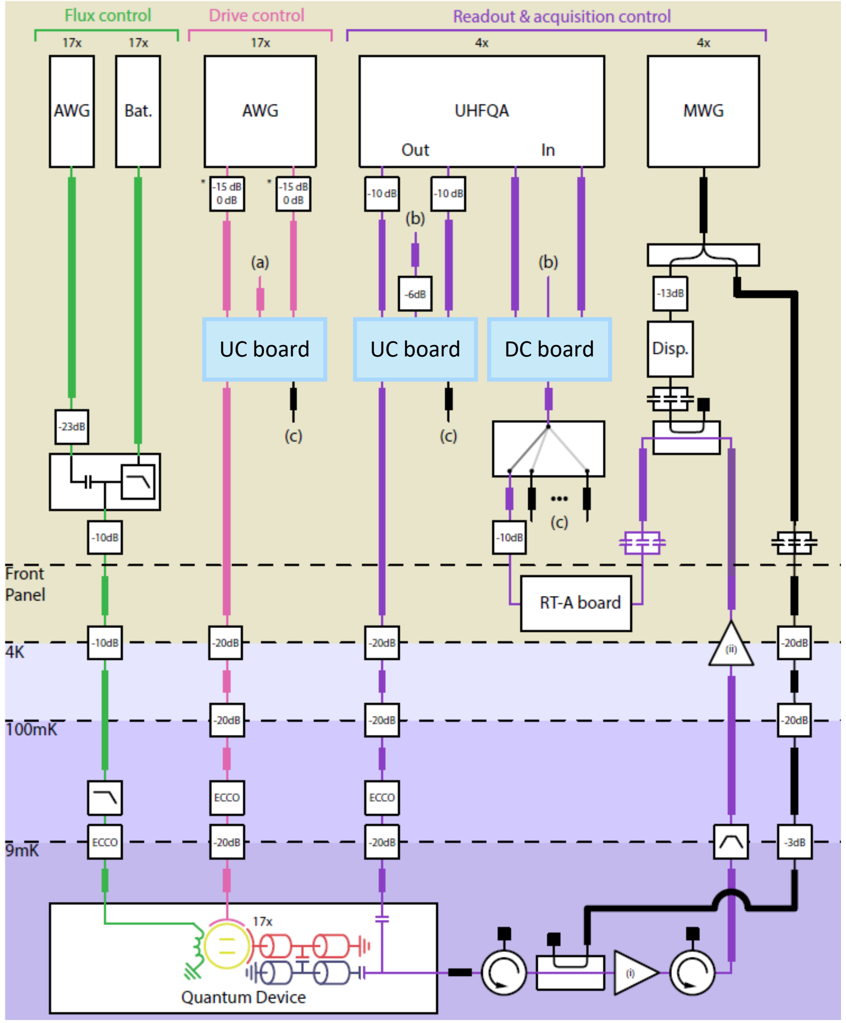
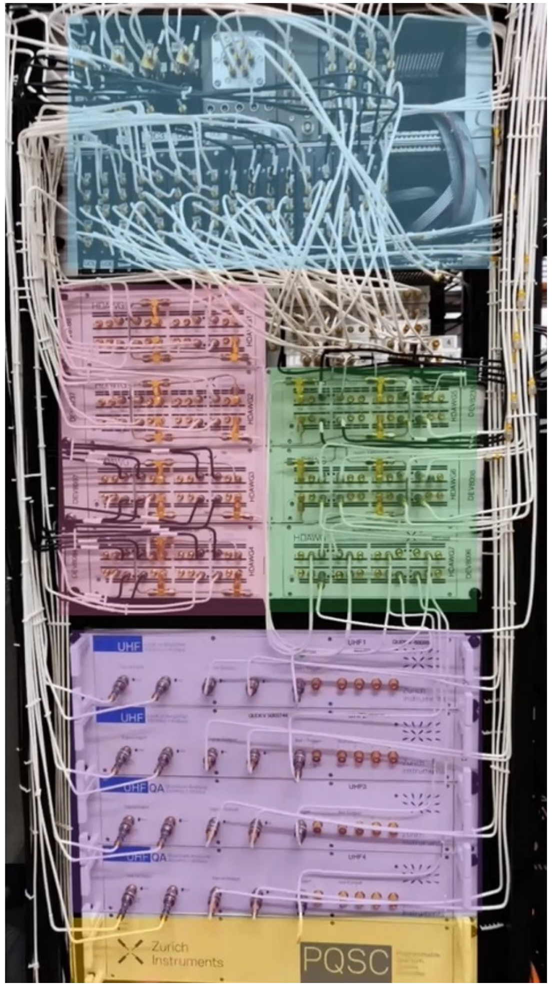
Qubit Control: Room-Temperature Electronics

- Qubit Control (HDAWG)
  - Flux drives
  - Baseband RF drives
- Qubit Readout (UHFQA)
  - Baseband signal generation and analysis (FPGA)
- Frequency conversion electronics (up, down) for qubit drive and readout
- Synchronization using PQSC
- Next steps:
  - Commercial, modular equipment customized for qubit control and readout





Krinner +, "Realizing repeated quantum error correction in a distance-three surface code", 2022, doi: 10.1038/s41586-022-04566-8

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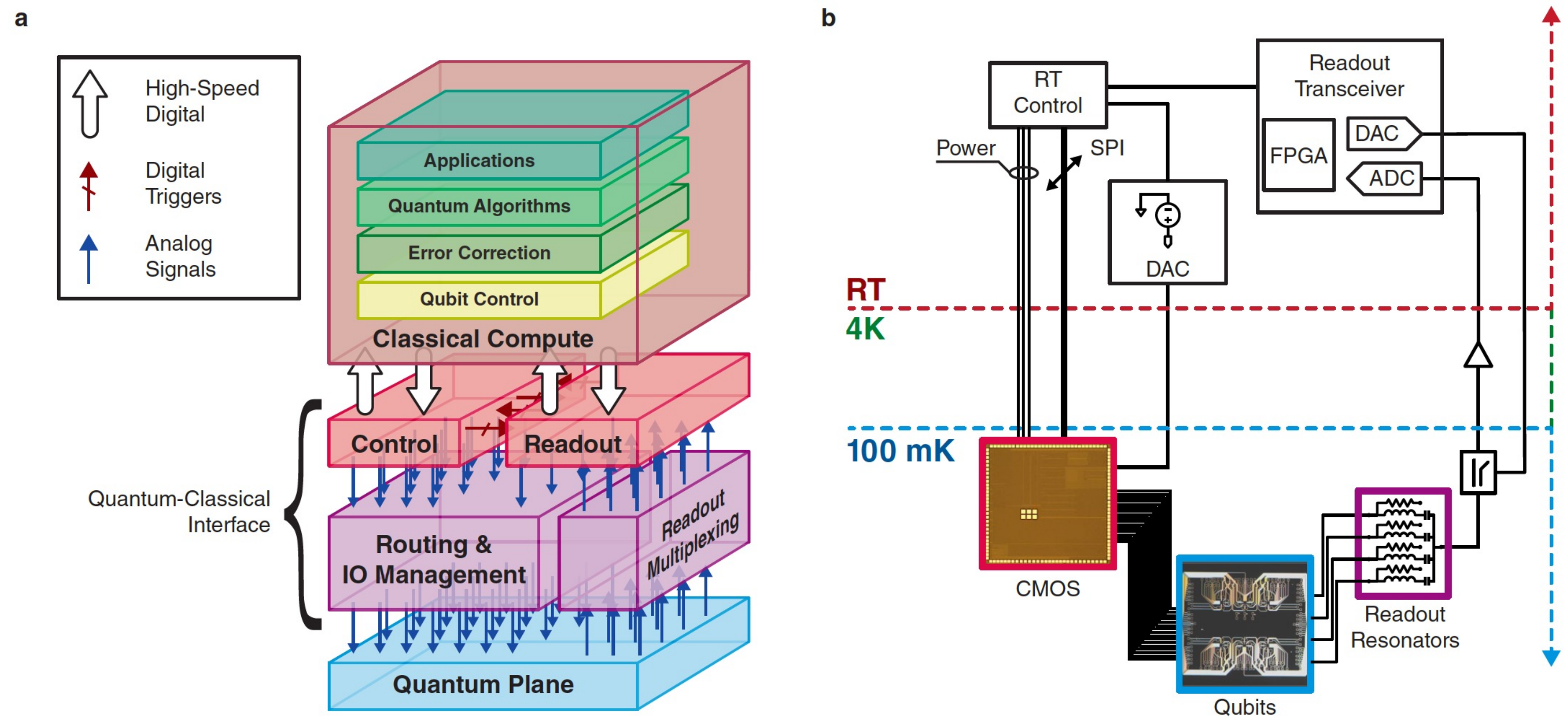
Qubit Control: Cryogenic Semiconductor Electronics

Quantum computing support



Microsoft: System to control and read out up to 32 voltage-controlled Si-qubits (not yet interacting) [1]

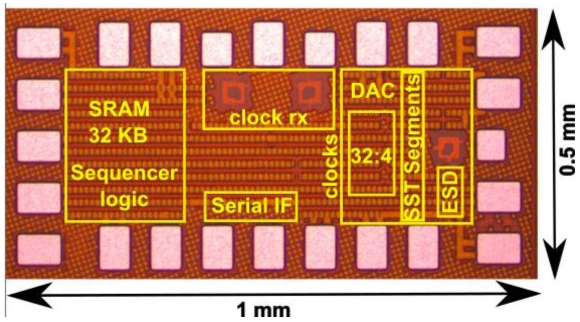
[1] S. J. Pauka *et al.*, “Characterizing quantum devices at scale with custom cryo-CMOS,” *Phys. Rev. Appl.*, vol. 13, no. 5, p. 054072, May 2020, doi: 10.1103/PhysRevApplied.13.054072.

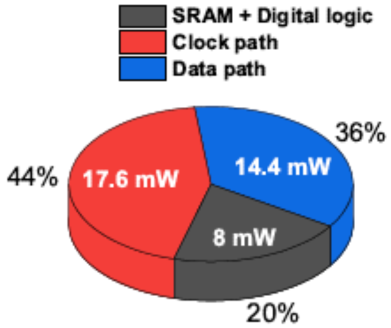
[2]. B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie, “Characterization and analysis of on-chip microwave passive components at cryogenic temperatures,” *IEEE J. Electron Devices Soc.*, Apr. 2020, doi: 10.1109/JEDS.2020.2986722.

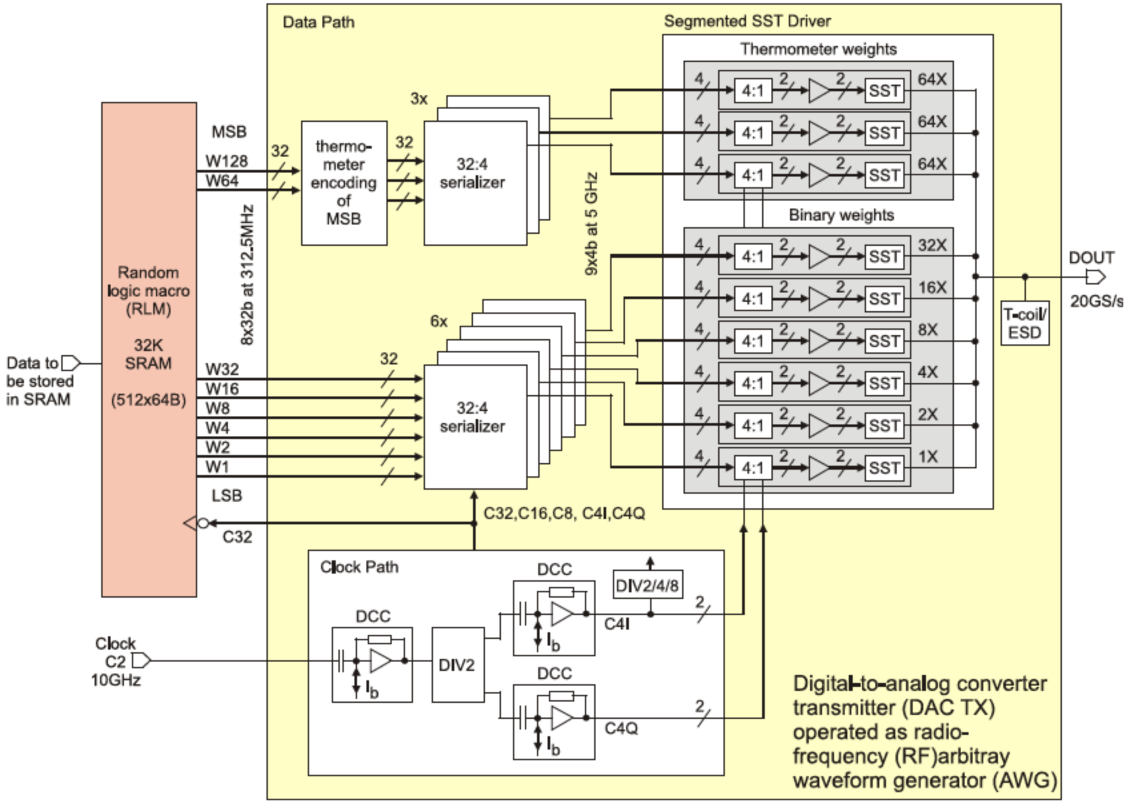
Qubit Control: Cryogenic Semiconductor Electronics

Development continues

- Digital to analog converter (DAC)
  - 32 KiB on-chip memory (SRAM)
  - 14 nm CMOS technology
  - Output at 4 K temperature: Qubit control waveforms in the 1 GHz to 18 GHz frequency range
  - Sampling rate: 40 GSa/s max.
  - 40 mW power dissipation at 4 K







Prathapan +, "A cryogenic SRAM based arbitrary waveform generator in 14 nm for spin qubit control," 2022, doi: 10.1109/ESSCIRC55480.2022.9911459.

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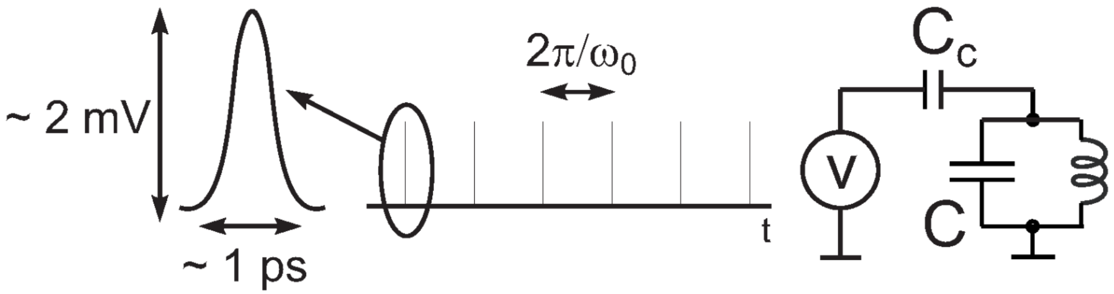
Qubit Control: Single Flux Quantum (SFQ) Pulses

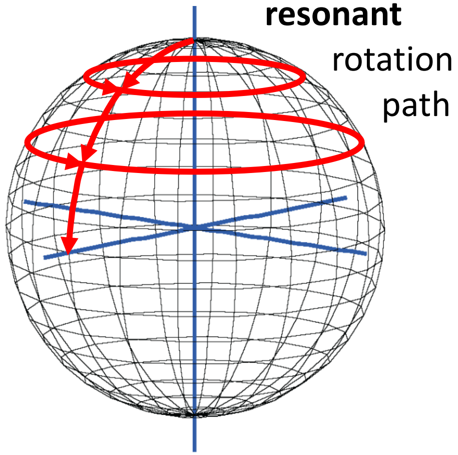
Skip conversion to microwaves

- Capacitively couple **resonant** train of narrow SFQ pulses to drive qubit rotations without microwaves [1]
- SFQ circuitry on flip-chip to reduce qubit degradation from quasiparticles
- **Optimized** SFQ pulse sequence reduces control error [2]
- Amplification of JJ output allows location of SFQ circuitry at 3 K temperature stage [3]



$$\delta\theta = C_c \Phi_0 \sqrt{\frac{2\omega_{01}}{\hbar C}}$$

- π rotation with ~100 pulses
- ~14 ns for 7 GHz qubit

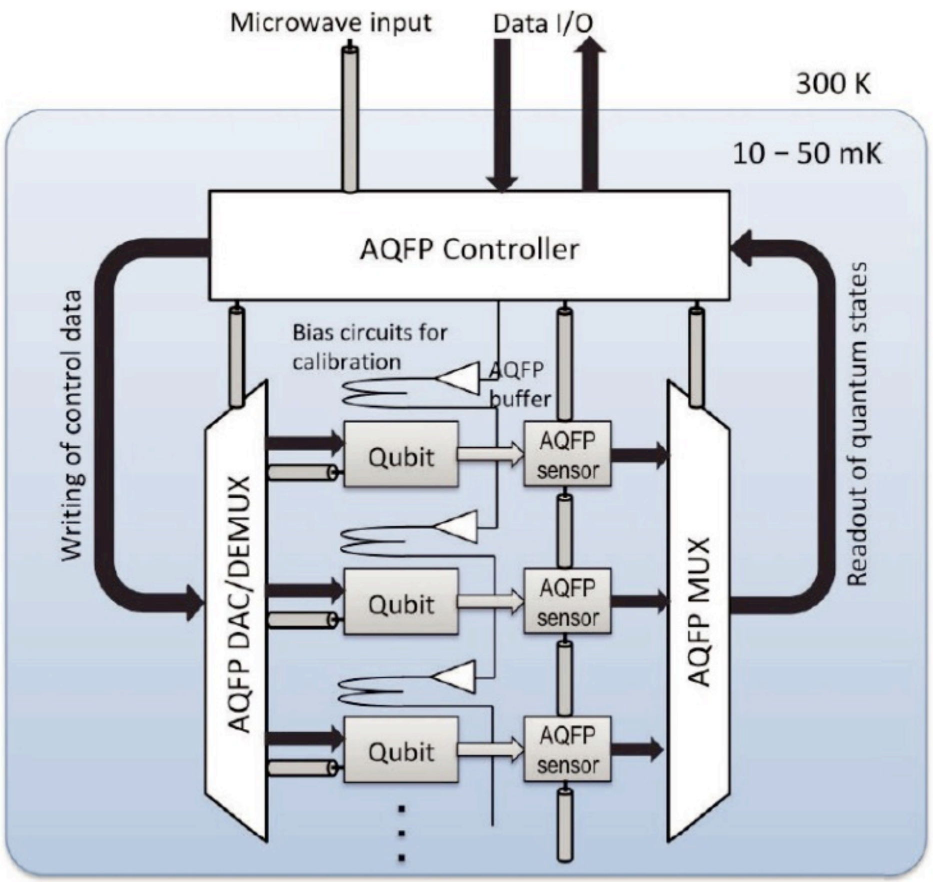


[1] McDermott +, 2014, doi: 10.1103/PhysRevApplied.2.014007
[2] McDermott +, 2018, doi: 10.1088/2058-9565/aaa3a0
[3] Howe +, 2022, doi: 10.1103/PRXQuantum.3.010350

Qubit Control: Superconductor Electronics

Seems like a natural for superconducting qubits

- Examples of recent work:
  - [1] Yoshikawa, "Superconducting digital electronics for controlling quantum computing systems," *IEICE*, 2019, doi: 10.1587/transele.2018SDI0003.
  - [2] Mukhanov +, "Scalable quantum computing infrastructure based on superconducting electronics," 2019, doi: 10.1109/IEDM19573.2019.8993634.
  - [3] Lecocq +, "Control and readout of a superconducting qubit using a photonic link," *Nature*, 2021, doi: 10.1038/s41586-021-03268-x.
  - [4] He +, "Compact RSFQ microwave pulse generator based on an integrated RF module for controlling superconducting qubits," *Appl. Phys. Lett.*, 2022, doi: 10.1063/5.0083972.
  - [5] Naaman +, "Synthesis of parametrically coupled networks," *PRX Quantum*, 2022, doi: 10.1103/PRXQuantum.3.020201.
  - [6] Ueno +, "NEO-QEC: Neural network enhanced online superconducting decoder for surface codes," 2022, doi: 10.48550/arXiv.2208.05758.
- AQFP is a superconductor electronic logic family with extremely low dissipation that could be used directly at mK temperatures [1]



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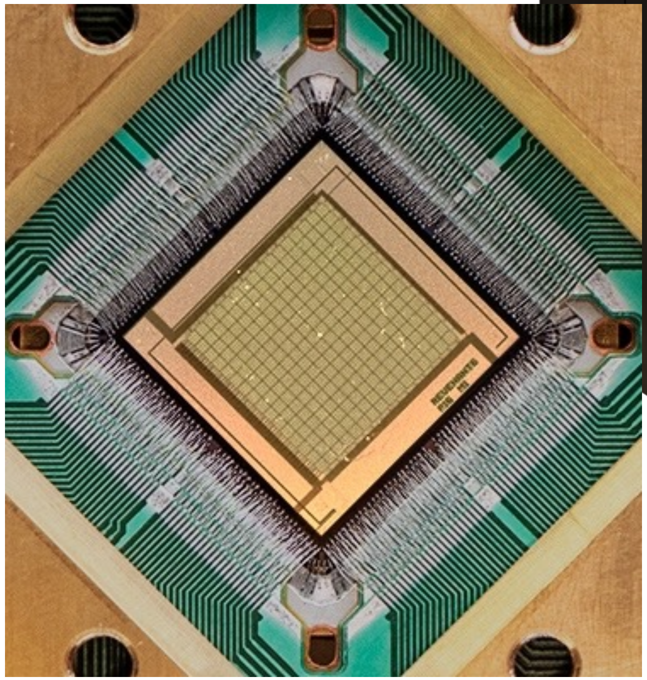
Quantum Processing Unit (D-Wave Systems)

Most complex superconductor electronic quantum control circuit

- D-Wave Advantage, Pegasus P16 quantum processing unit (QPU) using superconductor electronics
- 1,030,000 Josephson junctions
- 5640 qubit array
- 15 couplers per qubit
- Active area: 8.4 mm × 8.4 mm
- 15-20 mK operating temperature

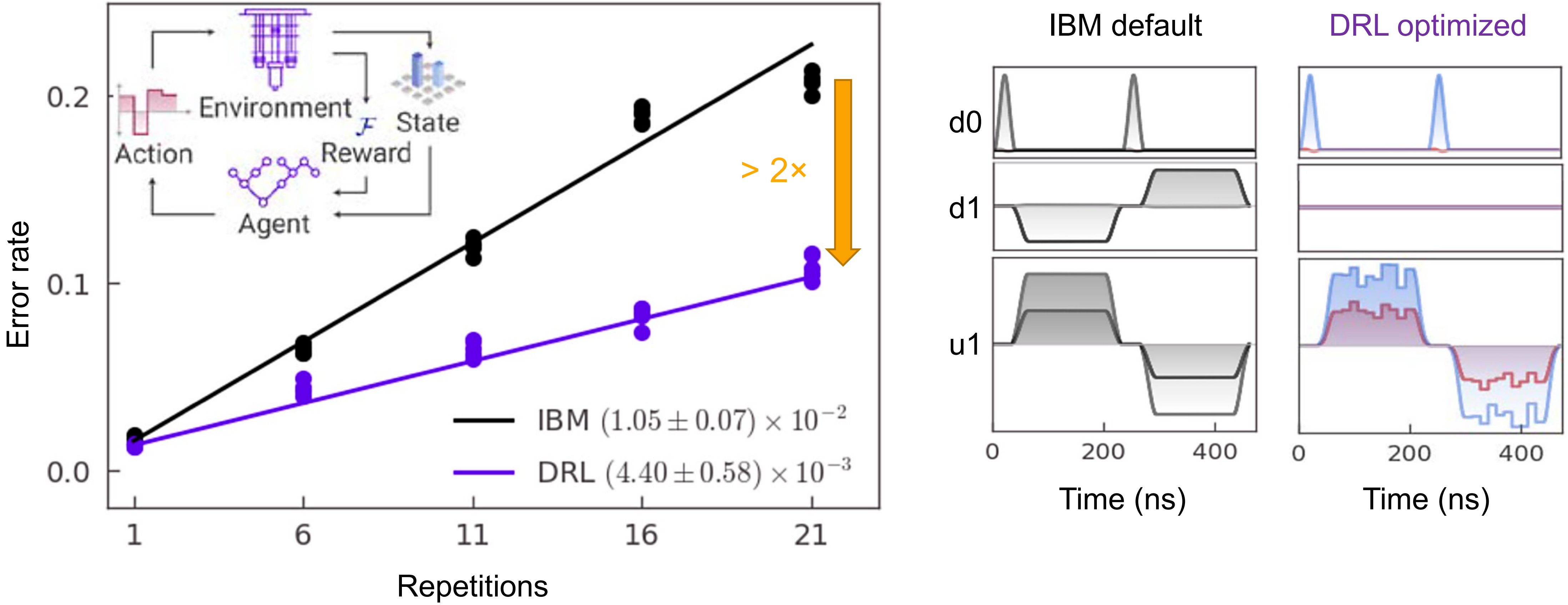


https://www.dwavesys.com/solutions-and-products/systems/

https://en.wikipedia.org/wiki/D-Wave_Systems#Pegasus

Control System Innovations (ML)

Deep reinforcement learning (DRL) agent discovers simpler, better controls



Y. Baum +, "Experimental deep reinforcement learning for error-robust gate-set design on a superconducting quantum computer," *PRX Quantum*, 2021, doi: 10.1103/PRXQuantum.2.040324

Mundada +, "Experimental benchmarking of an automated deterministic error suppression workflow for quantum algorithms," 2022, arXiv.2209.06864

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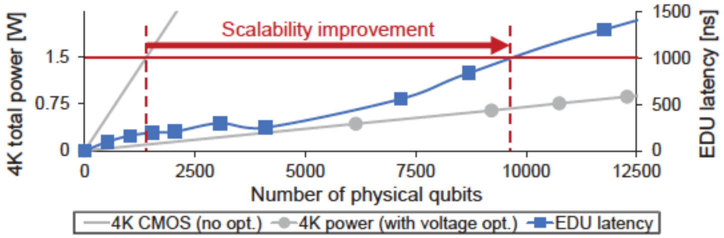
Limits for superconducting qubit control

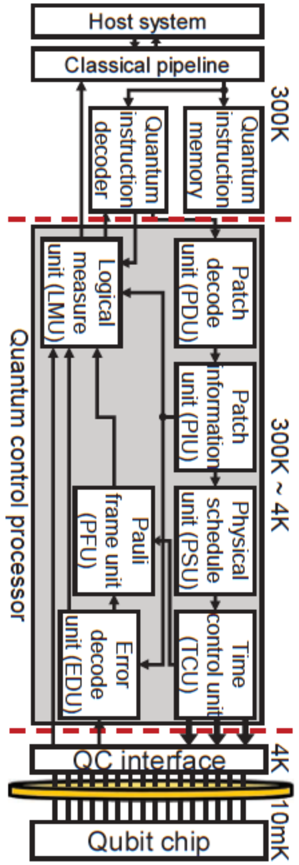
Where are the breakpoints?

- **XQsim**: quantum control processor simulator (open-source, cross-technology)
- Scalability analysis
    - Maximum number of qubits subject to constraints (delay, power, area)
    - Did not include QC interface



CMOS @ 4 K scalability analysis [1, Fig. 17b]

[1] Byun +, "XQsim: modeling cross-technology control processors for 10+K qubit quantum computers," Jun. 2022, doi: 10.1145/3470496.3527417.

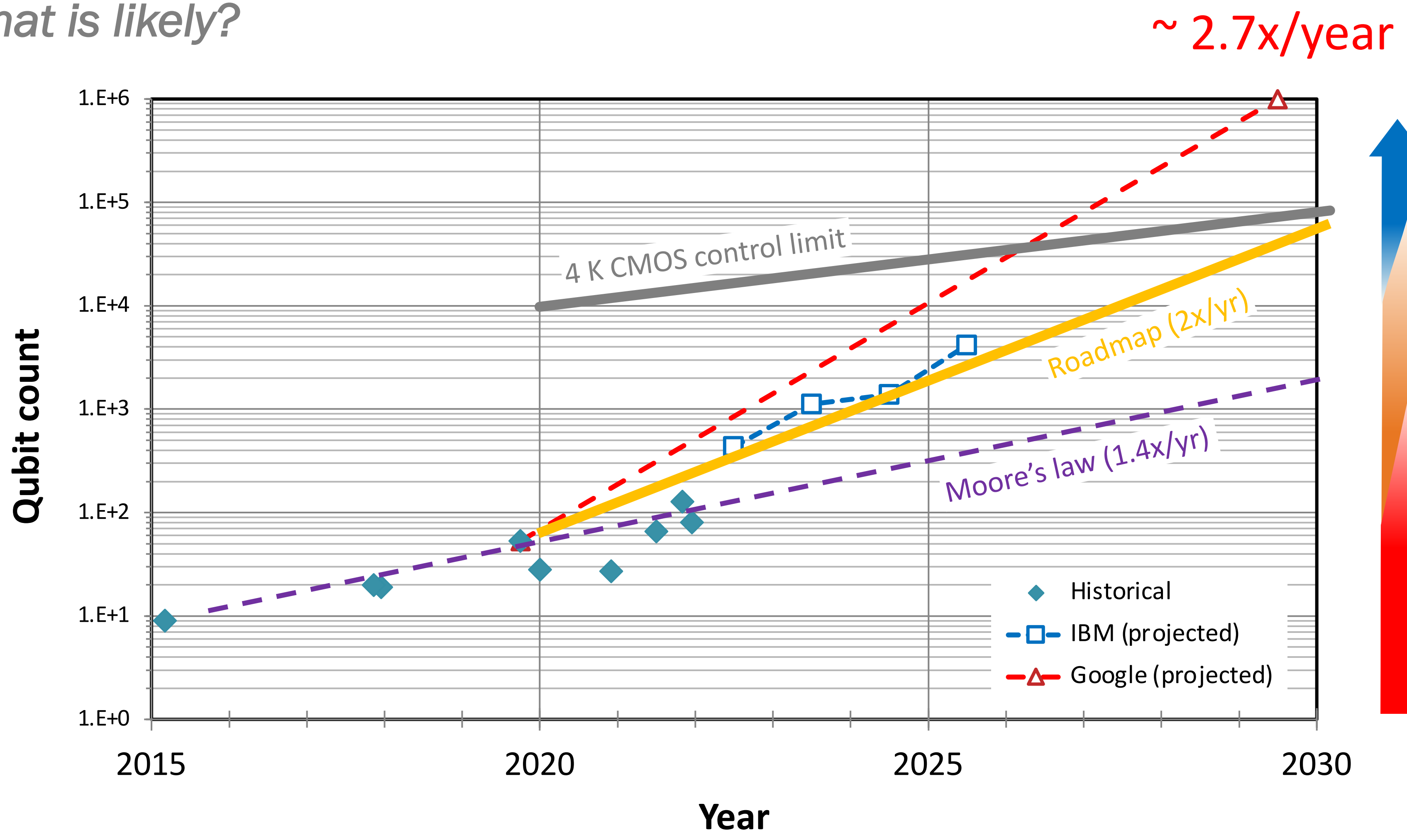


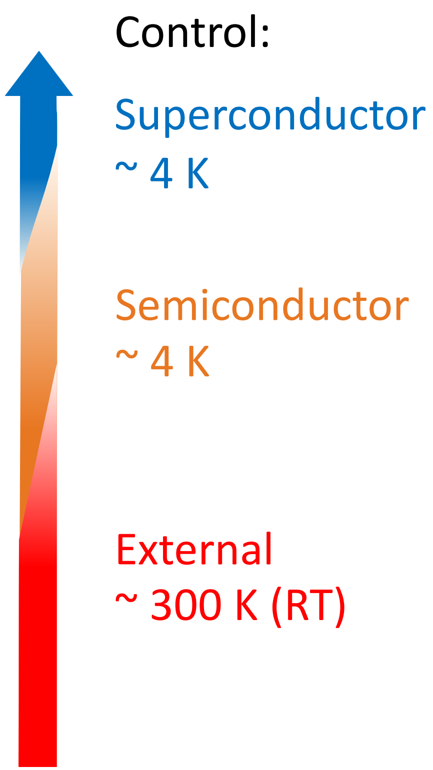
Fault-tolerant quantum computer system overview [1, Fig. 1]

Error decoder	
1e-3	Phys. error rate
15	Code distance
QECOOL:	Baseline error decoder
Physical quantum gate latency	
14 ns	1-qubit gate
26 ns	2-qubit gate
600 ns	Measurement
Refrigeration and wiring	
1.5 W	4 K power budget
620 cm^2	4 K area budget
31 mW, 10 Gb/s coaxial cable 300-4 K	
Clock frequency	
1.5 GHz	CMOS @ 4 K or 300 K
21 GHz	RSFQ or ERSFQ @ 4 K
Qubits controllable (limiting factor)	
1,700	CMOS @ 300 K (heat leak)
9,800	CMOS @ 4 K (delay)
4,600	RSFQ @ 4 K (power)
59,000	ERSFQ @ 4 K (power)
?	AQFP @ 4 K (?)

Superconducting Qubit Roadmap

What is likely?





Google: https://www.cnet.com/tech/computing/quantum-computer-makers-like-their-odds-for-big-progress-soon/

IBM: https://research.ibm.com/blog/ibm-quantum-roadmap-2025

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Qubit Design and Fabrication

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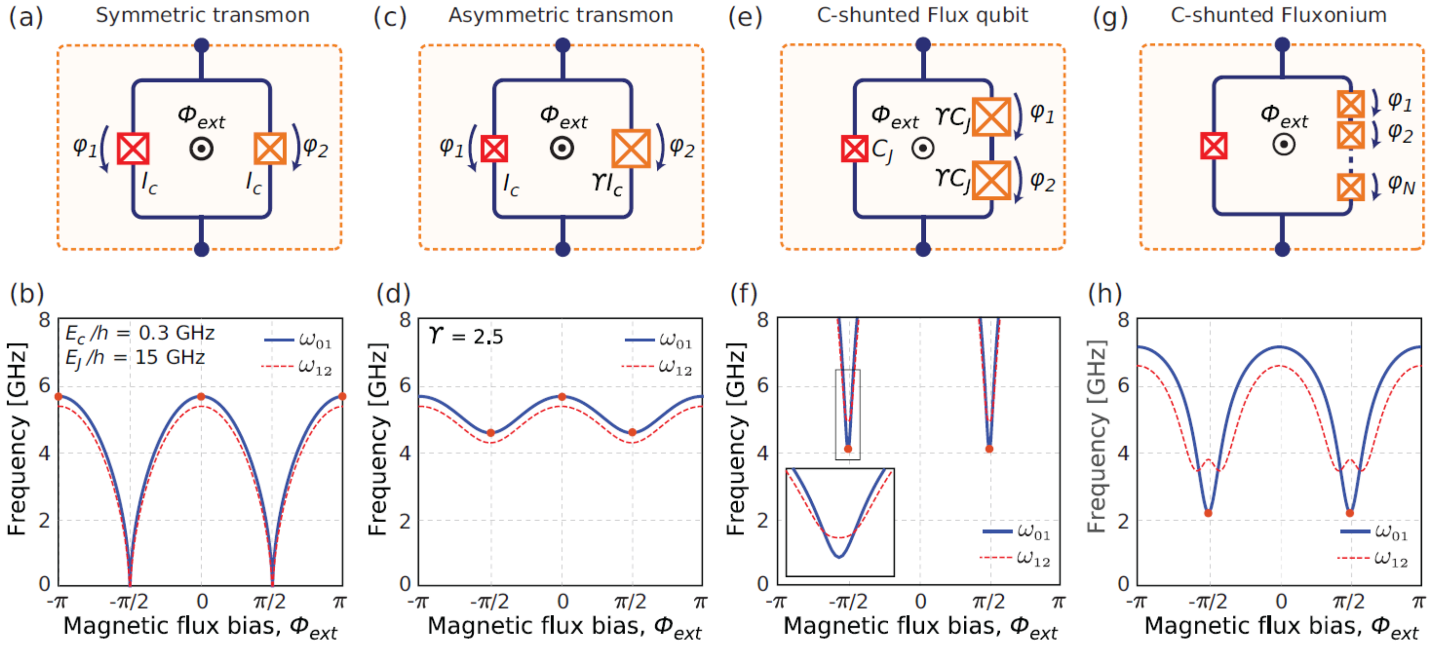
Superconducting Qubit Designs

Artificial qubits allow variety

- A few of the many types
  - Transmons
  - Flux qubits
  - Fluxonium
- Transmons have been dominant but might not scale
- Design for quantum error mitigation (QEM)
- Interconnect engineering (q-q, q-ctrl, q-readout) requires tradeoffs
- Still plenty of room for innovation!



Modular qubit circuit representations for capacitively shunted qubit modalities and corresponding qubit transition frequencies [1] Fig. 2

Krantz +, "A quantum engineer's guide to superconducting qubits," 2019, doi: 10.1063/1.5089550

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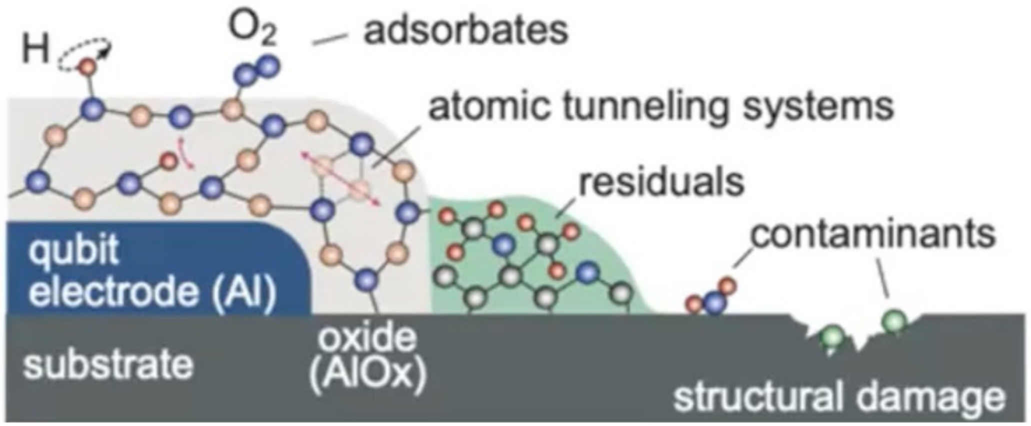
Materials affect qubit performance

Recent developments in understanding

- Metals
  - ✗ **Nb hydrides** precipitate on cooldown, vary over time, and affect transmon qubit performance [1]
  - ✗ **Nb oxides** vary in stoichiometry and crystallinity, leading to two-level systems that reduce qubit performance [2], [3]
  - **Ta** seems to perform better than Nb with transmon qubit lifetimes up to 500 µs [4]
- Substrate (wafers)
  - ✗ **Si** wafers have ~ 10x higher dielectric losses than expected [5]
  - ^{28}**Si** might be better
  - Al_2O_3 (sapphire) wafers have lower losses than Si, but TSVs are difficult ✗



Materials in qubit devices (credit: Anna Grassellino, FNAL)

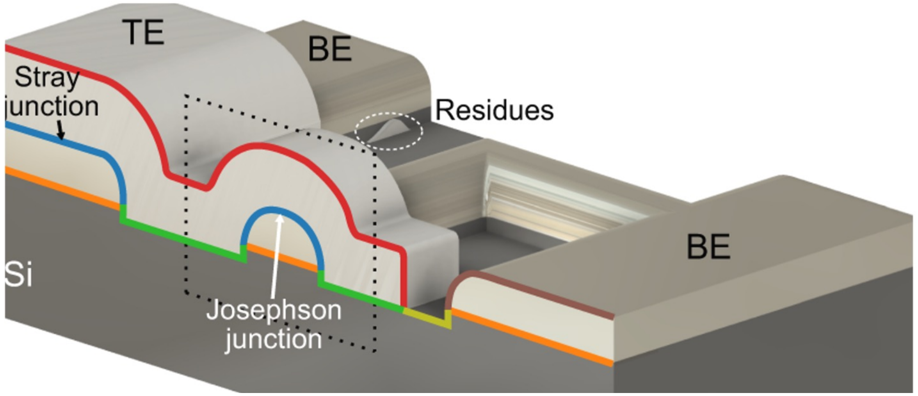
[1] Lee +, 2021, arXiv.2108.10385
[2] Murthy +, *Appl. Phys. Lett.*, 044002, 2022, doi: 10.1063/5.0079321
[3] Murthy +, 2022, arXiv.2203.08710
[4] Wang +, npj Quantum Inf., 2022, doi: 10.1038/s41534-021-00510-2
[5] Checchin +, *Phys. Rev. Appl.*, 2022, doi: 10.1103/PhysRevApplied.18.034013

Josephson Junction Fabrication for Qubits

Designs suitable for 200 or 300 mm fabrication processes

- Needed is a better process than aluminum (Al) double-angle evaporation and lift-off commonly used today
- Development has started

Ta/TaN/Ta junction (proposed)
[1] Fig. 8.



Al/AlOx/Al junction, T_1 ~ 100 μs, p_{1g} ~ 6e−4
[2] Fig. 1a.

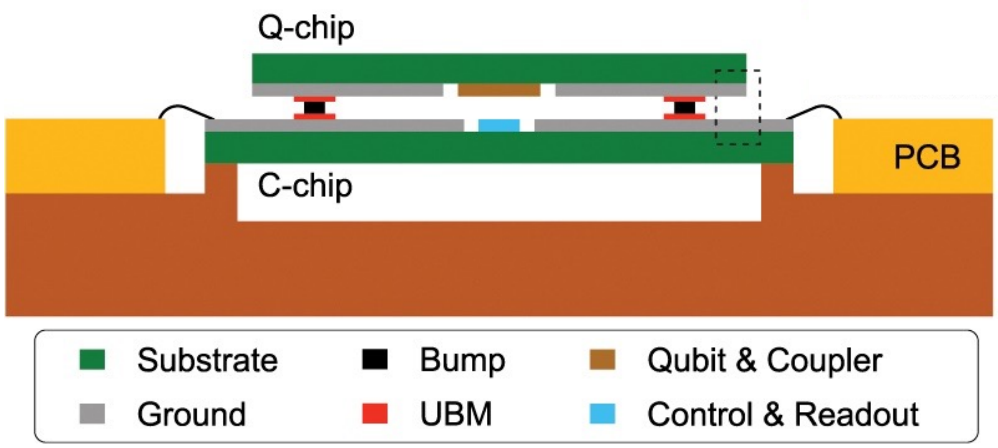
[1] Papa Rao +, *ECS Trans.*, **85**, 151 (2018) doi: 10.1149/08506.0151ecst

[2] Verjauw +, *npj Quantum Inf.*, **8**, 93 (2022) doi: 10.1038/s41534-022-00600-9

Multi-chip Modules (MCM)

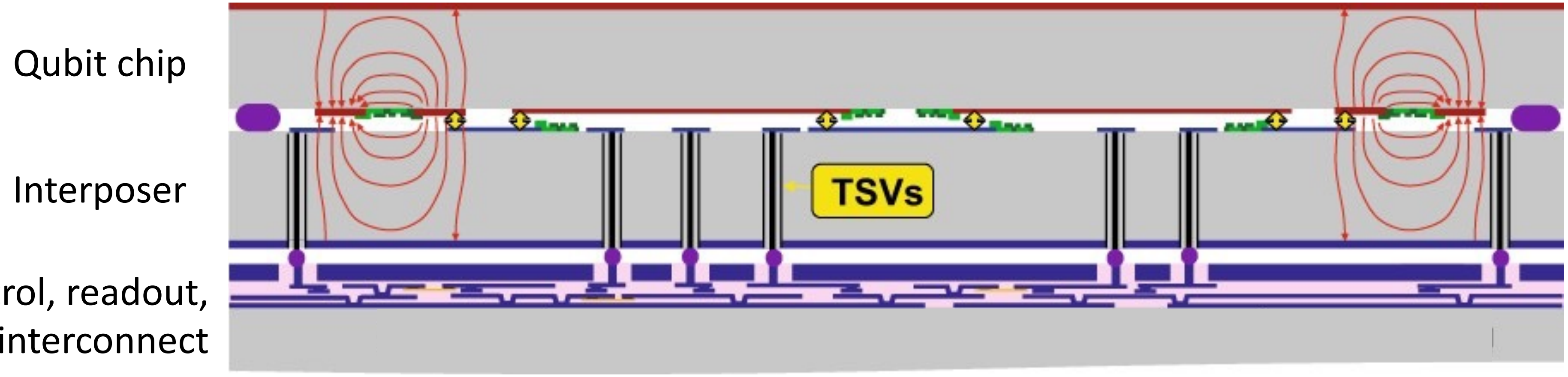
Heterogeneous integration and packaging

- Flip-chip
- Interposers or further stacking require superconducting through-substrate vias (TSVs)



[1] Fig. 1b

[2] Fig. 1



[1] Kosen +, *Quantum Sci. Technol.*, **7**, 035018 (2022) doi: 10.1088/2058-9565/ac734b
[2] Rosenberg +, npj Quantum Inf., **3**, 42 (2017) doi: 10.1038/s41534-017-0044-0

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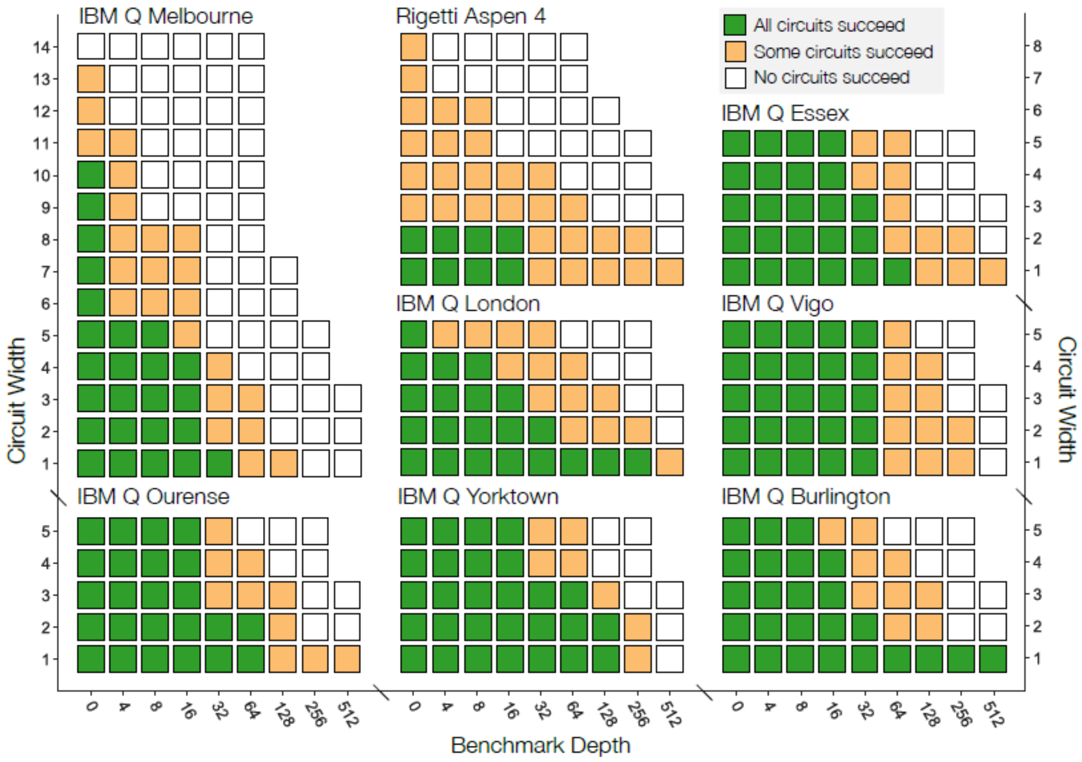
Roadmap

Metrics for Quantum Computing

Still seeking clarity

- Scale
  - Qubit count (not sufficient!)
- Quality
  - Quantum Volume (QV) [1]
  - Algorithmic Qubits (AQ) [2]
  - Mirror circuit benchmarks [3]
- Speed
  - Circuit Layer Operations Per Second (CLOPS) [1]



Empirical capability regions from **mirror circuit benchmarks** on various superconducting quantum processors [3] Fig. 3

[1] Wack +, 2021, arXiv:2110.14108

[2] Lubinski +, 2021, arXiv:2110.03137

[3] Proctor +, 2022, doi: 10.1038/s41567-021-01409-7

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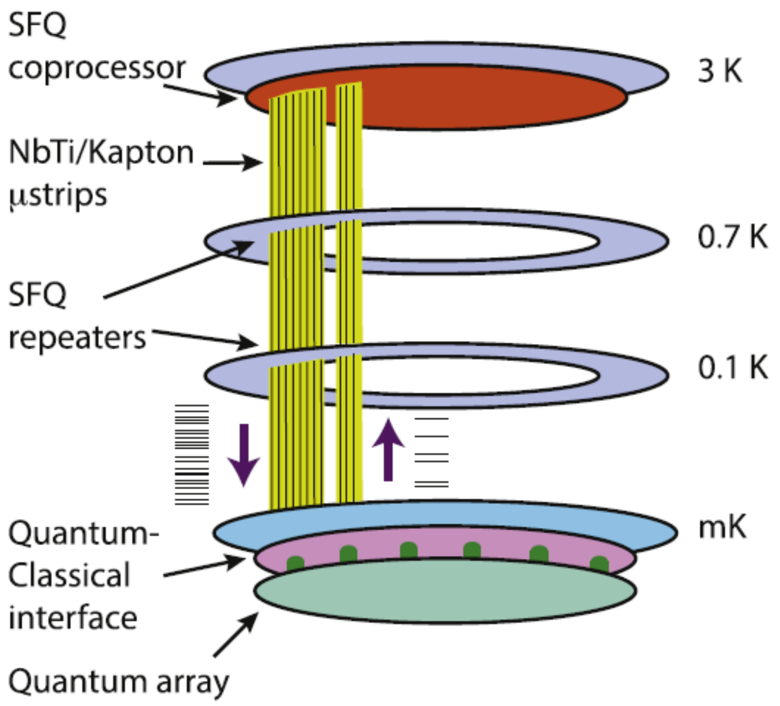
Scaling Requirements

QC with Superconducting Qubits

- Qubits
  - Low gate error rates (2-qubit is most important)
  - Large gate depth (qubit coherence time divided by gate time)
  - Low variation in qubit parameters
  - Modular architecture
- Interconnects
  - Reliable, low error
  - Switchable or tunable to avoid frequency crowding
- Control
  - Low error rates
  - Fast (relative to qubit coherence time)
  - Low power and energy
- Fabrication
  - Ability to manufacture at large scale



McDermott +, "Quantum–classical interface based on single flux quantum digital logic," Quantum Sci. Technol. 2018, doi: 10.1088/2058-9565/aaa3a0

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2023 Superconducting QC Roadmap, First Cut

Metric	2020	2022	2024	2026	2028	2030	2032
Qubit growth per year	2×	2×	2×	2×	2×	2×	2×
Qubit count	5.5e+1	2.2e+2	8.8e+2	3.5e+3	1.4e+4	5.6e+4	2.2e+5
Qubit type	Transmon	Transmon	Transmon	Transmon	?	?	?
Qubit lifetime T1, med. [ms]	0.5					10	
2 qubit gate error rate, median (p_2Q)	1.0e-2					1.0e-4	
Gate depth (1/p_2Q)	1.0e+2					1.0e+4	
Error correction code	Surface	Surface	Surface	Surface	Surface	Surface	?
Phys. qubits per logical qubit				1000	1000	1000	1000
Logical qubit count				3	14	56	220
Logical qubit error rate						1.0e-15	
Control type, temp. [K]	CMOS, 300	CMOS, 300	CMOS, 300	CMOS, 4	CMOS, 4	CMOS, 4	SCE, 4
SCE control complexity [JJ]	1.1e+5	4.5e+5	1.8e+6	7.2e+6	2.9e+7	1.2e+8	4.6e+8

In Progress

Superconducting quantum computing technology roadmap: First cut

Summary

1. No one approach is superior in every way
   - Tradeoffs need to be made at many levels
   - Overall system fitness will likely determine the winner
   - Plenty of opportunity for innovation at all levels

2. Roadmaps can help to guide R&D even when we don’t know how to build a fault-tolerant superconducting quantum computer
   - Difficult challenges need timelines to solution
   - System models will guide the roadmapping process

3. Superconductor electronics is a key need for superconducting QC
   - Good match in terms of circuit complexity and timeline
   - Don’t waste the opportunity!

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Catching the wave

Be ready!

Image by Kanenori from Pixabay

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Backup

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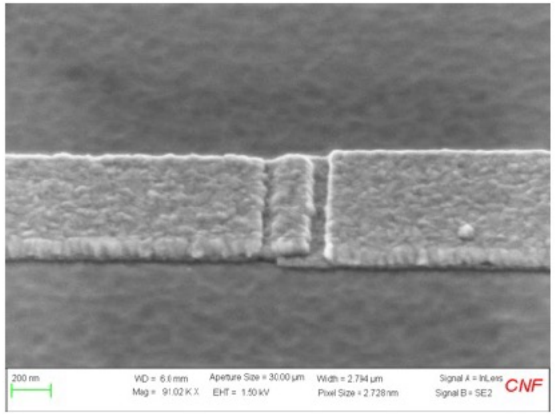
Basics: Superconducting qubits as anharmonic oscillators

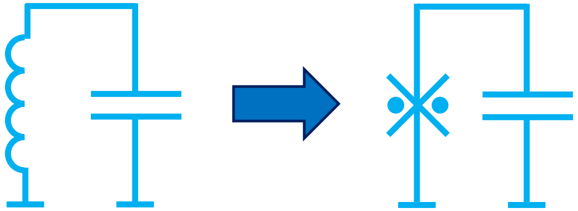
- Josephson tunnel junctions serve as superconducting nonlinear inductors

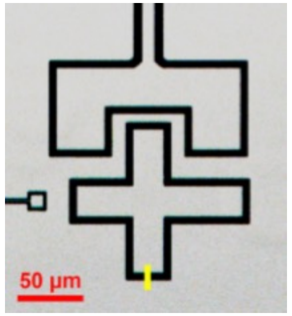


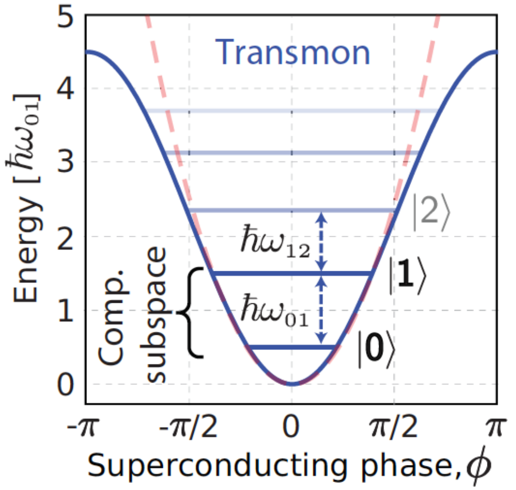
$$L_{Jt} = \frac{\Phi_0}{2\pi I_c}\left[\frac{\sin^{-1}(i/I_c)}{i/I_c}\right]$$

$$= L_{J0}\left[\frac{\varphi}{\sin\varphi}\right] \approx \frac{L_{J0}}{\cos\varphi}$$

- Shunt a Josephson junction with a capacitor to form a resonant circuit that functions as a qubit
  - Capacitor ≈ 70 fF
  - Junction critical current I_c ≈ 30 nA
  - Transition frequency ω_{01} ≈ 5 GHz
  - Anharmonicity $(\omega_{01} - \omega_{12})$ ≈ 300 MHz







Krantz +, "A quantum engineer's guide to superconducting qubits," 2019, doi: 10.1063/1.5089550

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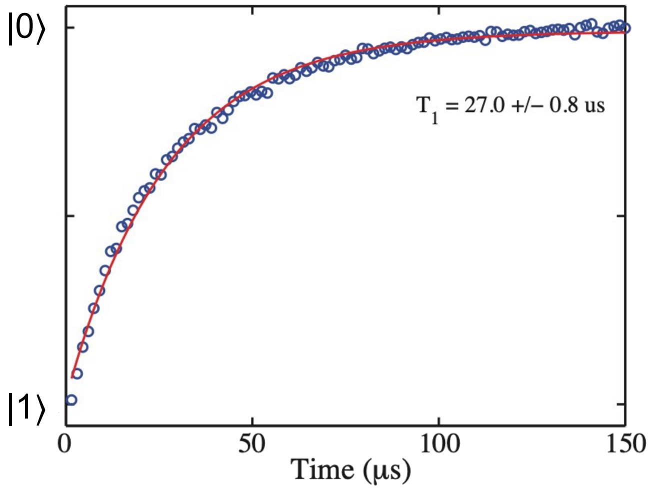
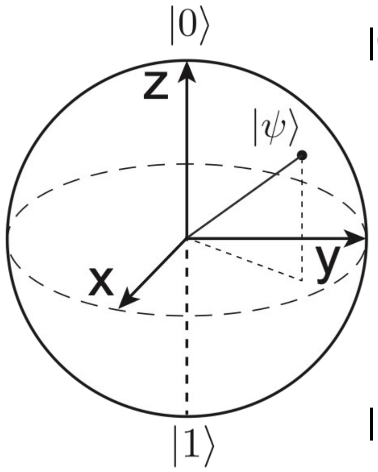
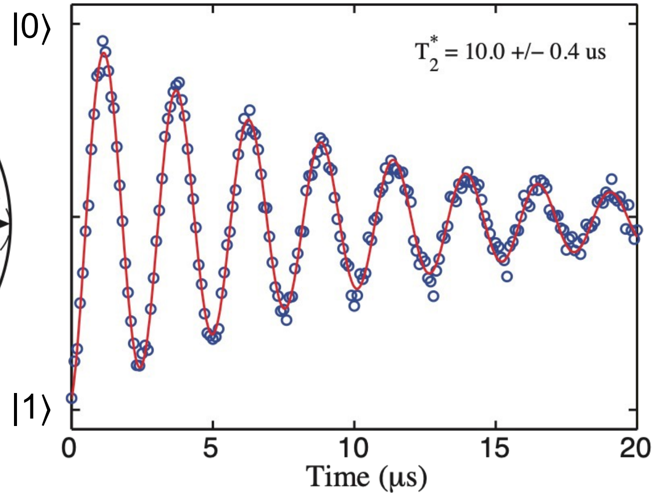
Basics: Decoherence in superconducting qubits







1. Relaxation → *Bit flip errors*

- Qubit decays from state |1⟩ to |0⟩ with characteristic time scale T1
- Causes:
  - Energy loss through interactions with the environment
  - Dielectric loss
  - Non-equilibrium quasiparticles

2. Dephasing → *Phase flip errors*

- Qubit decays from one phase to a mixture of phases with characteristic time scale T2
- Causes:
  - Magnetic flux noise
  - Charge noise
  - Readout cavity photon number fluctuations
  - Non-equilibrium quasiparticles

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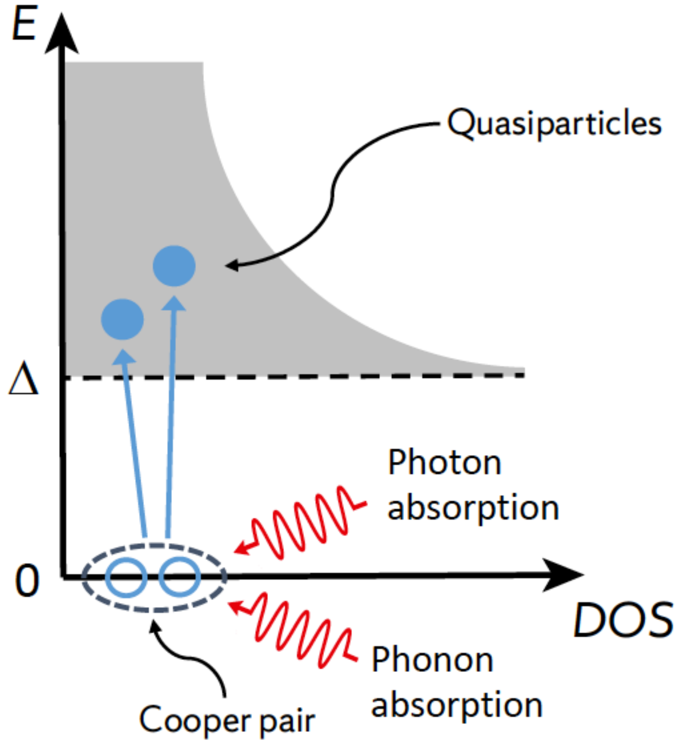
Basics: Non-equilibrium quasiparticles in superconductors



$$x_{qp} = n_{qp}/n_{cp}$$

$$x_{qp}^{eq} = \sqrt{2\pi k_B T/\Delta}\, e^{-\Delta/k_B T}$$

For Al: $\Delta_{\mathrm{Al}}/k_B \approx 2\ \mathrm{K}$

At DR temperatures, expect → $x_{qp}^{eq} \sim 10^{-50}$

Experiments observe → $x_{qp} \sim 10^{-10} - 10^{-6}$

- Causes:
  - Phonon bursts released from high-energy particle impacts: γ-rays, muons
  - Blackbody photons (mm-wave) absorbed directly in superconducting film
  - Resonant absorption of blackbody photons by spurious antenna modes of qubit

Liu +, "Quasiparticle poisoning of superconducting qubits ...", 2022, arXiv:2203.06577

slide credit: Britton Plourde