Superconductor electronic logic family metrics and comparisons

D. Scott Holmes and **George Tzimpragos**
IRDS CEQIP and the University of Michigan
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Superconductor electronic logic family metrics and comparisons

Abstract

Logic families are key to the future of digital superconductor electronics (SCE). Predicting the utility and cost of a given logic family for computing is challenging because logic families must satisfy various functional requirements, operational requirements, and technical requirements. However, common metrics such as throughput, power, area, and yield do not cover the full range of requirements. In this work, we first analyze the shortcomings of common figures of merit, and second, we establish a methodology and set of benchmarks tailored to SCE's target application domains. Lastly, we survey the most prominent superconductor logic families and perform both qualitative and quantitative analysis, where possible.

Presenter: D. Scott Holmes

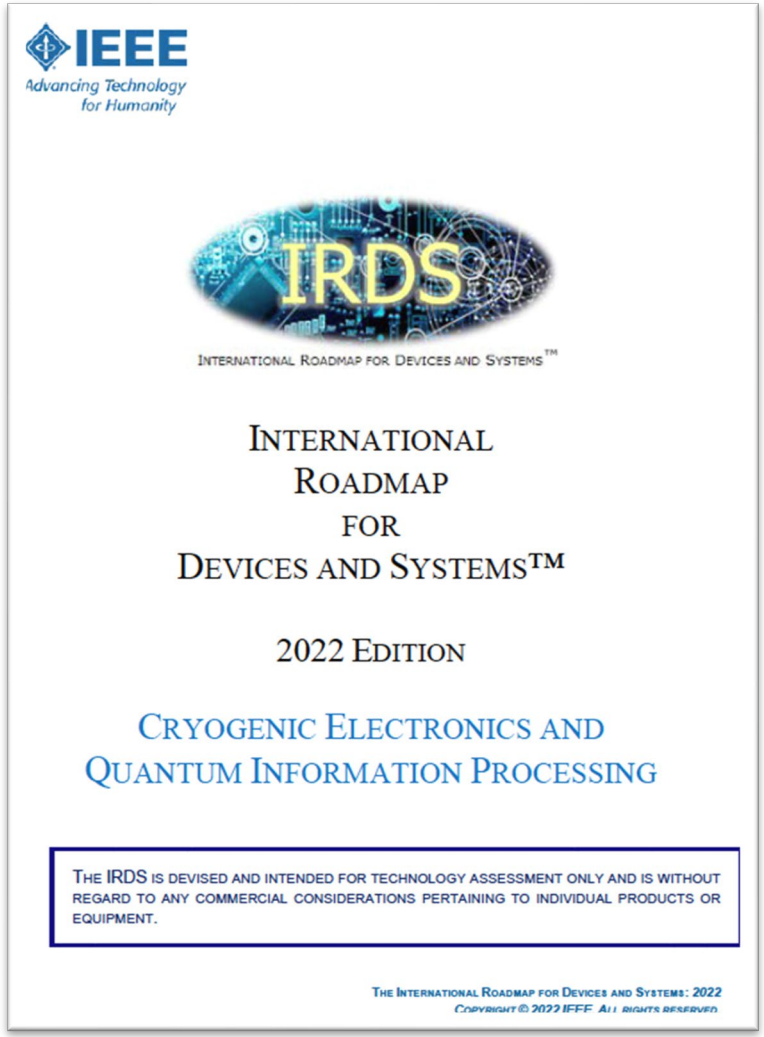
European Conference on Applied Superconductivity

2023 September 3–7, Bologna, Italy
https://eucas2023.esas.org/

2022 IRDS CEQIP summary

- Coverage
  - Superconductor Electronics (SCE)
  - Cryogenic Semiconductor Electronics
  - Quantum Information Processing (QIP)
- Key Messages from the 2022 report
  - SCE: Partial roadmaps
  - QC: Not yet ready for roadmaps
- Summary slides:
  - Difficult Challenges
  - Technology Requirements
  - Potential Solutions
- Updates
  - New Technology Requirements
  - Breakthroughs in Technology, Research
  - New Disruptors
  - Potential Solutions
- Conclusions and Recommendations

Available:
https://irds.ieee.org/editions



Superconductor Digital Logic Families

2022 Summary of current status

Name	*SFQ*	*Power*	*Static Power*	*Dynamic power per switch*	*Trans-formers*	*Clocked Gates*	*JJ count $log_{10}(n)$*
RSFQ: rapid single flux quantum	1	– DC	High	$\alpha I_c \Phi_0 f$	-	Yes	4.4
LR-RSFQ: inductor-resistor RSFQ	1	– DC	Low	$\alpha I_c \Phi_0 f$	-	Yes	1.6
LV-RSFQ: low-voltage RSFQ	1	– DC	Low	$\alpha I_c \Phi_0 f$	-	Yes	3.7
ERSFQ: energy-efficient RSFQ	1	– DC	0 *	$I_b \Phi_0 f$	-	Yes	3.8
eSFQ: efficient SFQ	1	– DC	0 *	$I_b \Phi_0 f$	-	Yes	3.4
Clockless SFQ	1	– DC					2.8
DSFQ: dynamic SFQ	1	– DC	‡	‡	-	Some	0.7
TSFQ: temporal SFQ	1	– DC			-	No	(2.8)
xSFQ: alternating SFQ	2	– DC	‡	‡	-	No	
nTron: nanowire cryotron	1	– DC	~0	varies	-	Yes	1.5
hTron: heater-cryotron nanowire	1	– DC	~0	varies	-	Yes	1.2
HFQ: half flux quantum	0.5	– DC	Low		-	Yes	1.2
SFQ-AC: AC-powered SFQ	1	~ AC	‡	‡	P	Yes	5.9
RQL: reciprocal quantum logic	2	~ AC	~0	$\alpha I_c \Phi_0 f$ 2/3	P, G	Some	4.9
PML: phase mode logic	1	~ AC	~0	$\alpha I_c \Phi_0 f$ /3	P, G	Some	
AQFP: adiabatic quantum flux parametron	-	~ AC	~0	$\alpha I_c \Phi_0 2 f \tau_{sw}/\tau_x$	P, G	Yes	4.3
RQFP: reversible QFP	-	~ AC	~0	$\alpha I_c \Phi_0 2 f \tau_{sw}/\tau_x$	P, G	Yes	1.4

2022 Table CEQIP-4

Superconducting QC Roadmap

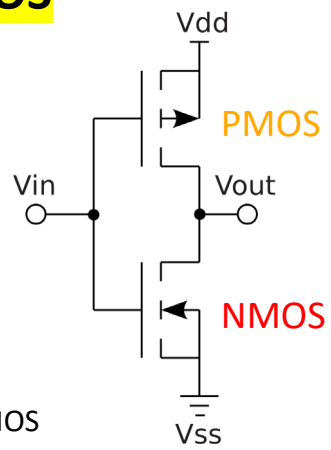
Metric	2020	2022	2024	2026	2028	2030	2032
Qubit growth per year	2×	2×	2×	2×	2×	2×	2×
Qubit count	5.5e+1	2.2e+2	8.8e+2	3.5e+3	1.4e+4	5.6e+4	2.2e+5
Qubit type	Transmon	Transmon	Transmon	Transmon	?	?	?
Qubit lifetime T1, med. [ms]	0.5					10	
2 qubit gate error rate, median (p_2Q)	1.0e-2					1.0e-4	
Gate depth (1/p_2Q)	1.0e+2					1.0e+4	
Error correction code	Surface	Surface	Surface	Surface	Surface	Surface	?
Phys. qubits per logical qubit				1800	1800	1568	1568
Logical qubit count				1	7	35	140
Logical qubit error rate						1.0e-15	
Control type, temp. [K]	CMOS, 300	CMOS, 300	CMOS, 300	CMOS, 4	CMOS, 4	CMOS, 4	SCE, 4
SCE control complexity [JJ]	1.1e+5	4.5e+5	1.8e+6	7.2e+6	2.9e+7	1.2e+8	4.6e+8

In Progress

Searching for a winning combination

Semiconductor logic families

1960s	1980s
ECL	ECL
DTL	DTL
TTL	TTL
NMOS	NMOS
PMOS	PMOS
CMOS	**CMOS**



en.wikipedia.org/wiki/CMOS

Superconductor logic families

2010s	2030s
– RSFQ	
– ERSFQ	
– eSFQ	
– nTron	
– DSFQ	
– HFQ	?
– xSFQ	
– FPL	
~ SFQ-AC	
~ RQL	
~ PML	
~ PCL	
~ AQFP	
~ DQFP	
~ RQFP	
~ SSBF	

Considerations:

- Performance
- Power (Static, Dynamic)
- Supply current
- Cost
  - Design
  - Area
  - Fabrication
  - Yield
  - Packaging
- …

▸ What are the key metrics and limits?

Key Metrics and Limits for SCE logic

1. Power dissipation (static + dynamic)
2. Current supply
3. Area and scalability (problems: transformers, path balancing)
4. Variation sensitivity (process, magnetic field, supply current, trapped flux)
5. Memory (using logic process)
6. Architectural
    1. Composability
    2. Logic depth per clock cycle
    3. Time usage
    4. Performance
7. Cost
    1. Design
    2. Fabrication (includes area, yield, packaging)
    3. Testing
    4. Shielding

2. Power dissipation

(static + dynamic)

Limits:

1. 100 mW/cm^2 in LHe
2. 10 mW/cm^2 on cold head

Best practice for power distribution:

1. No resistors
2. No switching junctions

2. Current Supply

Uses:

1. Junction biasing (waste!)
2. Makeup energy (necessary)

Best practice:

1. AC to SFQ
2. AC

DC Supply Current to Bias JJs

Biasing sets signal flow direction ➔

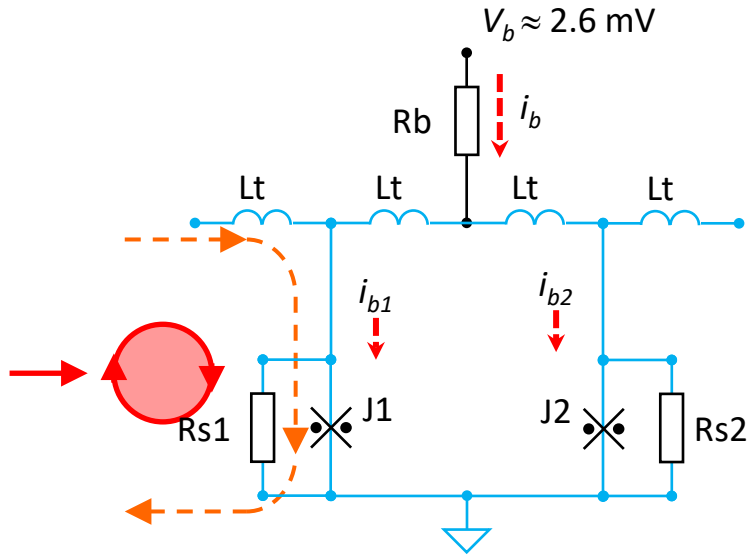
- $I_C \approx 100$ μA (constraints: thermal noise, switching energy)
- $K_0 \approx 0.7$ (bias current ratio, $K_0 \equiv i/I_C$)
- $\alpha \approx 0.5$ (fraction of biased junctions)

- Bias current for 1 million junctions in parallel?

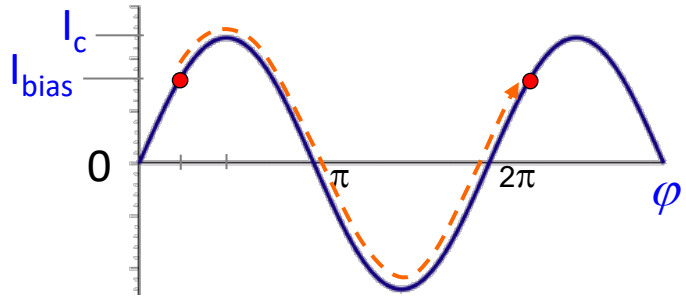
$$I_b = N I_C K_0 \alpha = (1e+6)(100e-6)(0.7)(0.5) = 35 \text{ A}$$

- Way too much current and not nearly enough junctions!

- Traditional DC biasing will not scale.



Junction bias in RSFQ



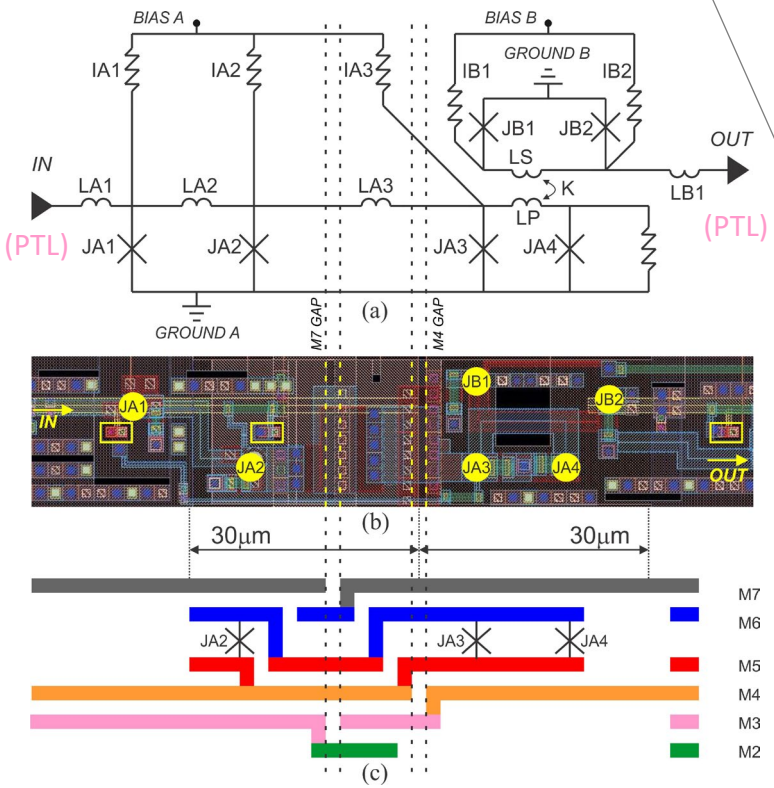
$$i = I_c \sin(\phi)$$

Supply Current: Recycling

DC bias current

- Pass DC bias current through a series of *N* ground plane 'islands'
  - *N* = 16 demonstrated with highly regular circuits (shift registers) [1]
- Advantages
  - *N*× bias current reduction
- Disadvantages
  - Clock, data nets also require separation
  - Area multiplier ≈ 1.5× (??)
  - JJ return current paths can affect margins
  - Complexity of balancing island currents
  - Capacitive coupling between floating islands
  - Ground plane gap shields needed

▸ Seems difficult with limited benefits



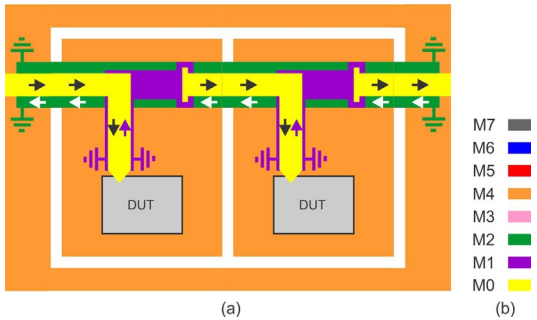


Fig. 1. Grapevine distribution of DC bias currents. [2]

Fig. 2. Driver-receiver pair (DRP) to transfer clock and data pulses between islands. [2]

[1] Semenov+, "Current recycling: New results," 2019, doi: 10.1109/TASC.2019.2904961

[2] Shukla+, "Serial biasing technique for electronic design automation in RSFQ circuits," 2022, doi: 10.1109/TASC.2022.3214767

Supply Current: AC/SFQ Conversion

- Better: Convert AC to SFQ (not DC) on chip using rectifiers
- Best used with logic cells that require AC or **no** bias current
- Advantages
  - AC supply to converters in series, so can supply more cells (≈ 1000× ?)
- Disadvantages
  - Complexity, area overhead factor ≈ 2× (?)
  - Transformers don't scale well
  - $f_{AC} > f_{clock}$ for best energy efficiency
  - Need to design more logic cells that use AC or no bias current

▸ Deserves further investigation

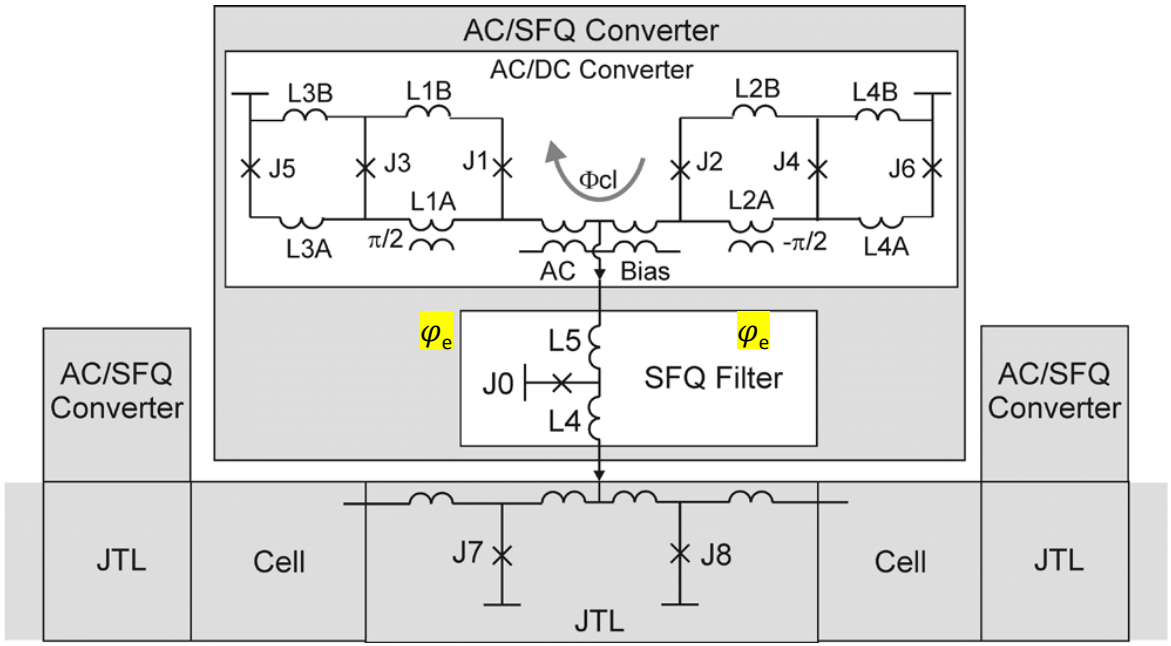


Fig. 3a. AC/SFQ converter supplying a JTL. [1]

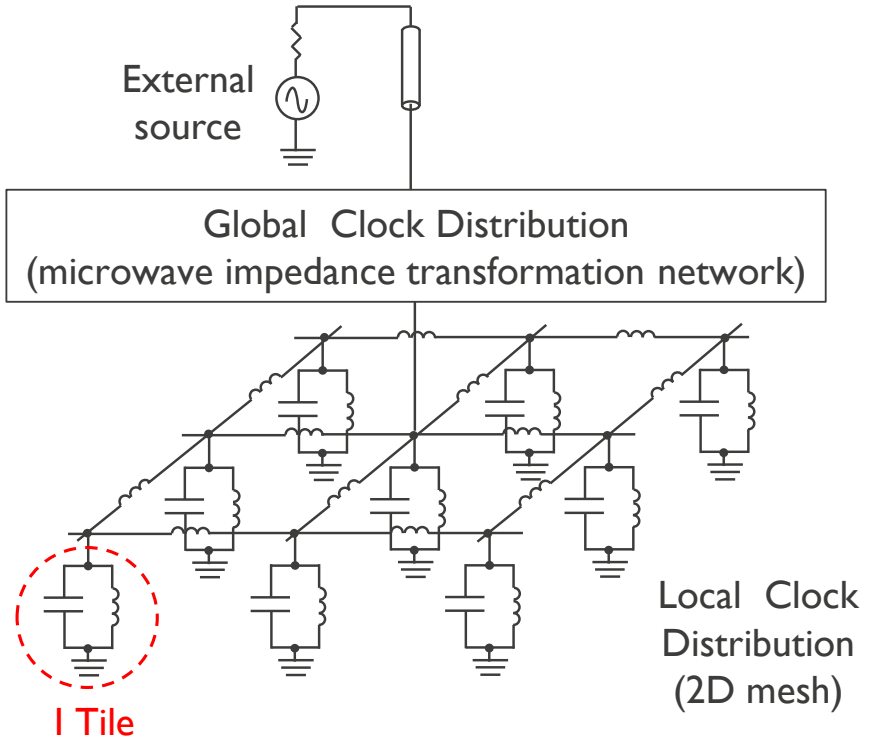
[1] Semenov+, 2021, doi: 10.1109/TASC.2021.3067231

▸ EUCAS 2023 Sep 7, **4-ES-SL-01**, Mukhanov

AC Power Distribution

Design concept for large-scale clock distribution

- Local storage of power and clock signal in high-Q LC-resonators
  - 1 resonator per tile
- 2D mesh of LC resonators has a zero-order mode
  - Clock signal distribution over large area with only small amplitude and phase variation
- 30 GHz design with 400 M taps/cm^2



A. Herr +, "Scaling NbTiN-based ac-powered Josephson digital to 400M devices/cm^2," 2023, arXiv.2303.16792

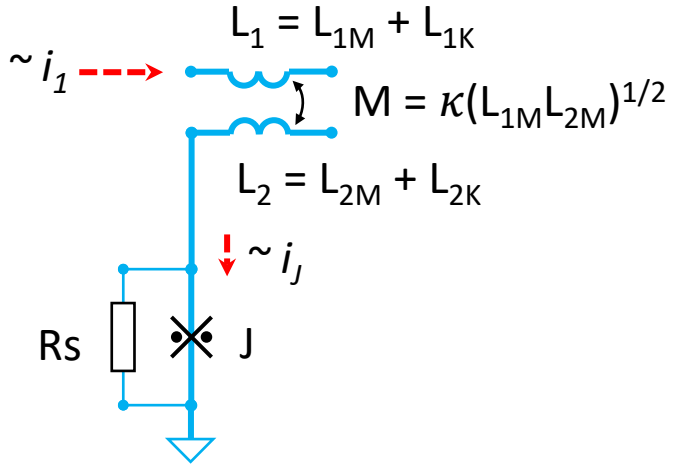
AC Power Scaling

Transformers or capacitors?

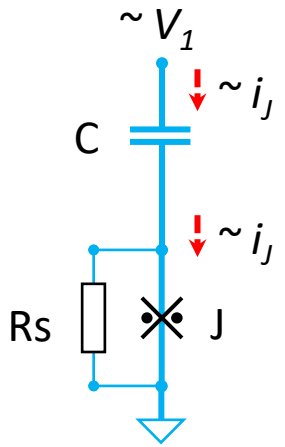
- Transformers [1]
  - Current required for JJ biasing does not scale
  - Wire size limited by wire J_C
  - Voltage also increases due to kinetic inductance at small sizes

$$i_1 \propto \frac{i_J}{M} \qquad V_1 = L\frac{di_1}{dt} \propto (L_{1M} + L_{1K}) f i_J$$

- Capacitors [2]
  - Current required for JJ biasing does not scale
  - But current is the same on both sides
  - Current increases with frequency



Transformer bias supply



$$I_J = C\frac{dV}{dt} \propto CfV_1$$

Capacitor bias supply

[1] S. Tolpygo, 2023, doi: 10.1109/TASC.2022.3230373

[2] A. Herr +, 2023, arXiv.2303.16792

3. Area and Scalability

Checks:

1. Inductors
2. Transformers
3. Passive transmission line (PTL) width
4. Josephson junctions
    1. Size and scalabilty
    2. Types (0-JJ, pi-JJ, phi-JJ)
    3. Self-shunted
    4. Unshunted

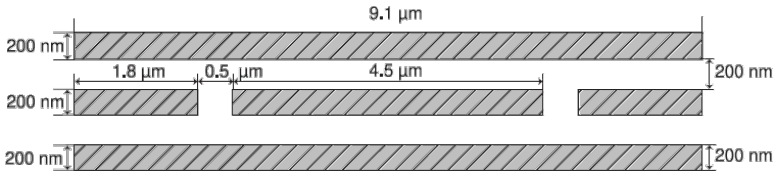
Best practices:

1. Mix of JTLs, PTLs
2. No shunt resistors

Passive transmission lines (PTL)

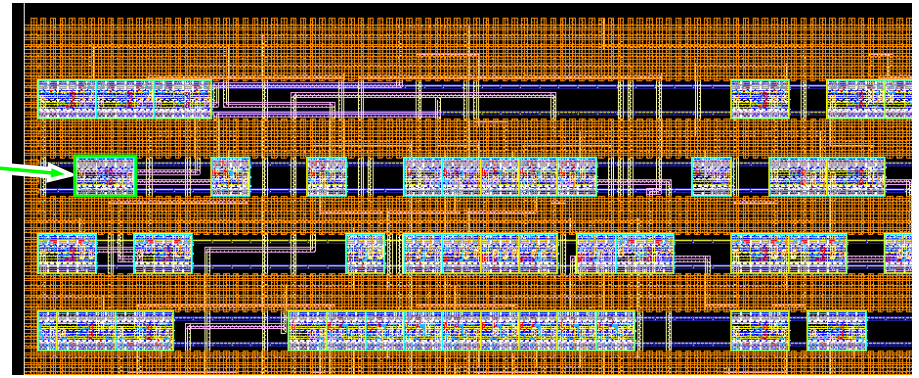
Important interconnects

- PTL width (~ 4 μm) is a major obstacle to scaling
  - JJs are low impedance drivers
  - Reducing the PTL width increases impedance, which causes reflections due to impedance mismatch
  - Reducing JJ Ic increases impedance, but reduces pulse energy
- Using only PTLs for routing requires too much area
- Additional PTL layers would increase area density but require +2 metal layers each



PTL cross section

Herbst +, 2020, doi: 10.1109/TASC.2020.3006988



AMD2901 4-bit processor design with 16,840 gates (upper left portion of overall layout)

Placed and routed in Synopsys **Fusion Compiler** (FC) and viewed in Custom Compiler

4. Variation sensitivity

Checks:

1. Process
2. Supply current or power
3. Trapped flux, Magnetic field

Best practices:

1. No need to match multiple devices (e.g. JJ and inductors)
2. No inductors or transformers
3. Phase shift devices (?)
4. Logic tolerant of variations (?)

Phase Engineering: φ Junctions

One Junction to rule them all?

- Storing element compaction [1]

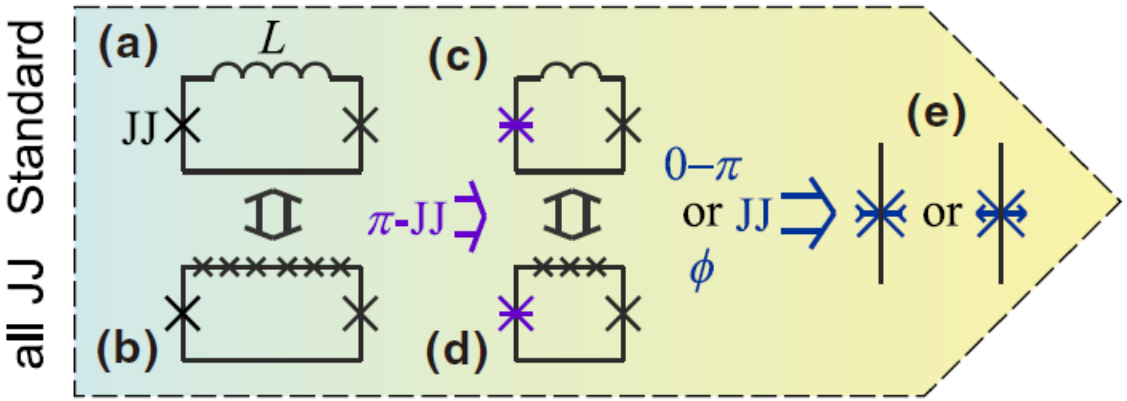


Fig. 1

- Question:
  - Can the devices be made?

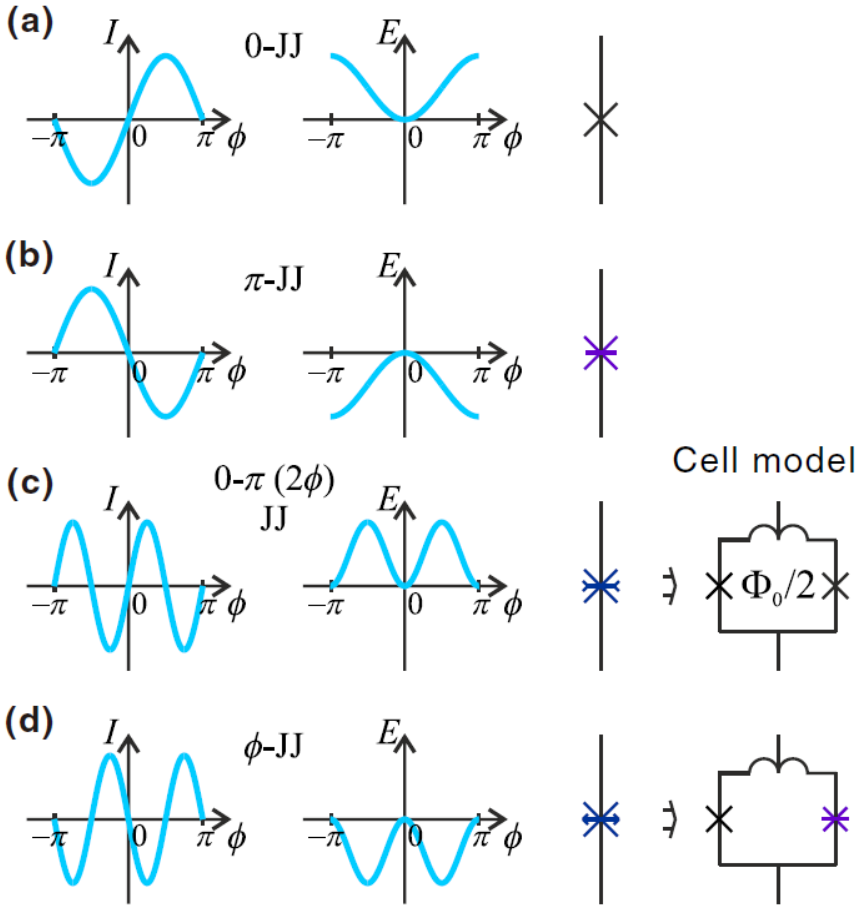


Fig. 2

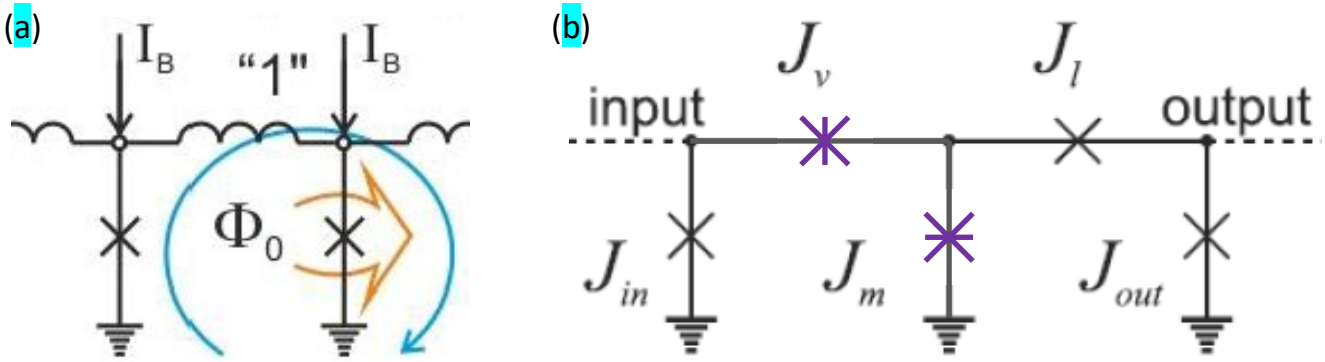
[1] I. I. Soloviev, "Superconducting circuits without inductors based on bistable Josephson junctions," 2021, doi: 10.1103/PhysRevApplied.16.014052

"Inductorless" circuits with small mutual inductances

Non-traditional Josephson junctions to replace inductors, reduce JJ count

- Junction types
  - 0 junctions (SIS), switching
  - **0 junction stacks** (SNsNsNS)
  - **π junctions** (SFS)
  - **ϕ junctions** [1], [3]

- Questions:
  - Can the devices be made?
  - And with sufficiently small parameter variations (I_c, L)?



[1] (a) JTL with inductors, (b) JTL with magnetic junctions

[1] Soloviev +, "Superconducting circuits without inductors based on bistable Josephson junctions," 2021, doi: 10.1103/PhysRevApplied.16.014052.
[2] Maksimovskaya +, "Phase logic based on π Josephson junctions," 2022, doi: 10.1134/S0021364022600884.
[3] Bakurskiy +, "Compact Josephson ϕ-junctions," 2018, doi: 10.1007/978-3-319-90481-8_3.

5. Memory

Metrics:

1. Capacity
2. Density
3. Time for read/write
4. Energy for read/write

Best practices:

1. (?)

6. Architectural

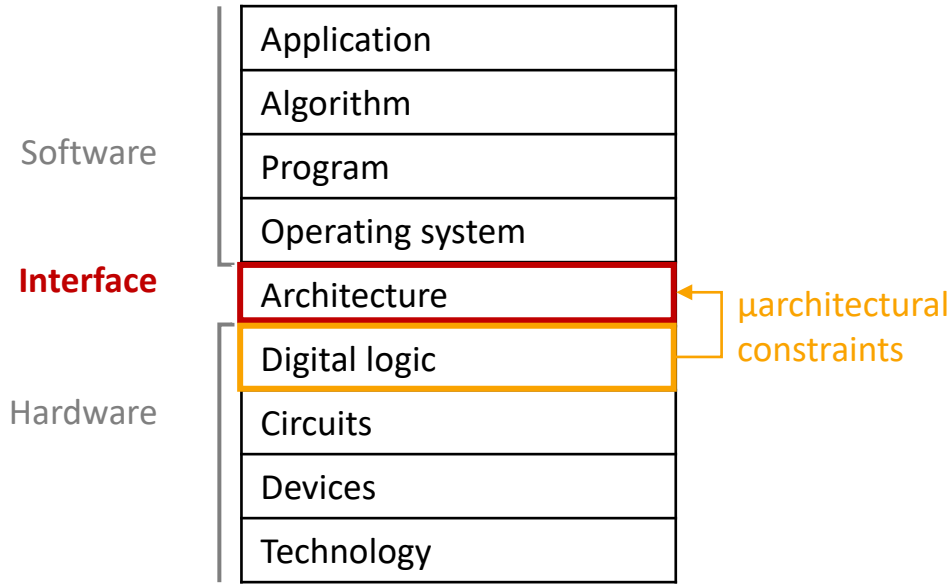
Goal: Add metrics for architectural properties

Metrics:

1. Logic depth per clock cycle
2. Time usage (?)
3. Performance (alone or per unit area, power, energy, or cost)
4. Composability

Best practices:

1. AC clocking
2. Clock reduction or elimination
    1. Macro blocks or cell-abutment logic
    2. Self-timed or asynchronous
3. Efficient data representation
4. Neuromorphic circuits (?)



Levels of abstraction

AC Clocking

Use AC power as the clock

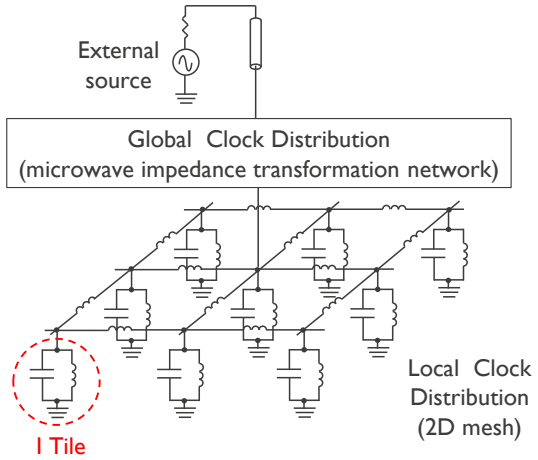
- AQFP (most established)
  - **Advantages**: JJs are all the same size and small (50 μA), energy efficient, good margins, majority logic
  - **Disadvantages**: large area, transformers, clocked gates, memory (?), majority logic
- Reciprocal quantum logic (RQL)
  - **Advantages**: Few JJs per logic gate, good margins, proven
  - **Disadvantages**: transformers, clock frequency limits, EDA tool support (?), controlled by Northrop Grumman
- **Pulse conserving logic (PCL)**
  - 12 levels of logic at 30 GHz
  - OMA3 gate (OR3/MAJ3/AND3)

New!

[1] Q. Herr +, 2023, doi: 10.1063/5.0148235

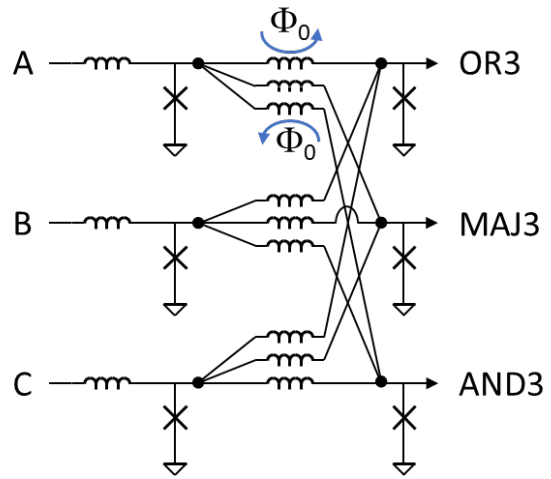
Design concept for large scale clock distribution
2D array of tightly coupled local, lumped LC resonators

- Local storage of power and clock signal in high-Q LC-resonators
  - 1 resonator/tile (1 tile ~5x5 μm²)
- 2D mesh of LC resonators has a zero-order mode
  - Clock signal distribution over large area with only small amplitude and phase variation



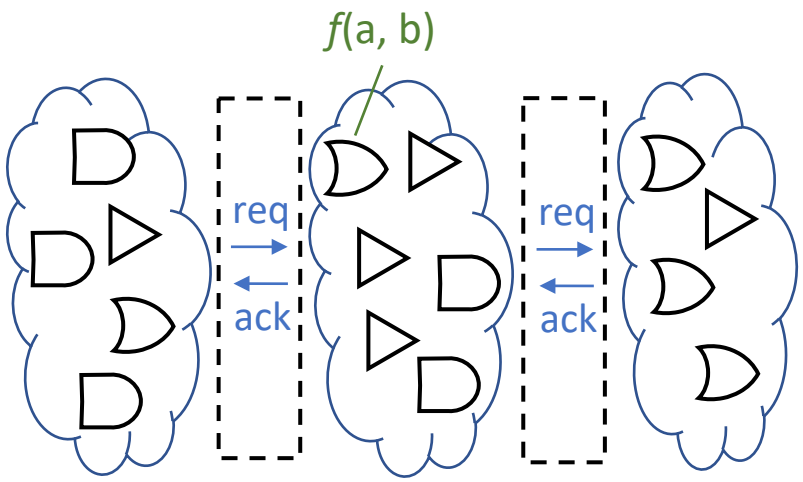
- 30 GHz design with 400 M taps/cm²

[2] A. Herr +, 2023, arXiv.2303.16792



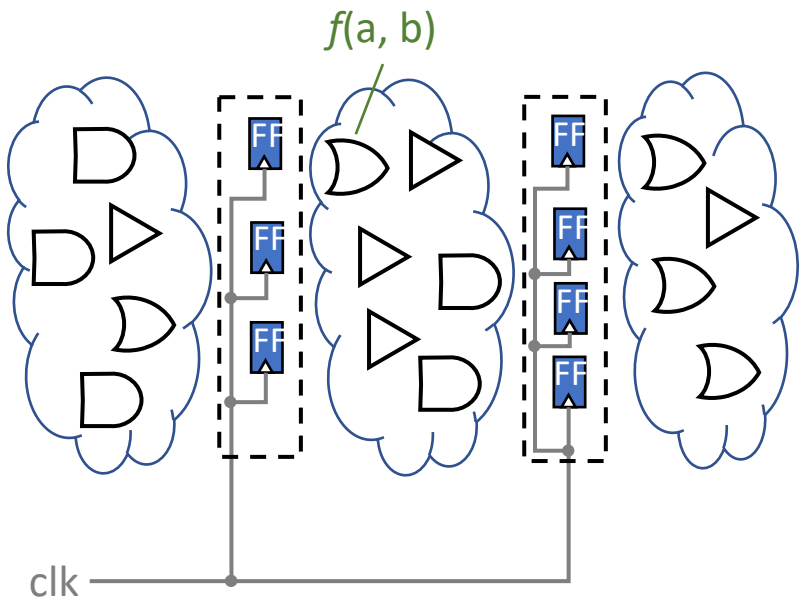
Different clocking approaches

Asynchronous



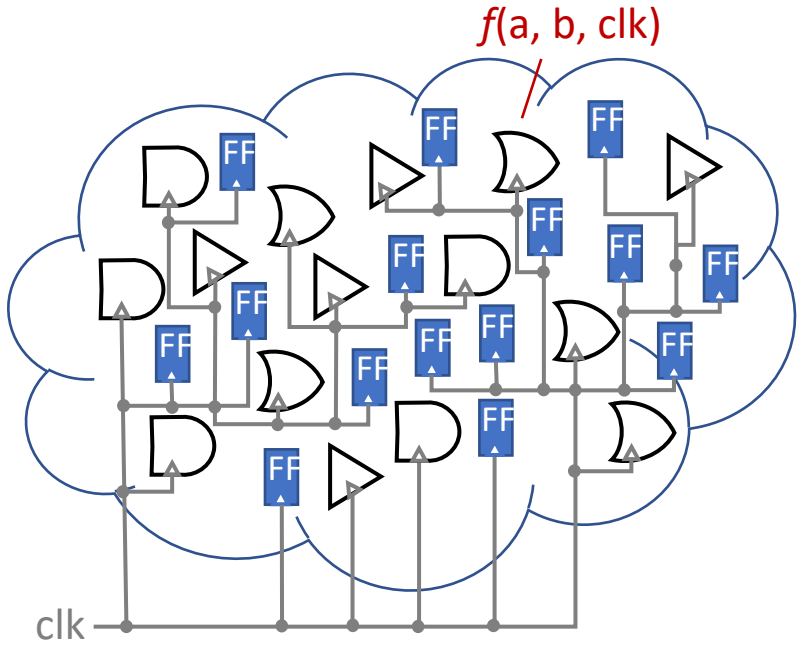
Flexible pipelining

Regular Synchronous



Flexible pipelining

Fully Synchronous



Fixed gate-level pipelining

Pipelining in traditional SFQs

Overhead multiplies the cost of clocking!

the good

~ 20-30 GHz

Ishida+, "32 GHz 6.5 mW, gate-level-pipelined 4-bit processor ...", 2020, doi: 10.1109/VLSICircuits18222.2020.9162826

Inverse Performance

TPI (Time/Instruction) = CPI x Cycle time

technology-dependent
µarchitecture-dependent

workload-dependent (% of p. hazards)
µarchitecture-dependent (# pipeline stages, etc.)

the bad

pipeline stages (p)= # gates on the critical path ($N_{logic\_gates\_cp}$)

RISC-V RV32I

- total # logic gates = 10,000
- # gates on the critical path = ***150***

10x

Cell count

$$N_{cells} = N_{l\_gates} + N_{FFs} + N_{splitters}$$
$$= N_{l\_gates} + (N_{l\_gates} \times p^{\eta}) + (N_{l\_gates} + (N_{l\_gates} \times p^{\eta}))$$

bias current ↑

Energy

EPI (Energy/Instruction) = $E_{dyn} + E_{stat}$

$$= ((N_{cells} \times E_{cell_{avg}} \times af \times CPI) \times o_{wires}) + E_{stat}$$
$$= ((N_{cells} \times E_{cell_{avg}} \times af \times CPI) \times o_{wires}) + (E_{dyn} \times o_{stat})$$

and the ugly

Varies between SFQ families

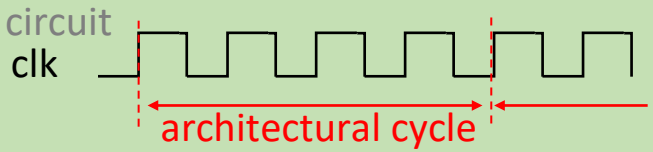
JJs per logic gate varies between RSFQ, LR-SFQ, ERSFQ, eSFQ

Mukhanov, 2011, doi: 10.1109/TASC.2010.2096792

Mukhanov, 2011, doi: 10.1109/TASC.2010.2096792

Architectural approaches: there are only 3!

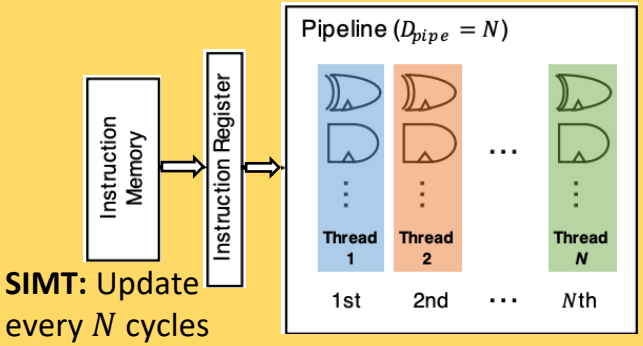
Fast (circuit) clock vs slow (architecture) clock



- MANA is a **two-stage pipeline** from a pure computer architecture point of view.
- This 1st stage has a latency of **1 cycle**.
- This 2nd stage has a total latency of **26 cycles**.
- The 2nd stage of MANA can accommodate **26 instructions in-flight** although MANA will only issue **a maximum of 4 instructions** successively

Ayala+, "MANA: A monolithic adiabatic integration architecture microprocessor ...", 2021, doi: 10.1109/JSSC.2020.3041338

Multi-threading



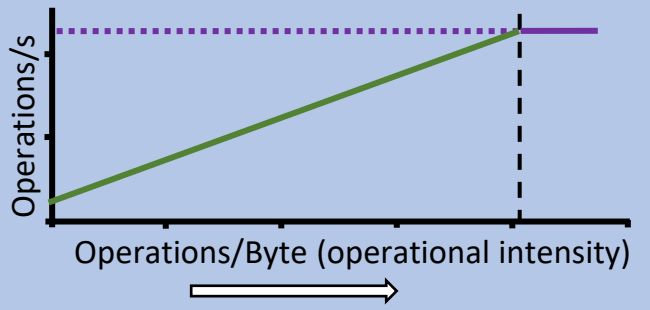
SIMT: Update every N cycles

- SFQ-GLPI consists of **24 pipeline stages**.
- We reduced the number of **threads to 12** because the chip **area was limited**.
- Although such degradation makes the total area required for implementing Register File (RF) half, it also **halves the peak performance.**

Ishida+, "32 GHz 6.5 mW, gate-level-pipelined 4-bit processor ...", 2020, doi: 10.1109/VLSICircuits18222.2020.9162826

Increase operational intensity

Roofline model:



- SuperNPU increases the operational intensity by assigning **more registers to each processing element (PE)**.
- Operational intensity is not only μarchitecture- but also **algorithm-dependent.**

Williams+, "Roofline: an insightful visual performance model for multicore architectures", 2009, doi: 10.1145/1498765.1498785

Ishida+, "SuperNPU: An extremely fast neural processing unit ...", 2020, doi: 10.1109/MICRO50266.2020.00018

7. Cost

Metrics:

1. Design
2. Fabrication (includes area, yield, packaging)
3. Testing
4. Shielding

M. Zabihi +, "A life-cycle energy and inventory analysis of adiabatic quantum-flux-parametron circuits," 2023-07-22, arXiv.2307.12216

Table I: Comparison of CMOS and AQFP RISC-V Processors

Processor	Manufacturing Energy	Assembly Energy	Use Phase Energy	Total Energy	Overall Improvement
CMOS RISC-V	0.17 KWh	0.08 KWh	665.23 KWh	665.48 KWh	237X (with cooling 205X)
AQFP RISC-V	1.61 KWh	1.19 KWh	0.001 KWh (with cooling 0.42 KWh)	2.81 KWh (with cooling 3.23 KWh)	

Key Metrics and Limits for SCE logic

1. Power dissipation (static + dynamic)
2. Current supply
3. Area and scalability (problems: transformers, path balancing)
4. Variation sensitivity (process, magnetic field, supply current, trapped flux)
5. Memory (using logic process)
6. Architectural
    1. Composability
    2. Logic depth per clock cycle
    3. Time usage
    4. Performance
7. Cost
    1. Design
    2. Fabrication (includes area, yield, packaging)
    3. Testing
    4. Shielding

Superconductor Digital Logic Families

Name	Crit. (I, V)	Power	SFQ	Critical value, typical at 4 K	Devices per unit current [A^{-1}]	Static Power	E switch [aJ]	Devices	Switch count	IC area	X-formers	Clocked	JJ count
RSFQ: rapid single flux quantum	I	dc –	1	1.5E-04	2.8E+4	High	0.1	JLR	x1	x1	☐	■	2.5E+4
LR-RSFQ: inductor-resistor RSFQ	I	dc –	1	5.0E-05	2.8E+4	Low	0.1	JLR	x1	x1.1	☐	■	3.6E+1
LV-RSFQ: low-voltage RSFQ	I	dc –	1	5.0E-05	2.8E+4	Low	0.1	JLR	x1	x1	☐	■	4.9E+3
ERSFQ: energy-efficient RSFQ	I	dc –	1	1.5E-04	2.8E+4	0 *	0.15	JLR	x1.4	x1.4	☐	■	6.8E+3
eSFQ: efficient SFQ	I	dc –	1	1.5E-04	2.8E+4	0 *	0.15	JLR	x1.4	x1	☐	■	2.6E+3
Self-timed SFQ	I	dc –	1	1.5E-04	2.8E+4			JLR	x4	x4			6.0E+2
DSFQ: dynamic SFQ	I	dc –	1	9.9E-05	2.8E+4	‡		JLR			☐	◘	5.0E+0
TSFQ: temporal SFQ	I	dc –	1	1.0E-04	2.8E+4			JLR			☐	☐	
xSFQ: alternating SFQ	I	dc –	2	1.0E-04	2.8E+4	‡		JLR			☐	☐	
HFQ: half flux quantum	I	dc –	0.5	1.8E-04	8.5E+4	Low	0.05	JLP	x1.5		☐	■	3.2E+01
nTron: nanowire cryotron	I	dc –	-	1.8E-04	1.1E+4	High	1	LN			☐	■	1.6E+01
hTron: heater-cryotron nanowire	I	dc –	-	5.0E-05	>1E+9	0	1000	LNR			☐	■	1.6E+01
SFQ-AC: AC-powered SFQ	I	ac ~	1	1.0E-04	>1E+8	‡		JLRT			◘	■	8.1E+05
RQL: reciprocal quantum logic	I	ac ~	2	5.0E-05	>1E+8	Low	0.07	JLRT	x0.5		■	◘	7.3E+04
PML: phase mode logic	I	ac ~	1	5.0E-05	>1E+8	Low	0.04	JLRT			■	◘	
PCL: pulse conserving logic	I	ac ~	1	5.0E-05	>1E+8	~0		CJLRT			◘	☐	
AQFP: adiabatic quantum flux parametron	I	ac ~	-	5.0E-05	>1E+8	~0	0.002	JLRT			■	■	2.1E+4
RQFP: reversible QFP	I	ac ~	-	5.0E-05	>1E+8	~0	~0	JLRT			■	■	2.8E+1
QPSJ: quantum phase slip junctions	V	dc –	-		>1E+9	~0	0.0001	CQ	x1		☐	■	2.0E+0

(Draft) 2023 Table CEQIP-4

Quantum phase-slip junctions (QPSJs)

Voltage controlled devices might interface better with semiconductor electronics

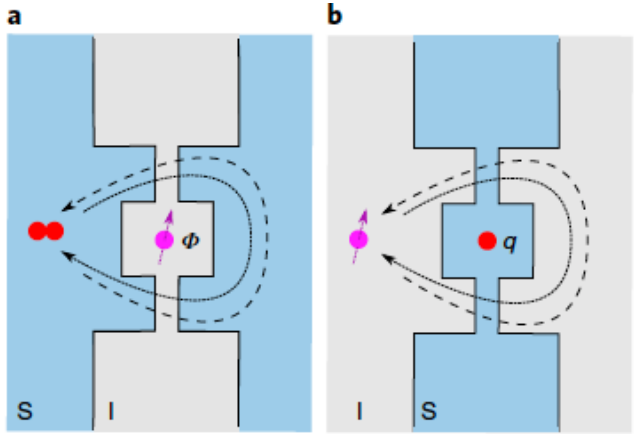
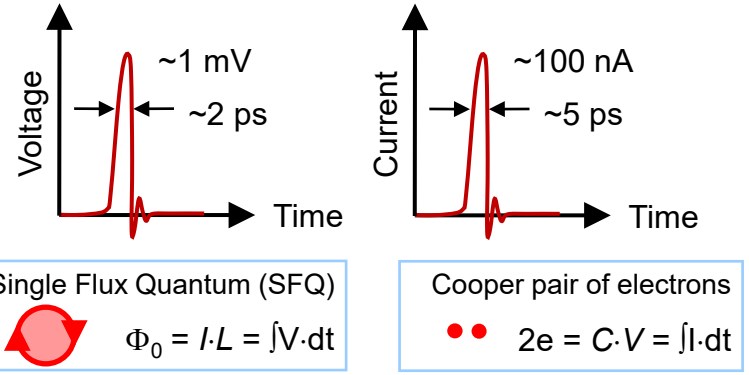


Fig. 1. SQUIDs using (a) JJs, (b) QPSJs [1]



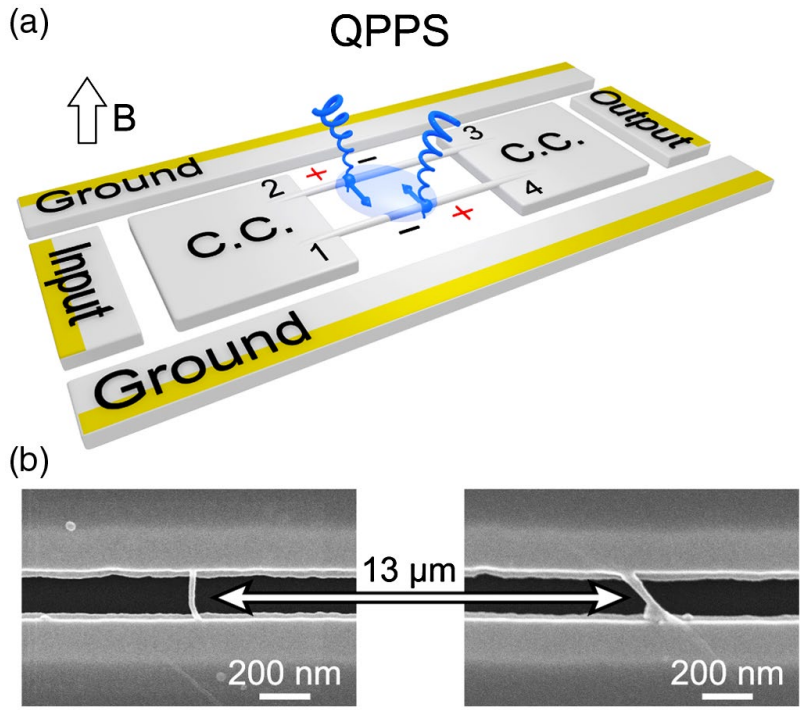


Fig. 2. MoGe nanowire QPSJs [2]

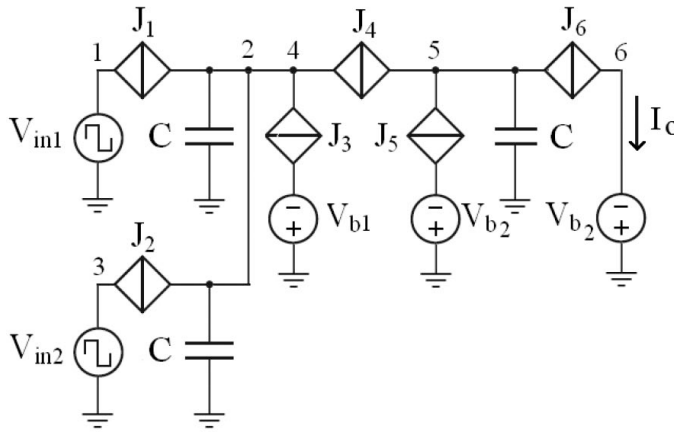


Fig. 3. Memoryless OR gate [3]

- Demonstration needed!

[1] de Graaf +, 2018, doi: 10.1038/s41567-018-0097-9
[2] Belkin +, 2015, doi: 10.1103/PhysRevX.5.021023
[3] Malekpoor +, 2021, doi: 10.1109/TASC.2021.3121344

Backup

2023 CEQIP Members

Name	Area	Organization	Region
Byun, Ilkwon	Cryo-Semi, QIP-QC	Seoul National University, Korea	Asia
Cuthbert, Michael	Cryo, QIP	National Quantum Computing Centre, UK	Europe
DeBenedictis, Erik	QIP-QC	Zettaflops, USA	Americas
Delfanazari, Kaveh	QIP-QC	University of Glasgow, UK	Europe
Fagaly, Bob	SCE-App	Honeywell (retired), USA	Americas
Fagas, Giorgios	QIP	Tyndall National Institute, Ireland	Europe
Febvre, Pascal	SCE-Fab	Université Savoie Mont Blanc, France	Europe
Filippov, Timur	SCE-Log	Hypres, USA	Americas
Fourie, Coenrad	SCE-EDA	Stellenbosch University, South Africa	Africa
Frank, Mike	SCE-Log, -Rmap	Sandia National Laboratories, USA	Americas
Gupta, Deep	SCE, Cryo-Semi	SEACORP, USA	Americas
Herr, Anna	SCE	IMEC, Belgium	Europe
Herr, Quentin	SCE	IMEC, USA	Americas
Holmes, D Scott [Chair]	SCE, Cryo-Semi, QIP	Booz Allen Hamilton, USA	Americas
Humble, Travis	QIP-QC	Oak Ridge National Laboratory, USA	Americas
Leese de Escobar, Anna	SCE-App, -Bench	Laconic, USA	Americas
Min, Dongmoon	Cryo-Semi, QIP-QC	Seoul National University, Korea	Asia
Mueller, Peter	QIP-QC-SC	IBM Zürich, Switzerland	Europe
Mukhanov, Oleg	QIP-QC, SCE-Log	Seeqc, USA	Americas
Nemoto, Kae	QIP	The National Institute of Informatics (NII), Japan	Asia
Papa Rao, Satyavolu	SCE-Fab, QIP	SUNY Polytechnic, USA	Americas
Pelucchi, Emanuele	QIP-QC	Tyndall National Institute, Ireland	Europe
Plourde, Britton	QIP	Syracuse University, USA	Americas
Soloviev, Igor	SCE	Lomonosov Moscow State University, Russia	Europe
Tzimpragos, George	SCE-Logic, -Metrics, -Rmap	University of Michigan, USA	Americas
Weides, Martin	SCE, QIP	University of Glasgow, UK	Europe
Yoshikawa, Noboyuki	SCE-Log, -Bench	Yokohama National University, Japan	Asia
You, Lixing	SCE	SIMIT, CAS, China	Asia

Additions for 2023

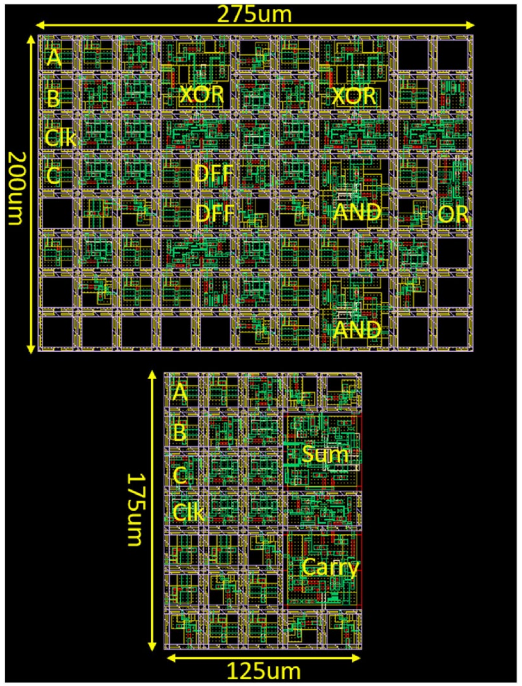
13: Americas
10: Europe + Africa
5: Asia
==========
28 total

Macro blocks or cell-abutment logic

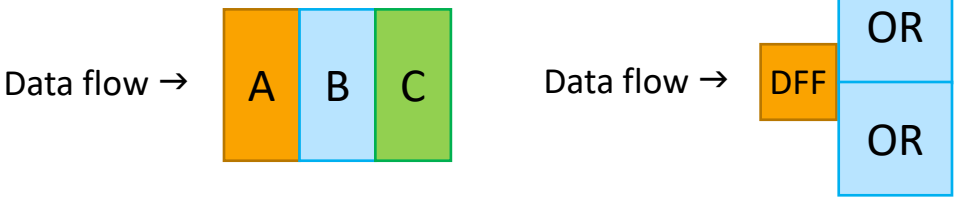
- **Macro blocks** to perform complex functions
  - Smaller, better performance
  - Licensed as intellectual property (IP) blocks
  - We need more of these!

2.5x area reduction: 8-bit multipliers using standard RSFQ gates and single-stage complex RSFQ gates

Cong +, 2021, doi: 10.1109/TASC.2021.3091963

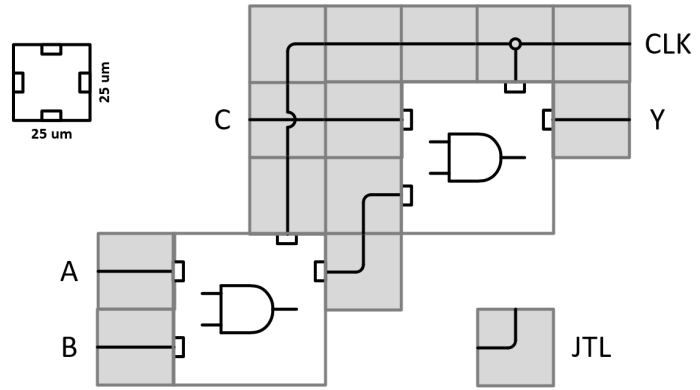


- **Cell abutment logic**
  - Cells connect directly, like LEGO blocks
  - Blocks can contain JTLs or PTLs
  - Problem: EDA tools do not currently support abutment



Volk +, 2023, 10.1109/TASC.2023.3256797

Cell abutment strategy



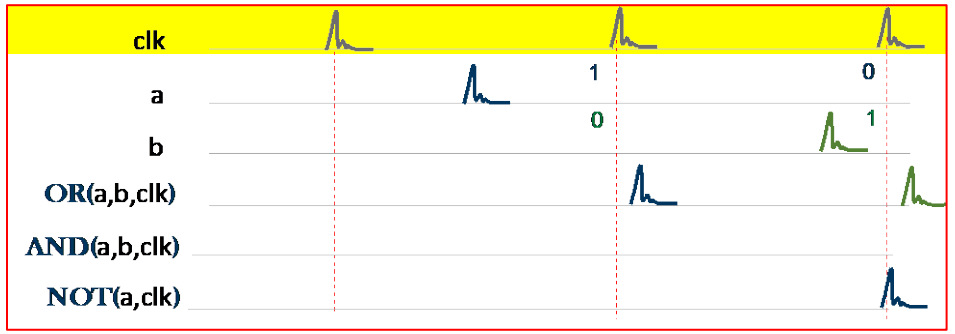
Clock Reduction or Elimination

Overhead multiplies the cost of clocking!

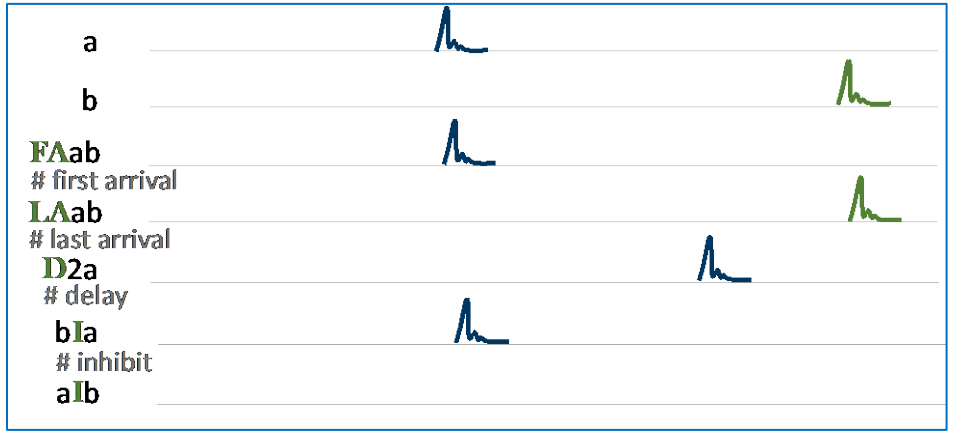
- Bias current overhead estimates **per clocked gate**:
  - ≈ 1.5× (?) for clocking (splitters, mostly)
  - ≈ 4× (?) for path balancing (superlinear)
  - ≈ 20× (?) for unused clock time (allowing for jitter, long lines, pipeline hazards, etc.)
  - ≈ 1.5× (?) for higher fraction of JJs that switch
- ≈ 180× (?) total

▸ Reduce or eliminate clocked cells

Clocked SFQ [1]



Temporal SFQ [1]



[1] Volk, "Circuit Abstractions for Low-Cost Fan-Out," ISCA, 2022

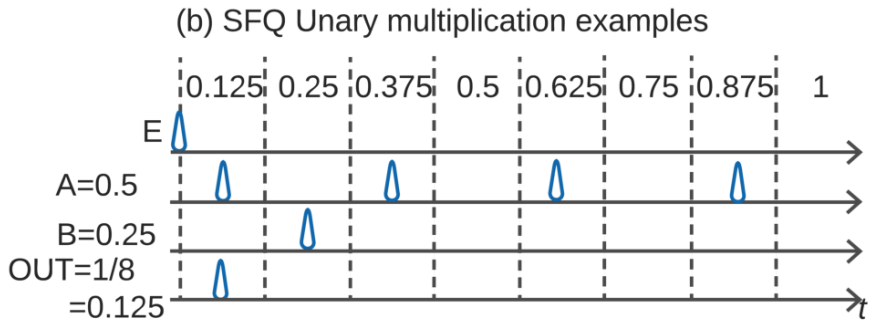
[2] Tzimpragos +, 2020, doi: 10.1145/3373376.3378517

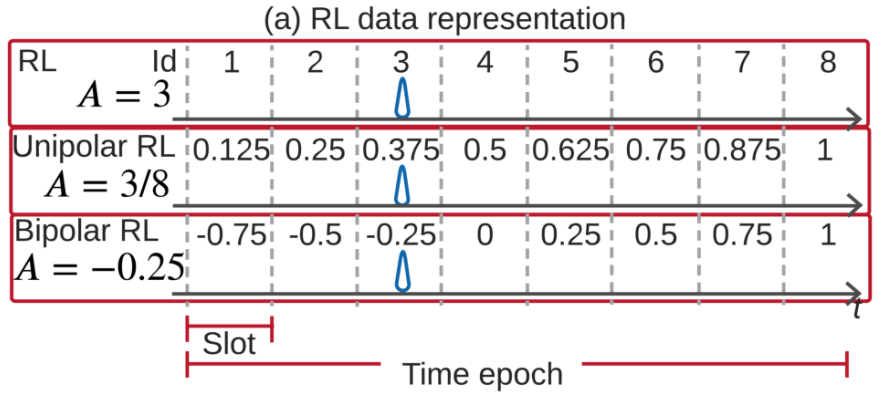
[3] Tzimpragos +, 2021, doi: 10.1109/ISCA52012.2021.00057

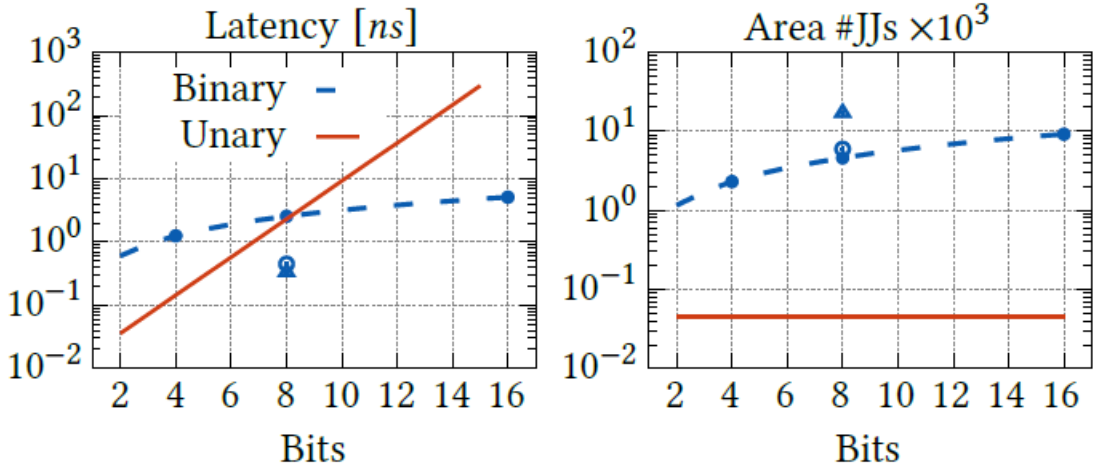
Data representation

"0" and "1" are not the only way

- Race logic (RL) represents data in time
- Time slots within a clock period can be used to represent information and perform computations
  - Unary SFQ is a combination of pulse-stream arithmetic and race logic
- Benefits can include greatly reduced circuit area







Multiplier circuit Latency and area comparison [1] Fig. 4

[1] Gonzalez-Guerrero +, 2022, doi: 10.1145/3503222.3507765

Neuromorphic Circuits using Superconductor Electronics

A more natural fit?

- Characteristics
  - Natural spiking behavior of Josephson junctions
  - Pulses travel on striplines without the RC time constants that typically hinder spike-based computing
  - Possibly tolerant to variations in component parameter values
- Needed:
  - Design methodology
  - Demonstrations at larger scale

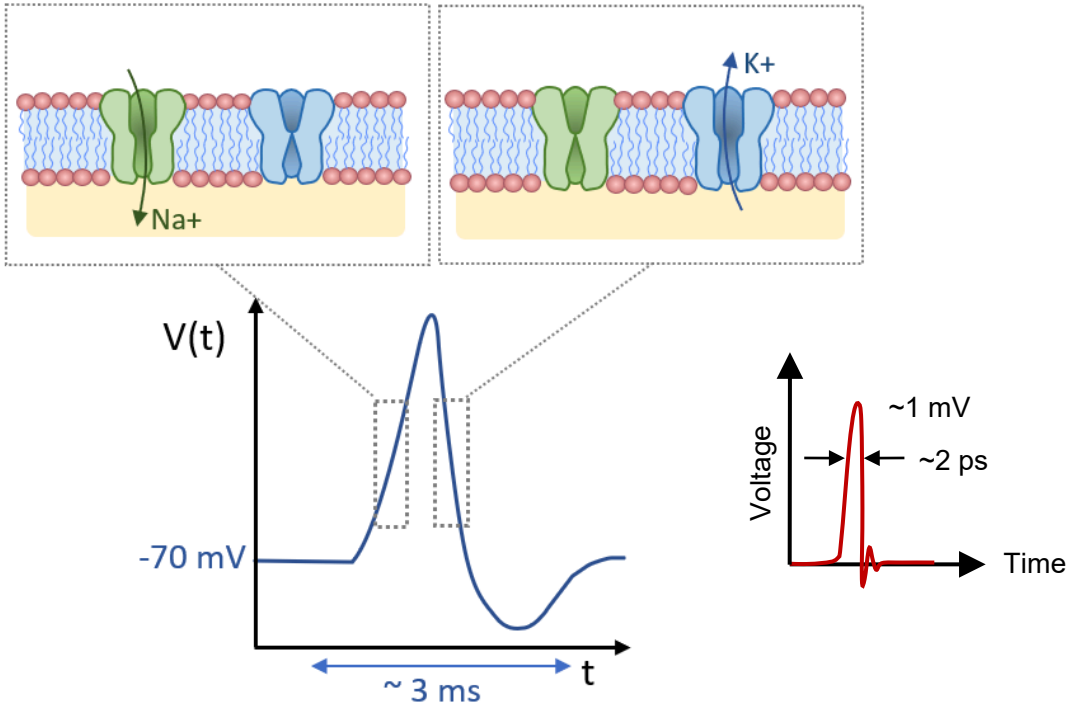


Fig. 3a. Spiking in biological neurons [1]

[1] Schneider +, "**Supermind**: a survey of the potential of superconducting electronics for neuromorphic computing," 2022, doi: 10.1088/1361-6668/ac4cd2