Superconductor electronic logic family metrics and comparisons

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IRDS CEQIP and the University of Michigan
2023-09-07 EUCAS 4-ES-SL-02I
Superconductor electronic logic family metrics and comparisons

Abstract

Logic families are key to the future of digital superconductor electronics (SCE). Predicting the utility and cost of a given logic family for computing is challenging because logic families must satisfy various functional requirements, operational requirements, and technical requirements. However, common metrics such as throughput, power, area, and yield do not cover the full range of requirements. In this work, we first analyze the shortcomings of common figures of merit, and second, we establish a methodology and set of benchmarks tailored to SCE's target application domains. Lastly, we survey the most prominent superconductor logic families and perform both qualitative and quantitative analysis, where possible.

Presenter: D. Scott Holmes

European Conference on Applied Superconductivity

2023 September 3–7, Bologna, Italy

https://eucas2023.esas.org/
2022 IRDS CEQIP summary

• Coverage
  - Superconductor Electronics (SCE)
  - Cryogenic Semiconductor Electronics
  - Quantum Information Processing (QIP)

• Key Messages from the 2022 report
  - SCE: Partial roadmaps
  - QC: Not yet ready for roadmaps

• Summary slides:
  - Difficult Challenges
  - Technology Requirements
  - Potential Solutions

• Updates
  - New Technology Requirements
  - Breakthroughs in Technology, Research
  - New Disruptors
  - Potential Solutions

• Conclusions and Recommendations

Available:
https://irds.ieee.org/editions
Superconductor Digital Logic Families

2022 Summary of current status

<table>
<thead>
<tr>
<th>Name</th>
<th>SFQ</th>
<th>Power</th>
<th>Static Power</th>
<th>Dynamic power per switch</th>
<th>Transformers</th>
<th>Clocked Gates</th>
<th>JJ count log10(n)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSFQ: rapid single flux quantum</td>
<td>1</td>
<td>– DC</td>
<td>High</td>
<td>$\alpha I_c \Phi_0 f$</td>
<td>-</td>
<td>Yes</td>
<td>4.4</td>
</tr>
<tr>
<td>LR-RSFQ: inductor-resistor RSFQ</td>
<td>1</td>
<td>– DC</td>
<td>Low</td>
<td>$\alpha I_c \Phi_0 f$</td>
<td>-</td>
<td>Yes</td>
<td>1.6</td>
</tr>
<tr>
<td>LV-RSFQ: low-voltage RSFQ</td>
<td>1</td>
<td>– DC</td>
<td>Low</td>
<td>$\alpha I_c \Phi_0 f$</td>
<td>-</td>
<td>Yes</td>
<td>3.7</td>
</tr>
<tr>
<td>ERSFQ: energy-efficient RSFQ</td>
<td>1</td>
<td>– DC</td>
<td>0 *</td>
<td>$I_b \Phi_0 f$</td>
<td>-</td>
<td>Yes</td>
<td>3.8</td>
</tr>
<tr>
<td>eSFQ: efficient SFQ</td>
<td>1</td>
<td>– DC</td>
<td>0 *</td>
<td>$I_b \Phi_0 f$</td>
<td>-</td>
<td>Yes</td>
<td>3.4</td>
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<tr>
<td>Clockless SFQ</td>
<td>1</td>
<td>– DC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.8</td>
</tr>
<tr>
<td>DSFQ: dynamic SFQ</td>
<td>1</td>
<td>– DC</td>
<td>‡</td>
<td>‡</td>
<td>-</td>
<td>Some</td>
<td>0.7</td>
</tr>
<tr>
<td>TSFQ: temporal SFQ</td>
<td>1</td>
<td>– DC</td>
<td></td>
<td></td>
<td>-</td>
<td>No</td>
<td>(2.8)</td>
</tr>
<tr>
<td>xSFQ: alternating SFQ</td>
<td>2</td>
<td>– DC</td>
<td>‡</td>
<td>‡</td>
<td>-</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>nTron: nanowire cryotron</td>
<td>1</td>
<td>– DC</td>
<td>~0</td>
<td>varies</td>
<td>-</td>
<td>Yes</td>
<td>1.5</td>
</tr>
<tr>
<td>hTron: heater-cryotron nanowire</td>
<td>1</td>
<td>– DC</td>
<td>~0</td>
<td>varies</td>
<td>-</td>
<td>Yes</td>
<td>1.2</td>
</tr>
<tr>
<td>HFQ: half flux quantum</td>
<td>0.5</td>
<td>– DC</td>
<td>Low</td>
<td></td>
<td>-</td>
<td>Yes</td>
<td>1.2</td>
</tr>
<tr>
<td>SFQ-AC: AC-powered SFQ</td>
<td>1</td>
<td>~ AC</td>
<td>‡</td>
<td>‡</td>
<td>P</td>
<td>Yes</td>
<td>5.9</td>
</tr>
<tr>
<td>RQL: reciprocal quantum logic</td>
<td>2</td>
<td>~ AC</td>
<td>~0</td>
<td>$\alpha I_c \Phi_0 f/2/3$</td>
<td>P, G</td>
<td>Some</td>
<td>4.9</td>
</tr>
<tr>
<td>PML: phase mode logic</td>
<td>1</td>
<td>~ AC</td>
<td>~0</td>
<td>$\alpha I_c \Phi_0 f/3$</td>
<td>P, G</td>
<td>Some</td>
<td></td>
</tr>
<tr>
<td>AQFP: adiabatic quantum flux parametron</td>
<td>-</td>
<td>~ AC</td>
<td>~0</td>
<td>$\alpha I_c \Phi_0 f \tau_{sw}/\tau_x$</td>
<td>P, G</td>
<td>Yes</td>
<td>4.3</td>
</tr>
<tr>
<td>RQFP: reversible QFP</td>
<td>-</td>
<td>~ AC</td>
<td>~0</td>
<td>$\alpha I_c \Phi_0 f \tau_{sw}/\tau_x$</td>
<td>P, G</td>
<td>Yes</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Table CEQIP-4

IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), October 2023. Invited presentation given at EUCAS 2023, Sept. 3-7, 2023, Bologna, Italy
# Superconducting QC Roadmap

<table>
<thead>
<tr>
<th>Metric</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
<th>2028</th>
<th>2030</th>
<th>2032</th>
</tr>
</thead>
<tbody>
<tr>
<td>Qubit growth per year</td>
<td>2×</td>
<td>2×</td>
<td>2×</td>
<td>2×</td>
<td>2×</td>
<td>2×</td>
<td>2×</td>
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<tr>
<td>Qubit count</td>
<td>5.5e+1</td>
<td>2.2e+2</td>
<td>8.8e+2</td>
<td>3.5e+3</td>
<td>1.4e+4</td>
<td>5.6e+4</td>
<td>2.2e+5</td>
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<tr>
<td>Qubit type</td>
<td>Transmon</td>
<td>Transmon</td>
<td>Transmon</td>
<td>Transmon</td>
<td>?</td>
<td>?</td>
<td>?</td>
</tr>
<tr>
<td>Qubit lifetime T1, med. [ms]</td>
<td>0.5</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td></td>
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<tr>
<td>2 qubit gate error rate, median (p_2Q)</td>
<td>1.0e-2</td>
<td></td>
<td></td>
<td></td>
<td>1.0e-4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate depth (1/p_2Q)</td>
<td>1.0e+2</td>
<td></td>
<td></td>
<td></td>
<td>1.0e+4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Error correction code</td>
<td>Surface</td>
<td>Surface</td>
<td>Surface</td>
<td>Surface</td>
<td>Surface</td>
<td>Surface</td>
<td>?</td>
</tr>
<tr>
<td>Phys. qubits per logical qubit</td>
<td>1800</td>
<td>1800</td>
<td>1568</td>
<td>1568</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logical qubit count</td>
<td>1</td>
<td>7</td>
<td>35</td>
<td>140</td>
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<td></td>
<td></td>
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<tr>
<td>Logical qubit error rate</td>
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<td></td>
<td></td>
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<td>1.0e-15</td>
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<td></td>
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<tr>
<td>Control type, temp. [K]</td>
<td>CMOS, 300</td>
<td>CMOS, 300</td>
<td>CMOS, 300</td>
<td>CMOS, 4</td>
<td>CMOS, 4</td>
<td>CMOS, 4</td>
<td>SCE, 4</td>
</tr>
<tr>
<td>SCE control complexity [JJ]</td>
<td>1.1e+5</td>
<td>4.5e+5</td>
<td>1.8e+6</td>
<td>7.2e+6</td>
<td>2.9e+7</td>
<td>1.2e+8</td>
<td>4.6e+8</td>
</tr>
</tbody>
</table>
Searching for a winning combination

Semiconductor logic families

<table>
<thead>
<tr>
<th>1960s</th>
<th>1980s</th>
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<tbody>
<tr>
<td>ECL</td>
<td>ECL</td>
</tr>
<tr>
<td>DTL</td>
<td>DTL</td>
</tr>
<tr>
<td>TTL</td>
<td>TTL</td>
</tr>
<tr>
<td>NMOS</td>
<td>NMOS</td>
</tr>
<tr>
<td>PMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>CMOS</td>
<td>CMOS</td>
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</table>

<table>
<thead>
<tr>
<th>2010s</th>
<th>2030s</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSFQ</td>
<td>RSFQ</td>
</tr>
<tr>
<td>ERSFQ</td>
<td>ERSFQ</td>
</tr>
<tr>
<td>eSFQ</td>
<td>eSFQ</td>
</tr>
<tr>
<td>nTron</td>
<td>nTron</td>
</tr>
<tr>
<td>DSFQ</td>
<td>DSFQ</td>
</tr>
<tr>
<td>HFQ</td>
<td>HFQ</td>
</tr>
<tr>
<td>xSFQ</td>
<td>xSFQ</td>
</tr>
<tr>
<td>FPL</td>
<td>FPL</td>
</tr>
<tr>
<td>SFQ-AC</td>
<td>SFQ-AC</td>
</tr>
<tr>
<td>RQL</td>
<td>RQL</td>
</tr>
<tr>
<td>PML</td>
<td>PML</td>
</tr>
<tr>
<td>PCL</td>
<td>PCL</td>
</tr>
<tr>
<td>AQFP</td>
<td>AQFP</td>
</tr>
<tr>
<td>DQFP</td>
<td>DQFP</td>
</tr>
<tr>
<td>RQFP</td>
<td>RQFP</td>
</tr>
<tr>
<td>SSBF</td>
<td>SSBF</td>
</tr>
</tbody>
</table>

Considerations:
- Performance
- Power (Static, Dynamic)
- Supply current
- Cost
  - Design
  - Area
  - Fabrication
  - Yield
  - Packaging
- ...

What are the key metrics and limits?

en.wikipedia.org/wiki/CMOS
Key Metrics and Limits for SCE logic

1. Power dissipation (static + dynamic)
2. Current supply
3. Area and scalability (problems: transformers, path balancing)
4. Variation sensitivity (process, magnetic field, supply current, trapped flux)
5. Memory (using logic process)
6. Architectural
   1. Composability
   2. Logic depth per clock cycle
   3. Time usage
   4. Performance
7. Cost
   1. Design
   2. Fabrication (includes area, yield, packaging)
   3. Testing
   4. Shielding
2. Power dissipation

*(static + dynamic)*

Limits:
1. 100 mW/cm² in LHe
2. 10 mW/cm² on cold head

Best practice for power distribution:
1. No resistors
2. No switching junctions
2. Current Supply

Uses:
1. Junction biasing (waste!)
2. Makeup energy (necessary)

Best practice:
1. AC to SFQ
2. AC
DC Supply Current to Bias JJs

*Biasing sets signal flow direction ➤*

- $I_C \approx 100 \, \mu\text{A}$ (constraints: thermal noise, switching energy)
- $K_0 \approx 0.7$ (bias current ratio, $K_0 \equiv i/I_C$)
- $\alpha \approx 0.5$ (fraction of biased junctions)

- Bias current for 1 million junctions in parallel?
  
  $$I_b = N I_C K_0 \alpha = (1\times10^6)(100\times10^{-6})(0.7)(0.5) = 35 \, \text{A}$$

- Way too much current and not nearly enough junctions!

- Traditional DC biasing will not scale.
Supply Current: Recycling

**DC bias current**

- Pass DC bias current through a series of \( N \) ground plane ‘islands’
  - \( N = 16 \) demonstrated with highly regular circuits (shift registers) [1]
- Advantages
  - \( N \times \) bias current reduction
- Disadvantages
  - Clock, data nets also require separation
  - Area multiplier \( \approx 1.5 \times \) (??)
  - JJ return current paths can affect margins
  - Complexity of balancing island currents
  - Capacitive coupling between floating islands
  - Ground plane gap shields needed

▶ Seems difficult with limited benefits

---


Supply Current: AC/SFQ Conversion

• Better: Convert AC to SFQ (not DC) on chip using rectifiers
• Best used with logic cells that require AC or no bias current
• Advantages
  • AC supply to converters in series, so can supply more cells (∼1000×)
• Disadvantages
  • Complexity, area overhead factor ≈ 2×
  • Transformers don’t scale well
  • $f_{AC} > f_{clock}$ for best energy efficiency
  • Need to design more logic cells that use AC or no bias current

Deserves further investigation

Fig. 3a. AC/SFQ converter supplying a JTL. [1]


EUCAS 2023 Sep 7, 4-ES-SL-01, Mukhanov
AC Power Distribution

Design concept for large-scale clock distribution

• Local storage of power and clock signal in high-Q LC-resonators
  • 1 resonator per tile

• 2D mesh of LC resonators has a zero-order mode
  • Clock signal distribution over large area with only small amplitude and phase variation

• 30 GHz design with 400 M taps/cm²

A. Herr +, “Scaling NbTiN-based ac-powered Josephson digital to 400M devices/cm²,” 2023, arXiv.2303.16792
AC Power Scaling

Transformers or capacitors?

• Transformers [1]
  • Current required for JJ biasing does not scale
  • Wire size limited by wire $J_c$
  • Voltage also increases due to kinetic inductance at small sizes

$\frac{i_1}{M} \propto \frac{i_j}{M} \quad V_1 = L \frac{di_1}{dt} \propto (L_{1M} + L_{1K}) f_j$

• Capacitors [2]
  • Current required for JJ biasing does not scale
  • But current is the same on both sides
  • Current increases with frequency

$M = \kappa (L_{1M} L_{2M})^{1/2}$

$L_1 = L_{1M} + L_{1K}$

$L_2 = L_{2M} + L_{2K}$

[I] S. Tolpygo, 2023, doi: 10.1109/TASC.2022.3230373

3. Area and Scalability

Checks:
1. Inductors
2. Transformers
3. Passive transmission line (PTL) width
4. Josephson junctions
   1. Size and scalability
   2. Types (0-JJ, pi-JJ, phi-JJ)
   3. Self-shunted
   4. Unshunted

Best practices:
1. Mix of JTLs, PTLs
2. No shunt resistors
Passive transmission lines (PTL)

**Important interconnects**

- PTL width (~ 4 µm) is a major obstacle to scaling
  - JJJs are low impedance drivers
  - Reducing the PTL width increases impedance, which causes reflections due to impedance mismatch
  - Reducing JJ Ic increases impedance, but reduces pulse energy

- Using only PTLs for routing requires too much area

- Additional PTL layers would increase area density but require +2 metal layers each

---

PTL cross section
Herbst +, 2020, doi: [10.1109/TASC.2020.3006988](https://doi.org/10.1109/TASC.2020.3006988)

Logic gate

AMD2901 4-bit processor design with 16,840 gates (upper left portion of overall layout)

Placed and routed in Synopsys Fusion Compiler (FC) and viewed in Custom Compiler
4. Variation sensitivity

Checks:
1. Process
2. Supply current or power
3. Trapped flux, Magnetic field

Best practices:
1. No need to match multiple devices (e.g. JJ and inductors)
2. No inductors or transformers
3. Phase shift devices (?)
4. Logic tolerant of variations (?)
Phase Engineering: $\varphi$ Junctions

One Junction to rule them all?

• Storing element compaction [1]

“Inductorless” circuits with small mutual inductances

Non-traditional Josephson junctions to replace inductors, reduce JJ count

• Junction types
  • 0 junctions (SIS), switching
  • 0 junction stacks (SNsNSNsNS)
  • π junctions (SFS)
  • φ junctions [1], [3]

• Questions:
  • Can the devices be made?
  • And with sufficiently small parameter variations ($I_c, L$)?

5. Memory

Metrics:
1. Capacity
2. Density
3. Time for read/write
4. Energy for read/write

Best practices:
1. (?)
6. Architectural

Goal: Add metrics for architectural properties

Metrics:
1. Logic depth per clock cycle
2. Time usage (?)
3. Performance (alone or per unit area, power, energy, or cost)
4. Composability

Best practices:
1. AC clocking
2. Clock reduction or elimination
   1. Macro blocks or cell-abutment logic
   2. Self-timed or asynchronous
3. Efficient data representation
4. Neuromorphic circuits (?)
AC Clocking

Use AC power as the clock

- AQFP (most established)
  - **Advantages**: JJs are all the same size and small (50 μA), energy efficient, good margins, majority logic
  - **Disadvantages**: large area, transformers, clocked gates, memory (?), majority logic

- Reciprocal quantum logic (RQL)
  - **Advantages**: Few JJs per logic gate, good margins, proven
  - **Disadvantages**: transformers, clock frequency limits, EDA tool support (?), controlled by Northrop Grumman

- Pulse conserving logic (PCL)
  - **New!**
  - 12 levels of logic at 30 GHz
  - OMA3 gate (OR3/MAJ3/AND3)


Design concept for large scale clock distribution
2D array of tightly coupled local, lumped LC resonators

- Local storage of power and clock signal in high-Q LC-resonators
  - 1 resonator/tile (1 tile ~5x5 μm²)
- 2D mesh of LC resonators has a zero-order mode
  - Clock signal distribution over large area with only small amplitude and phase variation

- 30 GHz design with 400 M taps/cm²

Different clocking approaches

Asynchronous

Regular Synchronous

Fully Synchronous

- Flexible pipelining
- Flexible pipelining
- Fixed gate-level pipelining
Pipelining in traditional SFQs

Overhead multiplies the cost of clocking!

Inverse Performance

\[ \text{TPI (Time/Instruction)} = \text{CPI} \times \text{Cycle time} \]

- Inverse Performance
- Technology-dependent
- Architecture-dependent
- Workload-dependent (% of p. hazards)
- Architecture-dependent (# pipeline stages, etc.)

Cell count

\[ N_{\text{cells}} = N_{L_{\text{gates}}} + N_{FFS} + N_{\text{splitters}} \]

- \( N_{L_{\text{gates}}} \)
- \( N_{FFS} \)
- \( N_{\text{splitters}} \)

Energy

\[ \text{EPI (Energy/Instruction)} = E_{\text{dyn}} + E_{\text{stat}} \]

- \( E_{\text{dyn}} \)
- \( E_{\text{stat}} \)

- Varies between SFQ families

RISC-V RV32I

- Total # logic gates = 10,000
- # gates on the critical path = 150

- \# JJs per logic gate varies between RSFQ, LR-SFQ, ERSFQ, eSFQ

Mukhanov, 2011, doi: 10.1109/TASC.2010.2096792

Ishida+, “32 GHz 6.5 mW, gate-level-pipelined 4-bit processor ...”, 2020, doi: 10.1109/VLSICircuits18222.2020.9162826
Architectural approaches: there are only 3!

**Fast (circuit) clock vs slow (architecture) clock**

- MANA is a two-stage pipeline from a pure computer architecture point of view.
- This 1st stage has a latency of 1 cycle.
- This 2nd stage has a total latency of 26 cycles.
- The 2nd stage of MANA can accommodate 26 instructions in-flight although MANA will only issue a maximum of 4 instructions successively.

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**Multi-threading**

- SFQ-GLPI consists of 24 pipeline stages.
- We reduced the number of threads to 12 because the chip area was limited.
- Although such degradation makes the total area required for implementing Register File (RF) half, it also halves the peak performance.

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**Increase operational intensity**

- SuperNPU increases the operational intensity by assigning more registers to each processing element (PE).
- Operational intensity is not only architecture- but also algorithm-dependent.

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Ishida+, “32 GHz 6.5 mW, gate-level-pipelined 4-bit processor ...”, 2020, doi: 10.1109/VLSICircuits18222.2020.9162826


7. Cost

Metrics:

1. Design
2. Fabrication (includes area, yield, packaging)
3. Testing
4. Shielding


<table>
<thead>
<tr>
<th>Processor</th>
<th>Manufacturing Energy</th>
<th>Assembly Energy</th>
<th>Use Phase Energy</th>
<th>Total Energy</th>
<th>Overall Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS RISC-V</td>
<td>0.17 KWh</td>
<td>0.08 KWh</td>
<td>665.23 KWh</td>
<td>665.48 KWh</td>
<td>237X (with cooling 205X)</td>
</tr>
<tr>
<td>AQFP RISC-V</td>
<td>1.61 KWh</td>
<td>1.19 KWh</td>
<td>0.001 KWh (with cooling 0.42 KWh)</td>
<td>2.81 KWh (with cooling 3.23 KWh)</td>
<td></td>
</tr>
</tbody>
</table>
Key Metrics and Limits for SCE logic

1. Power dissipation (static + dynamic)
2. Current supply
3. Area and scalability (problems: transformers, path balancing)
4. Variation sensitivity (process, magnetic field, supply current, trapped flux)
5. Memory (using logic process)
6. Architectural
   1. Composability
   2. Logic depth per clock cycle
   3. Time usage
   4. Performance
7. Cost
   1. Design
   2. Fabrication (includes area, yield, packaging)
   3. Testing
   4. Shielding
## Superconductor Digital Logic Families

<table>
<thead>
<tr>
<th>Name</th>
<th>Crit. (I, V)</th>
<th>Power</th>
<th>SFQ.</th>
<th>Critical value, typical at 4 K</th>
<th>Devices per unit current [A⁻¹]</th>
<th>Static Power</th>
<th>E switch [aj]</th>
<th>Devices</th>
<th>Switch count</th>
<th>IC area</th>
<th>X-formers</th>
<th>Clock. JJ count</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSFQ: rapid single flux quantum</td>
<td>dc – 1</td>
<td>1.5E-04</td>
<td>2.8E+4</td>
<td>High</td>
<td>0.1</td>
<td>JLR</td>
<td>x1</td>
<td>x1</td>
<td></td>
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<td>LR-RSFQ: inductor-resistor RSFQ</td>
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<td>0.1</td>
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<td>x1</td>
<td>x1</td>
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<td>LV-RSFQ: low-voltage RSFQ</td>
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<td>ERSFQ: energy-efficient RSFQ</td>
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<td>2.8E+4</td>
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<td>0.15</td>
<td>JLR</td>
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<td>x1.4</td>
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<td>6.8E+3</td>
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<td>eSFQ: efficient SFQ</td>
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<td>Self-timed SFQ</td>
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<td>TSFQ: temporal SFQ</td>
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<td>xSFQ: alternating SFQ</td>
<td>dc – 2</td>
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<td>2.8E+4</td>
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<td>JLR</td>
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<td>HFQ: half flux quantum</td>
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<td>8.5E+4</td>
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<td>0.05</td>
<td>JLP</td>
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<td>nTron: nanowire cryotron</td>
<td>-</td>
<td>1.8E-04</td>
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<td>1</td>
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<td>hTron: heater-cryotron nanowire</td>
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<td>&gt;1E+9</td>
<td>0</td>
<td>1000</td>
<td>LNR</td>
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<td>SFQ-AC: AC-powered SFQ</td>
<td>ac ~ 1</td>
<td>1.0E-04</td>
<td>&gt;1E+8</td>
<td>†</td>
<td>JLR</td>
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<td>8.1E+05</td>
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<tr>
<td>RQL: reciprocal quantum logic</td>
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<td>&gt;1E+8</td>
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<td>0.07</td>
<td>JLR</td>
<td>x0.5</td>
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<td>7.3E+04</td>
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<td>PML: phase mode logic</td>
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<td>5.0E-05</td>
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<td>Low</td>
<td>0.04</td>
<td>JLR</td>
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<tr>
<td>PCL: pulse conserving logic</td>
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<td>&gt;1E+8</td>
<td>~0</td>
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<tr>
<td>AQFP: adiabatic quantum flux parametron</td>
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<td>5.0E-05</td>
<td>&gt;1E+8</td>
<td>~0</td>
<td>0.002</td>
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<td>2.1E+4</td>
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<td>RQFP: reversible QFP</td>
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<td>&gt;1E+8</td>
<td>~0</td>
<td>~0</td>
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<td>QPSJ: quantum phase slip junctions</td>
<td>V dc – -</td>
<td>&gt;1E+9</td>
<td>0.0001</td>
<td>CO</td>
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Quantum phase-slip junctions (QPSJs)

Voltage controlled devices might interface better with semiconductor electronics

![Fig. 1. SQUIDs using (a) JJs, (b) QPSJs [1]](image)

![Fig. 2. MoGe nanowire QPSJs [2]](image)

![Fig. 3. Memoryless OR gate [3]](image)

- Single Flux Quantum (SFQ): $\Phi_0 = I_L = \int V \, dt$

- Cooper pair of electrons: $2e = C \cdot V = \int I \, dt$

Demonstration needed!

Backup
## 2023 CEQIP Members

<table>
<thead>
<tr>
<th>Name</th>
<th>Area</th>
<th>Organization</th>
<th>Region</th>
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Macro blocks or cell-abutment logic

- **Macro blocks** to perform complex functions
  - Smaller, better performance
  - Licensed as intellectual property (IP) blocks
  - We need more of these!

- **Cell abutment logic**
  - Cells connect directly, like LEGO blocks
  - Blocks can contain JTLs or PTLs
  - Problem: EDA tools do not currently support abutment

2.5x area reduction: 8-bit multipliers using standard RSFQ gates and single-stage complex RSFQ gates

Cong +, 2021, doi: [10.1109/TASC.2021.3091963](https://doi.org/10.1109/TASC.2021.3091963)

Volk +, 2023, [10.1109/TASC.2023.3256797](https://doi.org/10.1109/TASC.2023.3256797)
Clock Reduction or Elimination

Overhead multiplies the cost of clocking!

- Bias current overhead estimates per clocked gate:
  - \( \approx 1.5 \times (?) \) for clocking (splitters, mostly)
  - \( \approx 4 \times (?) \) for path balancing (superlinear)
  - \( \approx 20 \times (?) \) for unused clock time (allowing for jitter, long lines, pipeline hazards, etc.)
  - \( \approx 1.5 \times (?) \) for higher fraction of JJs that switch

- \( \approx 180 \times (?) \) total

▷ Reduce or eliminate clocked cells

Clocked SFQ [1]

<table>
<thead>
<tr>
<th>clk</th>
<th>a</th>
<th>b</th>
<th>OR(a,b,clk)</th>
<th>AND(a,b,clk)</th>
<th>NOT(a,clk)</th>
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<tr>
<td>clk</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
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Temporal SFQ [1]

- FAb
- Laab
- D2a
- bl
- alb

Data representation

“0” and “1” are not the only way

• Race logic (RL) represents data in time
• Time slots within a clock period can be used to represent information and perform computations
  • Unary SFQ is a combination of pulse-stream arithmetic and race logic
• Benefits can include greatly reduced circuit area

Gonzalez-Guerrero +, 2022, doi: 10.1145/3503222.3507765
Neuromorphic Circuits using Superconductor Electronics

A more natural fit?

• Characteristics
  • Natural spiking behavior of Josephson junctions
  • Pulses travel on striplines without the RC time constants that typically hinder spike-based computing
  • Possibly tolerant to variations in component parameter values

• Needed:
  • Design methodology
  • Demonstrations at larger scale

Fig. 3a. Spiking in biological neurons [1]