IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), October 2017.
Contributed presentation We-SDM-15 given at ISEC 2017, Sorrento, Italy.

Superconductor Electronics and the International Roadmap for Devices and Systems

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ISEC 2017

Sorrento, Italy

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SCE and the International Roadmap for Devices and Systems (IRDS)

- How we got to IRDS
  - Electronics technology roadmaps
  - Rebooting Computing Initiative
- SCE (Superconductor Electronics)
  - Applications and Drivers
  - Benchmarking and Metrics
  - Technology Roadmaps
- Conclusions

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Electronics Technology Roadmaps

- 1993-1997 **NTRS**: National Technology Roadmap for Semiconductors

Characteristic	1992	1995	1998	2001	2004	2007
Feature size (microns)	0.50	0.35	0.25	0,18	0,12	0.10
Gates per chip (millions)	0.3	0.8	2.0	5.0	10.0	20.0
Bits per chip						
DRAM	16M	64M	256M	1G	4G	16G
SRAM	4M	16M	64M	256M	1G	4G
Wafer processing cost ($/cm²)	$4.00	3.90	3.80	3.70	3.60	3.50
Chip size (mm²)						
logic	250	400	600	800	1,000	1,250
memory	132	200	320	500	700	1,000
Wafer diameter (mm)	200	200	200-400	200-400	200-400	200-400
Defect density (defects/cm²)	0.10	0.05	0.03	0.01	0.004	0.002
Levels of interconnect (for logic)	3	4-5	5	5-6	6	6-7
Maximum power (watts/die)						
high performance	10	15	30	40	40-120	40-200
portable	3	4	4	4	4	4
Power supply voltage						
desktop	5	3.3	2.2	2.2	1.5	1.5
portable	3.3	2.2	2.2	1.5	1.5	1.5

By Semiconductor Industry Association - SIA, Semiconductor Technology Workshop Reports (1993), CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=20308931

Electronics Technology Roadmaps

- 1993-1997 **NTRS**: National Technology Roadmap for Semiconductors
- 1998-2013 **ITRS**: International Technology Roadmap for Semiconductors
  - Applied Moore's Law to integrated circuits
  - Physical scaling worked until about 2004, then cores, 3D, …
  - 2010: First selection of post-CMOS devices

Year of Production	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
MPU Printed Gate Length (nm)	31	28	25	22	19.8	17.7	15.7
MPU Physical Gate Length (nm)	22	20	18	17	15.3	14.0	12.8
Trench width at top (nm) [A]	38.4	32.4	28.8	25.2	22.6	20.2	18.0
Trench sidewall angle (degrees) [B]	>88.2	>88.2	>88.5	>88.7	>88.8	>88.9	>89.0
Gate etch bias (nm) [C]	5.4	4.9	4.5	4.1	3.7	3.4	3.0
Lgate 3s variation (nm) [D]	2.65	2.42	2.21	2.02	1.84	1.68	1.53
Lgate line width roughness 3s (nm) [E]	2.1	1.91	1.74	1.6	1.45	1.33	1.21
Across chip Lgate variation 3s (nm) [F]	1.31	1.24	1.17	1.1	1.04	0.98	0.93
Across wafer Lgate variation 3s (nm) [G]	0.91	0.84	0.77	0.7	0.64	0.58	0.53
Wafer to wafer within lot Lgate 3s (nm)	0.55	0.5	0.46	0.41	0.38	0.35	0.32
Lot to lot Lgate 3s (nm)	0.55	0.5	0.46	0.41	0.38	0.35	0.32
Dummy Gate Stack Removal Induced Lgate Variation 3s (nm) [H]	0.59	0.55	0.50	0.45	0.42	0.37	0.35
Minimum measurable gate dielectric remaining (post gate etch clean) [I]	>0	>0	>0	>0	>0	>0	>0
Profile control (side wall angle) [J]	90	90	90	90	90	90	90

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  - 2010: First selection of post-CMOS devices
- 2014-2015 **ITRS 2.0**
  - Driver changed from scaling to **applications**
  - 2015: Post-CMOS map of devices
- 2016+ **IRDS**: International Roadmap for Devices and Systems
  - Opened the door to non-semiconductor technologies
  - 2017: First roadmaps expected in November

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Rebooting Computing

- IEEE Rebooting Computing
  - 2013-16: 3 summits, 1 conference
- Elie Track
  - IEEE Rebooting Computing co-chair
  - IEEE Council on Superconductivity past president
  - Hypres past president
- Erik DeBenedicts
  - Sandia National Laboratories
  - ITRS Emerging Research Architectures
- Paolo Gargini
  - ITRS Chairman 1998-2016
  - Intel Fellow and Director of Technology Strategy (retired)

Rebooting Computing Summit 2 - Goal Setting

2014 May 12-14

Santa Cruz, CA

D. Scott Holmes, Ph.D.
Facilitator

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IRDS Organization

- International Focus Teams (IFTs)
  - Application Benchmarking
  - More Moore
  - **Beyond CMOS**
    - Memory
    - Logic
      - Charge state variable
      - Non-charge state variable
        - Spin
        - **Cryogenic Electronics** (here?)
    - Cryogenic Electronics (or here?)
  - Outside System Connectivity
  - Factory Integration
  - Metrology
  - Environment, Health, and Safety
  - Yield
  - System and Architecture (prelim.)

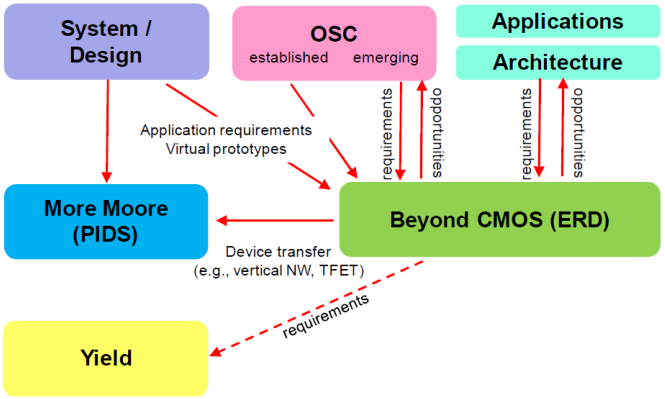

Figure 1. Illustration of cross-team interactions for Beyond CMOS (BC).

Source: http://irds.ieee.org/ > 2016_BC.pdf

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SCE Applications and Drivers

Application	Drivers	Metrics
Research & development	Quantum information processing, advanced sensors, computing, government funding	Foundries, process design kits, process capability, layer count, feature sizes, yield
Metrology	Voltage standard	Accuracy, precision, voltage range, frequency range (for ac)
RF signal processing & control	RF processor	Clock rate, signal-to-noise ratio, bandwidth
Data pre-processing	DSP: digital signal processor	Clock rate, throughput, bits, circuit density
Network routing	SOC-NW: system-on-chip, networking	throughput
High performance computing	MPU-HP: microprocessor unit, high performance	Floating point computation, memory performance, data rate, chip area, physical volume, energy efficiency
Data center	Microserver	Integer computation, memory performance, data rate, chip area, physical volume, energy efficiency

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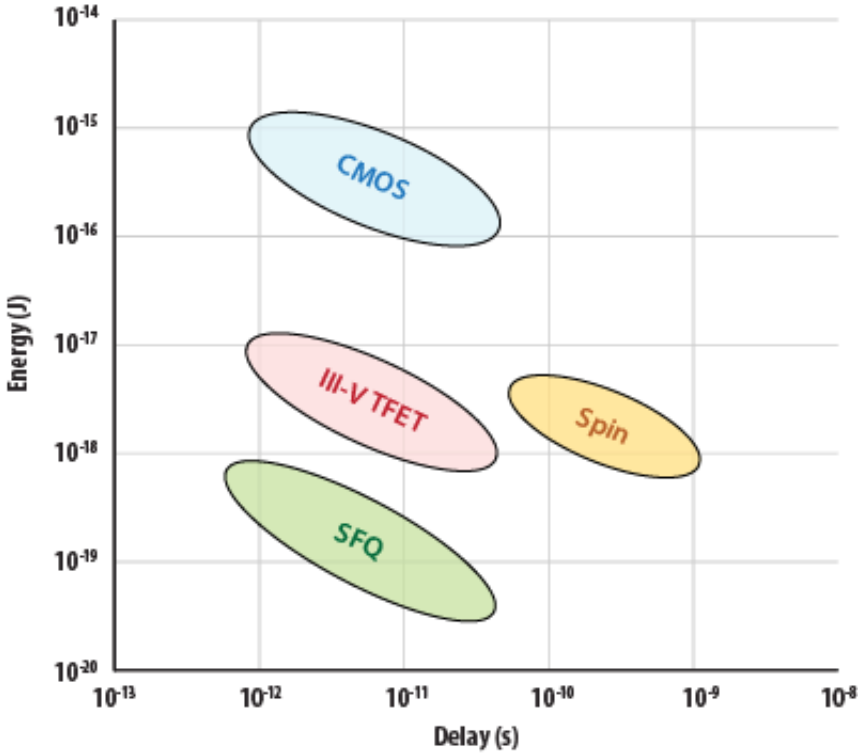
SCE Benchmarking and Metrics



MIT Lincoln Laboratory, "Forecasting superconductive electronics technology," The Next Wave, vol. 20, no. 3, 2014.
https://www.nsa.gov/research/tnw/tnw203/article2.shtml

- Superconducting SFQ looks good based on switching energy-delay, **but**:
  - Refrigeration requires x400 to x5000 energy
  - Wiring + leakage losses dominate for other technologies
- Conclusions:
  - Full system evaluation is required for SFQ
  - Better metrics and figures-of-merit needed!

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Energy–Delay Metrics: 32 bit Add

- RQL : Reciprocal Quantum Logic, a superconducting single flux quantum (SFQ) logic;
  J_c = 100 μA/μm^2, 12. 1 GHz
  - **RCA**: ripple-carry adder
  - **STPPA**: sparse-tree parallel-prefix adder
- 4.2 K operation; energy at room temperature with 1000 W/W refrigeration (range I : 400–10,000 W/W)
- Source for RQL data:
  Dorojevets, Chen, Ayala, Kasperek, "Towards 32-bit Energy-Efficient Superconductor RQL Processors: The Cell-Level Design and Analysis of Key Processing and On-Chip Storage Units," *IEEE Trans. Appl. Supercond.*, 2015.
  doi: 10.1109/TASC.2014.2368354 (Table I)
- Added to:
  Nikonov, Young, "Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits," *IEEE J. Exploratory Solid-State Comp. Devices Circuits*, 2015.
  doi: 10.1109/JXCDC.2015.2418033

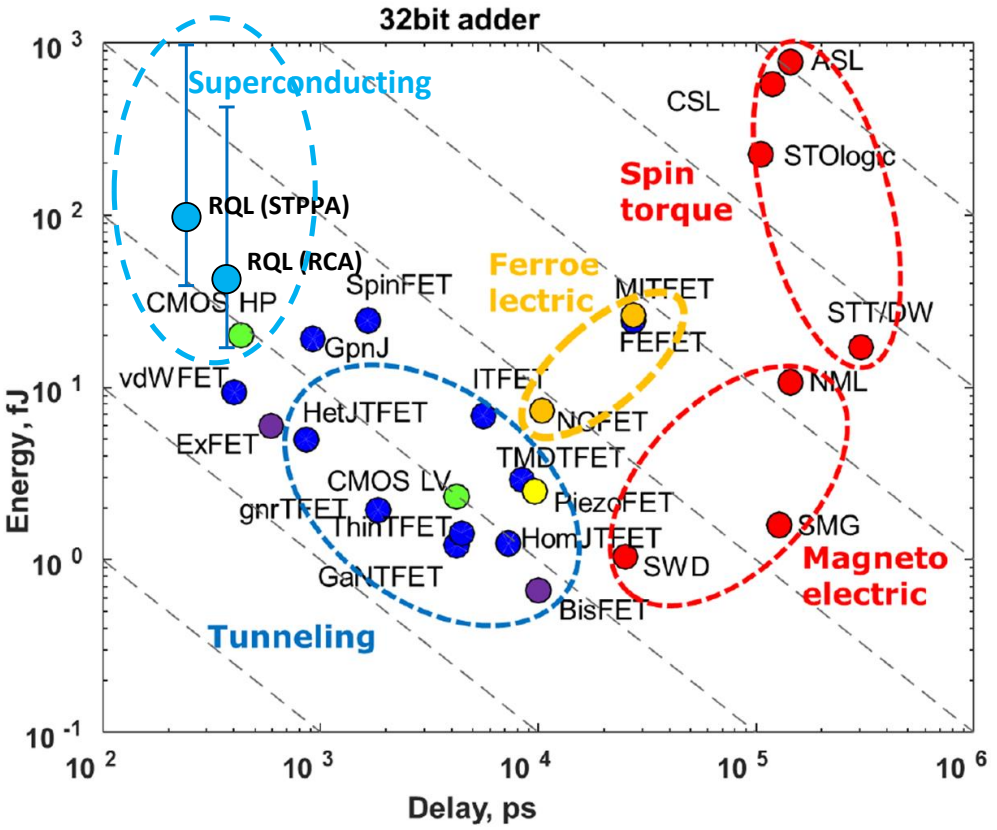

FIGURE 5. Switching energy versus delay of a 32-bit adder.

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Energy–Delay Metrics: 32 bit ALU

- RQL : Reciprocal Quantum Logic, a superconducting single flux quantum (SFQ) logic;
  J_c = 100 μA/μm^2, 16. 3 GHz, 205 fJ/op (32 bit), 402 ps
  - 4.2 K operation; energy at room temperature with 1000 W/W refrigeration (range I : 400–10,000 W/W)
  - Source for RQL data:
    Dorojevets, Chen, Ayala, Kasperek, "Towards 32-bit Energy-Efficient Superconductor RQL Processors: The Cell-Level Design and Analysis of Key Processing and On-Chip Storage Units," *IEEE Trans. Appl. Supercond.*, 2015.
    doi: 10.1109/TASC.2014.2368354 (Table I)
  - Added to:
    Nikonov, Young, "Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits," *IEEE J. Exploratory Solid-State Comp. Devices Circuits*, 2015.
    doi: 10.1109/JXCDC.2015.2418033

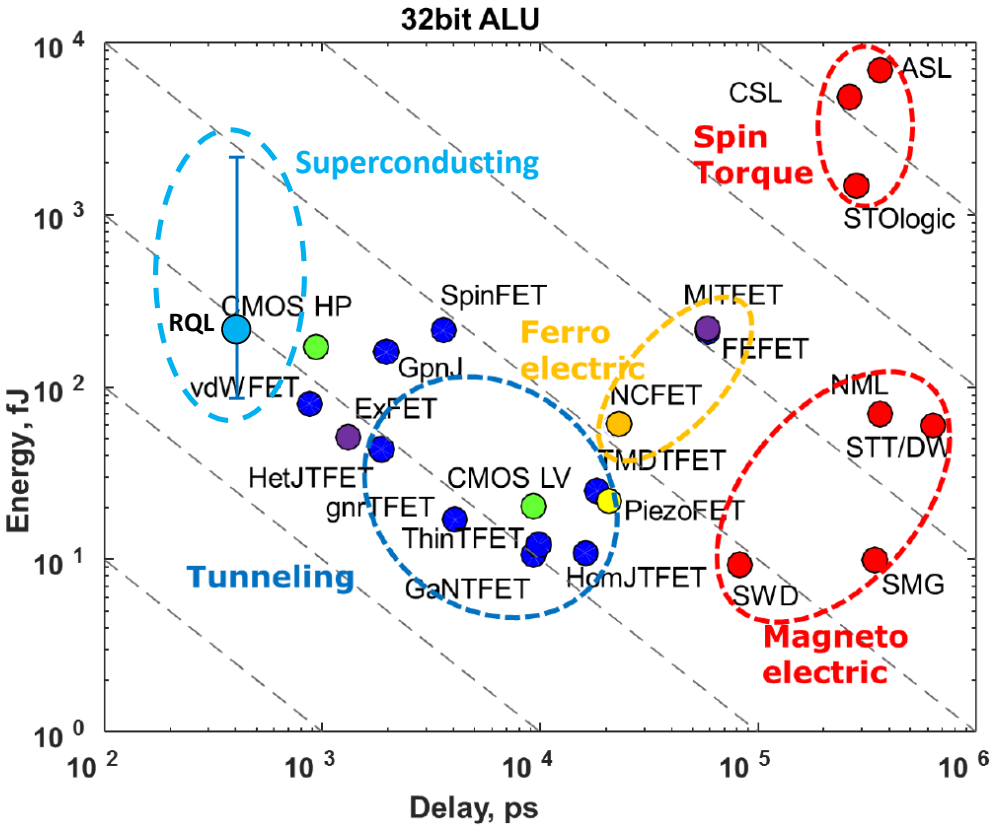

FIGURE 6. Switching energy versus delay of a 32-bit ALU.

Energy–Delay Metrics: Wiring

- RQL : Reciprocal Quantum Logic, a superconducting single flux quantum (SFQ) logic, J_c = 100 μA/μm^2
  - **JTL**: Josephson transmission line (0.13 fJ/bit, 5.5 ps)
  - **PTL**: passive transmission line (0.26 fJ/bit **0.01–20 mm**, 6.5 ps)
- 4.2 K operation; energy per bit at room temperature with 1000 W/W refrigeration (range I : 400–10,000 W/W)
- Source for RQL data:
  Dorojevets, Chen, Ayala, Kasperek, "Towards 32-bit Energy-Efficient Superconductor RQL Processors: The Cell-Level Design and Analysis of Key Processing and On-Chip Storage Units," *IEEE Trans. Appl. Supercond.*, 2015.
  doi: 10.1109/TASC.2014.2368354 (Fig. 1)
  + private communication for delays
- Added to:
  Pan, Chang, Naeemi, "Performance analyses and benchmarking for spintronic devices and interconnects," *2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC)*, San Jose, CA, 2016. doi: 10.1109/IITC-AMC.2016.7507679

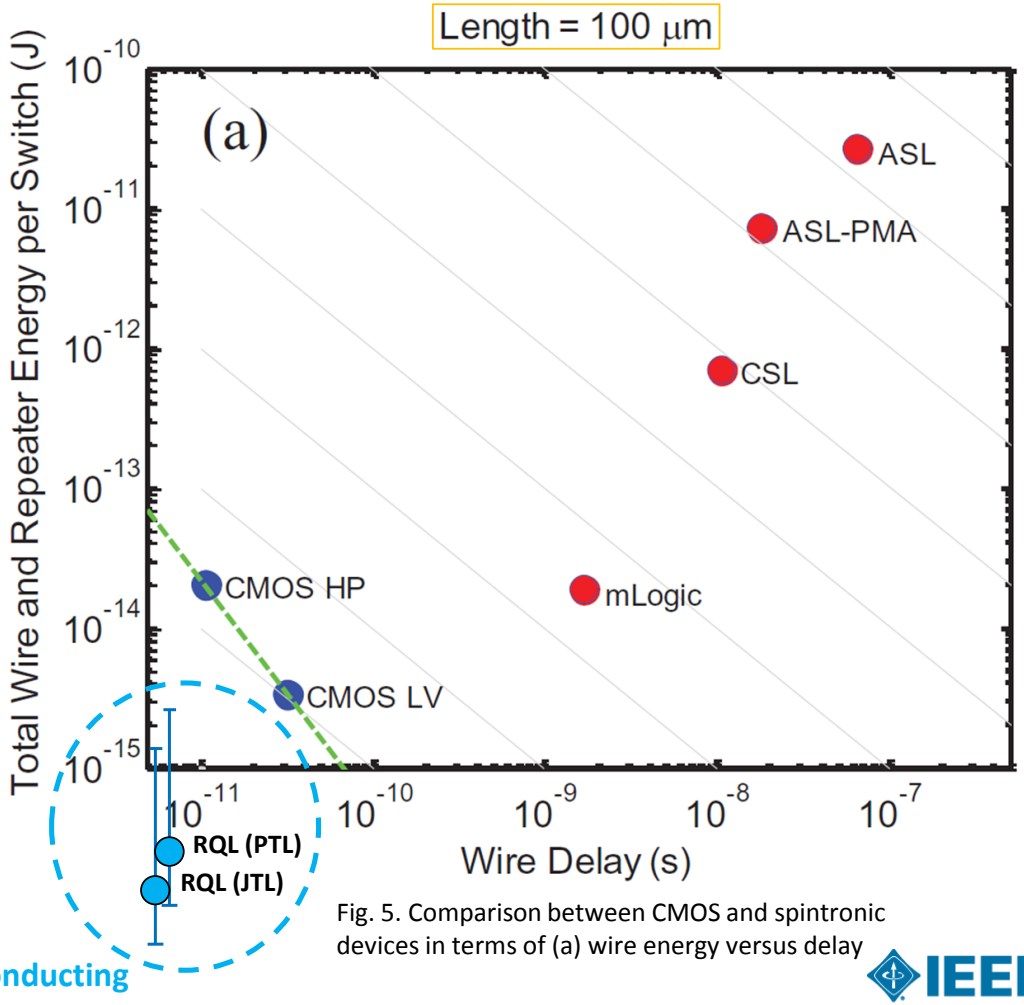

Fig. 5. Comparison between CMOS and spintronic devices in terms of (a) wire energy versus delay

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Metric: Throughput & Power Density

- RQL : Reciprocal Quantum Logic, a superconducting single flux quantum (SFQ) logic; J_c = 100 μA/μm^2, 16. 3 GHz, 9950 JJs, 205 fJ/iop (32 bit), ~5.6 mm^2
- 4.2 K operation; energy at room temperature with 1000 W/W refrigeration (range I : 400–10,000 W/W)
- Source for RQL data: Dorojevets, Chen, Ayala, Kasperek, "Towards 32-bit Energy-Efficient Superconductor RQL Processors: The Cell-Level Design and Analysis of Key Processing and On-Chip Storage Units," *IEEE Trans. Appl. Supercond.*, 2015. doi: 10.1109/TASC.2014.2368354 (Table I) + private communication for areas (**250 nm process**)
- Added to (10 nm processes): Nikonov, Young, "Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits," *IEEE J. Exploratory Solid-State Comp. Devices Circuits*, 2015. doi: 10.1109/JXCDC.2015.2418033

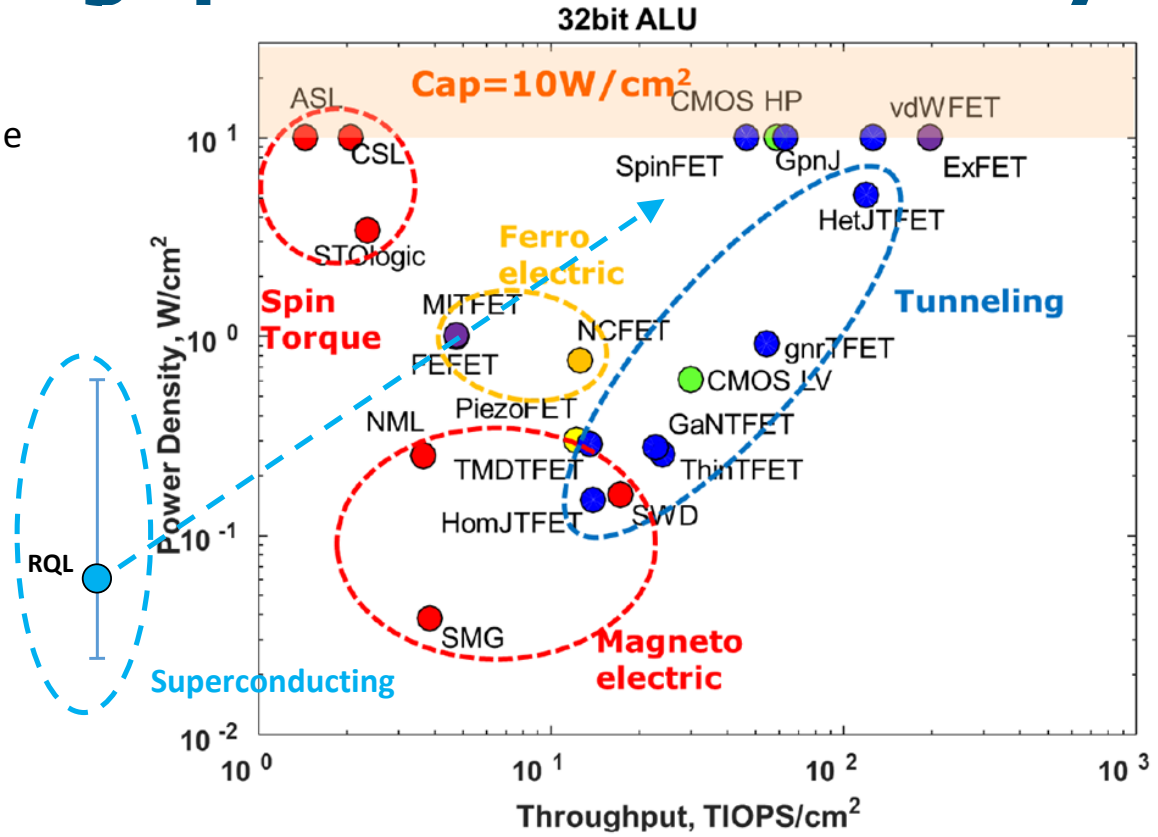

FIGURE 8. Dissipated power versus computational throughput (capped at 10 W/cm^2) related to a 32-bit ALU.

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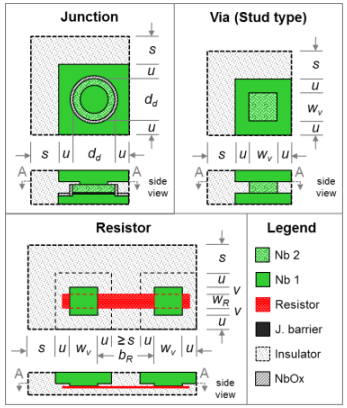
Metrics: Next Steps

- **Models** for devices and circuits
  - Variety of superconductor technologies (e.g., RSFQ, AQFP)
  - Core metrics: circuit area, delay, and energy
  - Scaling models
- **Metrics** for applications
  - Logic, Memory, Interconnects
- **Refrigeration**: standard multipliers (vs. operating T, capacity) and ranges



SCE Technology Roadmap

- 15+ year span
  - Current (-1)
  - Near term (0 to +7)
  - Long term (+8 to +15)
  - Will be far less detailed than for CMOS
- First roadmap for digital computing
- Key areas:
  - Foundry and fabrication processes
  - Circuit parameters
  - Design tools
  - Packaging and integration

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SCE Technology Roadmap

- Past roadmaps provide a base for future efforts

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2. J. M. Rowell, "Recommended directions of research and development in superconducting electronics," *IEEE Trans. Appl. Supercond.*, vol. 9, no. 2, pp. 2837–2848, Jun. 1999.
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4. S. Tahara *et al.*, "Superconducting digital electronics," *IEEE Trans. Appl. Supercond.*, vol. 11, no. 1, pp. 463–468, Mar. 2001.
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7. O. Tsukamoto, "Overview of superconductivity in Japan - Strategy **road map** and R&D status," *Physica C: Superconductivity and its Applications*, vol. 468, no. 15–20, pp. 1101–1111, 2008.
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9. J. Kohlmann and R. Behr, "Development of Josephson voltage standards," Chapter 11 in: *Superconductivity - Theory and Applications, Adir Moyses Luiz, Ed.*, 2011. DOI: 10.5772/17031
10. C. J. Fourie and M. H. Volkmann, "Status of Superconductor Electronic Circuit Design Software," *v*, vol. 23, no. 3, pp. 1300205–1300205, Jun. 2013.

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Balance

- Progress (distance)
- Speed of Innovation (change rate × difficulty)

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Conclusions

- IRDS is a **golden opportunity** for SCE
- Your participation is encouraged!