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Digital Circuits Using Self-Shunted $Nb/Nb_xSi_{1-x}/Nb$ Josephson Junctions

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***Abstract* – For the first time superconducting digital circuits based on Josephson junctions with amorphous niobium-silicon (a-NbSi) barriers have been fabricated and tested. Single-flux-quantum (SFQ) shift registers operated with ±30 % bias margins, confirming junction reproducibility and uniformity. Static digital dividers operated up to 165 GHz for a single value of bias current, which was only marginally slower than circuits fabricated with externally shunted AlO_x-barrier junctions having a comparable critical current density of 4.5 kA/cm^2. In comparison, self-shunted a-NbSi junctions enabled a doubling in circuit density. This and their relatively thick 10 nm barriers could increase the yield of complex SFQ circuits.**

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Josephson junctions are the basis for superconducting electronics. Their exceptional properties, including terahertz cut-off frequency, low power dissipation, and low noise, have found many applications in metrology, mixed-signal circuits, radiation detectors, and magnetic sensors. Superconducting single-flux-quantum (SFQ) technology realizes unprecedented high-speed and low-power operation [1].

Currently, most superconducting digital circuits are based on $Nb/AlO_x/Nb$ superconductor–insulator–superconductor (SIS) Josephson junctions [2]. They have demonstrated good uniformity and reproducibility on a scale of 10,000 or more junctions per chip [3, 4]. However, the maximum operating frequency of such circuits is an order of magnitude lower than that of small circuits based on the same junctions [5]. One limitation of this type of junction may be imposed by the thin (~1 nm) tunnel barrier. A typical Nb/Al–AlO_x/Nb device has a critical current density (J_c) of 4.5 kA/cm^2. Devices with J_c = 20 kA/cm^2 approach a potential practical limit for AlO_x [6], as transport becomes increasingly dominated by barrier defects as J_c increases. Tunnel junctions have a high intrinsic capacitance and require external shunting in order to reduce the *RC* time constant. This increases the complexity of the fabrication process and circuit layout, and reduces circuit density.

These limitations are avoided in self-shunted $Nb/Nb_xSi_{1-x}/Nb$ junctions. For similar J_c, a Nb_xSi_{1-x} barrier is nearly ten times thicker than an AlO_x tunnel barrier. If effects such as surface roughness or pinholes are limiting the junction uniformity, junctions with thicker barriers should have better uniformity, leading to better circuit yield. Indeed, silicide junctions have been demonstrated in voltage standard devices with 70,000 junctions [7].

The electrical characteristics of NbSi-barrier junctions are tunable due to the fact that the barrier is formed by co-sputtering Si and Nb. By independently controlling the composition (through the relative sputtering rates) and the thickness (through the duration of the deposition), a large range of values for the junction properties may be obtained, enabling these junctions to be used in a wide range of circuits and applications [8].

The NbSi films of interest for SFQ circuits are on the insulating side of the metal-insulator transition. In this regime, flexible control of the barrier dissipation and capacitance is possible by changing its composition and thickness. For instance, it is possible to have junctions with the same J_c, but different I_cR values (I_c is the critical current and R is the effective resistance of the junction). Likewise, it is possible to have junctions with different values of J_c which have the same I_cR product [9]. These junctions can be made to be intrinsically critically-damped over a wide range of J_cs. The co-sputtered deposition process is simple and does not require any intermediate oxidation steps. The barrier materials can also be dry-etched with the same process as the Nb electrodes. Both of these features were exploited to produce uniform arrays of double- and triple-stacked junctions for voltage standard circuits [10]. Higher-density SFQ circuits may also be possible by exploiting this simple fabrication process.

The two SFQ circuits we measured were a static digital divider and a 16-bit shift register. The divider circuit is the industry standard for determining the speed of a digital technology [5, 11]. The shift register is a standard circuit for verifying junction reproducibility and yield. Both circuits were designed using conservative 2 μm design rules for the interconnects and 1.5 μm smallest diameter of the junctions, similar to the typical design rules used for 4.5 kA/cm^2 Nb/AlO$_x$/Nb processes [12].

The two wafers whose chips produced the results presented here were intentionally fabricated to have nearly the same critical current density of 5.5 kA/cm^2, but different junction resistances in order to study the effective damping of the NbSi junctions in digital circuits. Wafer B had junctions with 10.8 nm thick barriers deposited with Nb/Si sputtering powers of 16/200 W, while wafer C had junctions with 9.6 nm thick barriers with 15/200 W Nb/Si sputter powers.

Figure 1 shows the dc I–V curves of 2.5 μm x 2.5 μm square junctions from wafer B at 4.2 K, without and with suppression of the Josephson critical current by a magnetic field parallel to the film plane. No hysteresis is observed. An indication of the uniformity of the silicide barriers in this work is the nearly ideal Fraunhofer patterns (I_c variation with applied field) observed; I_c is nearly completely suppressed. With I_c suppressed, the I–V curves are non-linear at low voltages and approximately linear above the superconducting gap, V_g= 2.6 mV.

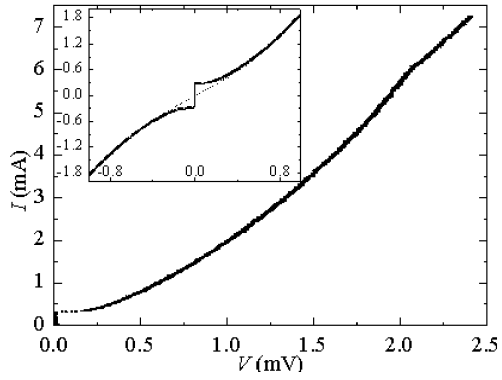

Fig. 1. *I–V* characteristic of a typical junction at 4.2 K. The inset shows the curve limited to low currents. For the solid curve no magnetic field was applied, while the dashed curve corresponds to the first minimum in the Fraunhofer pattern.

The nonlinearity below ~1 mV in Fig. 1 is of interest for digital circuits and needs to be further investigated. It is likely that the conduction through the barrier, which is near a metal-insulator transition, is intrinsically nonlinear. The dynamic resistance of the *I–V* curve below the gap voltage is generally higher than the linear resistance (R_n) that is measured above the gap. This means that the effective characteristic voltage, $V_c=I_cR$, for digital circuit applications is higher than estimates based on R_n. While the resistance is highly non-linear, an accurate model of the resistor can be implemented in SPICE for physical-level circuit simulation. By matching the hysteresis of the junction to the SPICE model, the junction capacitance may also be estimated.

The quality factors of both junctions were estimated from the amount of hysteresis in the curves [13]. This indicates that the junctions are approximately optimally damped with McCumber parameters $\beta_c \leq 1$ and $\beta_c \approx 2$ for wafers B and C, respectively.

An SFQ static divider is a useful diagnostic tool for junction properties, because it can directly measure the maximum operating frequency for a digital circuit. Numerous experiments with SFQ static dividers fabricated in Nb/AlO_x/Nb processes [5, 11] show that the maximum operating frequency, f_{max}, scales as the square root of J_c, at optimum damping of $\beta_c = 1$, as follows:

$$f_{\max} = k\frac{V_c}{\Phi_0} = k\frac{1}{\sqrt{2\pi\Phi_0}}\sqrt{\frac{J_c}{C_f}}, \qquad (1)$$

where C_f is the specific capacitance of the junction and $k \approx 0.82$ is an empirical constant. This universal trend is relatively insensitive to the actual value of the damping, although it has not been extensively studied with barrier materials different from AlO_x.

The static divider consists of a voltage-controlled oscillator (VCO), Josephson transmission lines (JTL) interconnecting twelve stages of SFQ toggle flip-flops (TFF), and an output amplifier. The VCO converts a dc input into a SFQ pulse train. The TFF acts as a logical divide-by-two, and alternately sends pulses to two output ports. A daisy chain of twelve TFF's divides the VCO frequency by 2^{12}. The divider chain and the VCO are biased independently. An additional independent bias is used for a six-stage JTL buffer in order to reduce loading effects between the TFF and the VCO. Two additional JTL stages are used between each TFF stage. The last stage is connected directly to a two-junction comparator that converts the state of the TFF into a voltage, in a manner similar to the SFQ-to-dc converter described in [14].

The chip was mounted in a 20 GHz, 3 dB cut-off, 20 pad chip holder and cooled to 4.2 K. All lines to the circuit are dc except the output, which is used to apply current and to read voltage through a bias-T at the top of the probe. Results are shown in Fig. 2, in which each set of connected points corresponds to the output frequency of the divider as a function of TFF bias with a fixed operating point of the VCO. The horizontal region of each curve indicates proper digital operation of the divider chain. The observed output frequency is referred back to the VCO pulse train by multiplying by 2^{12}. For fixed TFF bias, the divider chain showed operating margins at all frequencies up to 165 GHz (hashed region in Fig. 2).

The results for these wafers are slightly below the frequency trend determined by Eq. 1 for AlO_x junctions, which indicates a higher C_f for the given J_c. Specifically, the 165 GHz speed of 5.5 kA/cm^2 NbSi devices compares to the 200 GHz speed for 4.5 kA/cm^2 AlO_x devices. If we assume that NbSi-barrier junctions follow the trend of Eq. 1, C_f must be 100 fF/μm^2, compared to 59 fF/μm^2 for the oxide barrier. In the future, it is important to test other NbSi-barrier junctions with different values of J_c to determine their actual speed performance. Because different compositions and barrier thicknesses can produce similar J_c, it is possible that the speed scales differently. In addition, a more straightforward test would be to compare

externally shunted NbSi junctions with externally shunted AlO_x junctions in which case C_f should be similar.

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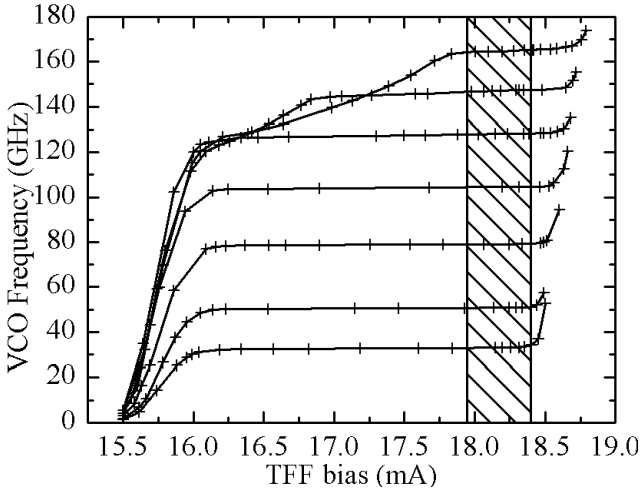

Fig. 2. Measurement of static divider for wafer B. VCO frequency is inferred by multiplying the output frequency by 2^{12}. The circuit shows operating margins up to 165 GHz.

Separately, a 16-bit SFQ counter-flow shift register was tested. The design, with 4 junctions per stage (similar to [15]) used parameters identical to a previously tested [16] version of the circuit based on AlO_x–barrier junctions. By omitting the external junction shunts, which are unnecessary for these NbSi-barrier junctions, the unit cell area was halved.

Two circuits from each wafer were measured. At the optimum designed bias current of 8.2 mA all circuits showed correct operation with the same experimental bias current margins of about ± 30 %. The measured margins agree with simulated results and are larger than the best reported margins of ± 23 % for similar devices based on AlO_x–barrier junctions [16]. The broader operating margins can be attributed to smaller spread in the NbSi junction properties.

The circuit was designed for low speed test with standard SFQ/dc converters. The experimentally measured waveforms shown in Fig. 3 were generated by shift register circuits from the two wafers and demonstrate the correct circuit operation. The measured output voltages of 0.05 mV and 0.13 mV correspond to the dc voltages on single junctions at biases near $1.5I_c$, which agrees with the designed bias and expected output voltage. Output voltages were sufficient for testing the shift registers up to 500 MHz and 1 GHz clock frequency for wafers B and C, respectively.

For C_f = 100 fF/μm^2, which was estimated using the maximum static divider frequency, and with effective V_cs of 0.37 and 0.67 mV measured from SFQ/dc converters, the effective

damping can be estimated to be $\beta_c \approx 0.8$ and $\beta_c \approx 2.6$, which agrees with damping parameters estimated from *I-V* curves measurements of single junctions.

The design with self-shunted junctions uses half the area and gives better uniformity of junction resistance than its externally shunted version based on AlO_x junctions. This could be a very important advantage in the case of complex circuits with more than 10^4 junctions, especially if the improvement persists to higher-speed devices.

This work presents the first high-yield digital circuits fabricated with intrinsically self-shunted Josephson junctions. The results suggest that silicide-barrier junctions may be a useful and important junction technology for high-speed digital circuits.

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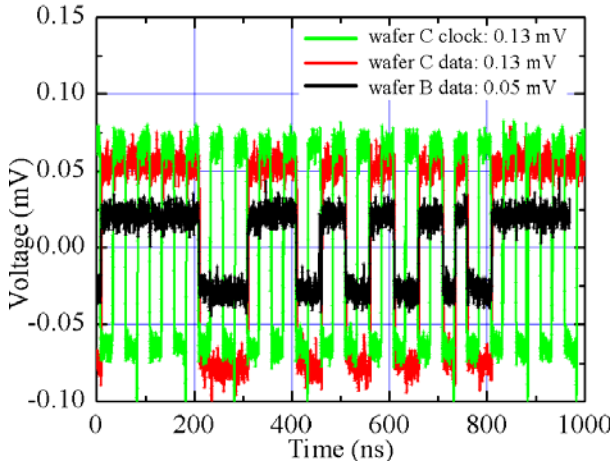

Fig. 3. Correct output waveforms for the 16 bit shift register are shown for an arbitrary data pattern at 40 Mb/s. The output voltage is 0.05 mV for wafer B and 0.13 mV for wafer C.

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