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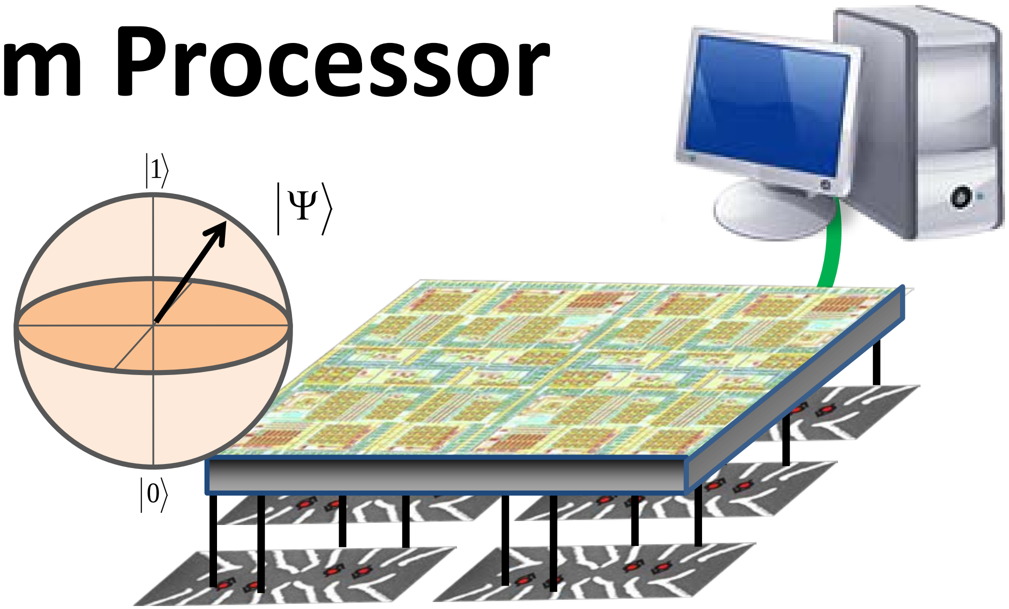
Design Considerations for Integrated Semiconductor Control Electronics for a Large-scale Solid State Quantum Processor



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Quantum Computing

Classical bits

0 or 1

N bits => 2^N states 0, 1, …, 2^N-1

Quantum bits

$\alpha|0\rangle + \beta\,|1\rangle$

N qubits: 2^N dimensional Hilbert space

$|0\rangle, |1\rangle, \ldots, |2^N\text{-}1\rangle$

Principles of quantum mechanics

⇒**Huge memory space**

⇒**Built-in parallelism**

⇒ **Exponential speedup** (for some problems)

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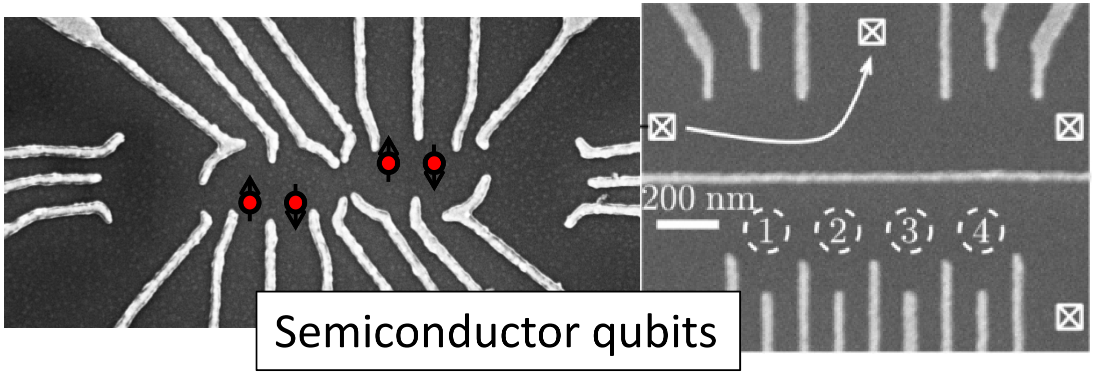
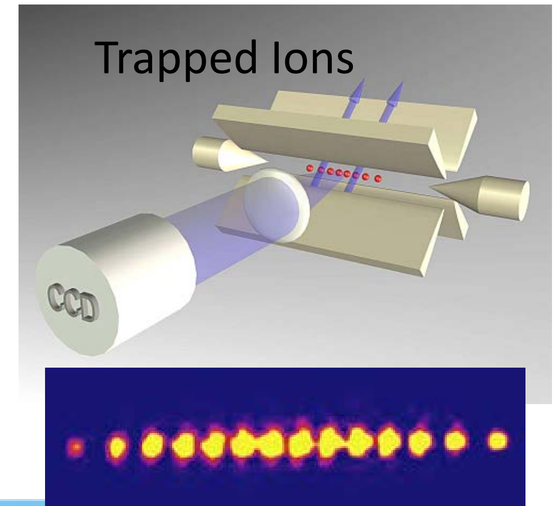
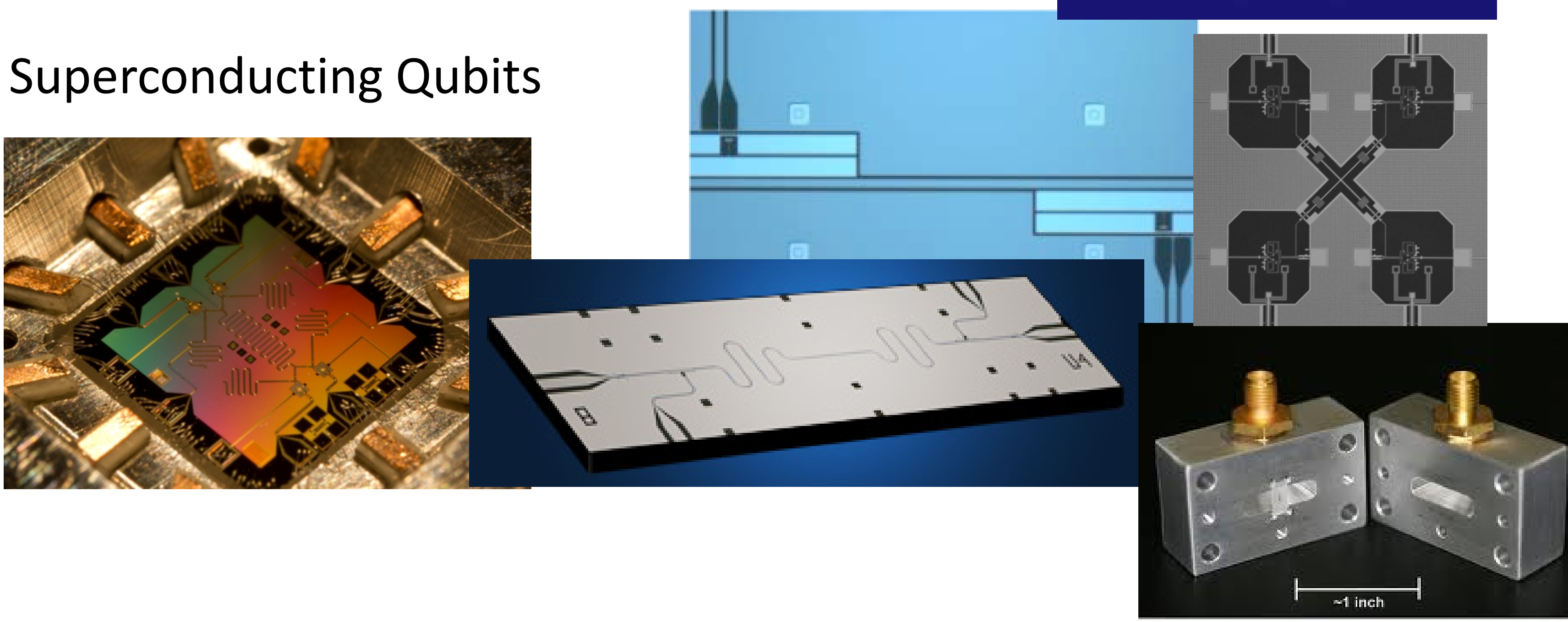
Qubit Zoo





Superconducting Qubits



Scaling Need for Applications

Predicted resource requirement

Prime factorization and decryption

5×10^8 qubits, 1 day for 1024 bit number

Quantum Chemistry

10^8 qubits, 13 days for $C_3H_7NO_2$

10^6 qubits for Fe_2S_2

- Catalyst design for CO_2 capture or fertilizer production
- Quantum material design

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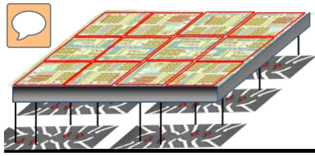


Quantum Computing Architecture

Requirements for surface-code error correction

- Lattice 2D nearest neighbor interaction
- Error rate < 10^{-3}

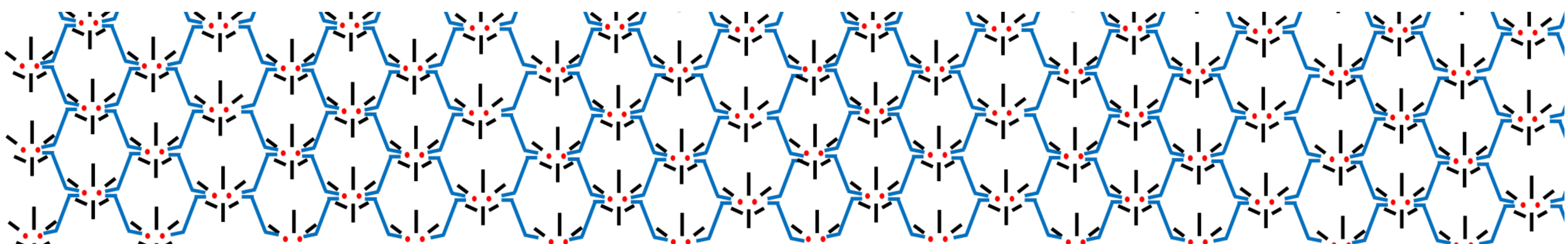
Resource needs for high impact computations

10000 logical, error corrected qubits

x 1000 physical qubits per logical qubit

<u>x 10 overhead to work around drawbacks of error correction</u>

= 10^8 qubits



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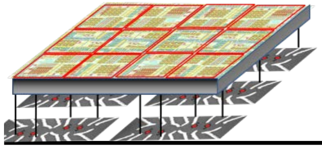
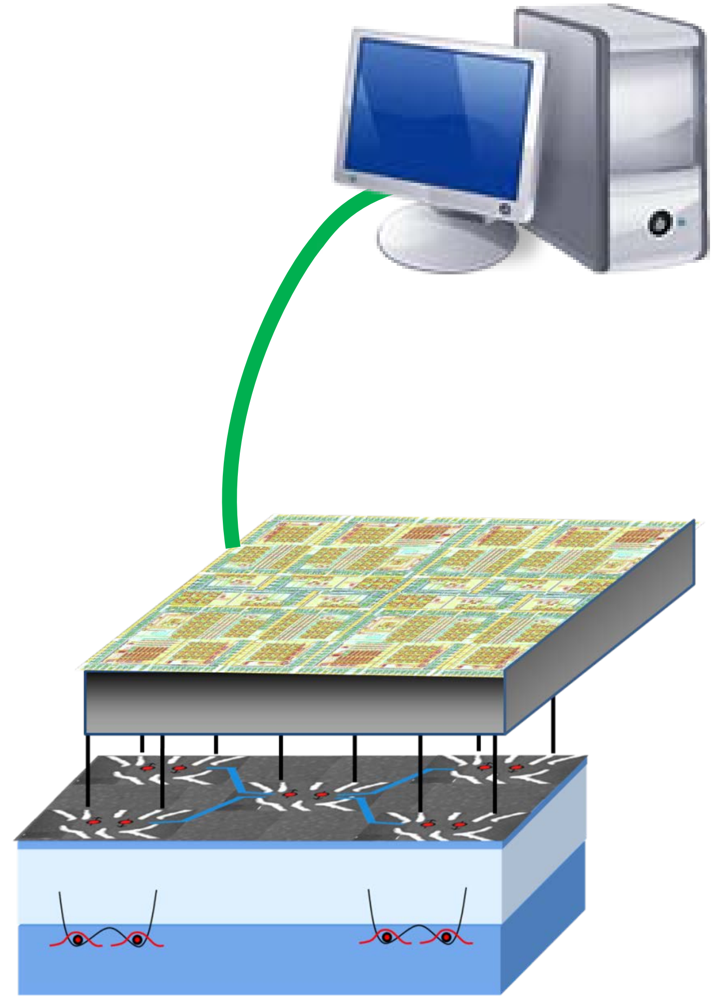


Outline



Requirements for scalable quantum computing

Vision of a scalable quantum processor

Ultra-low power control electronics

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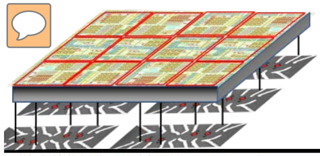
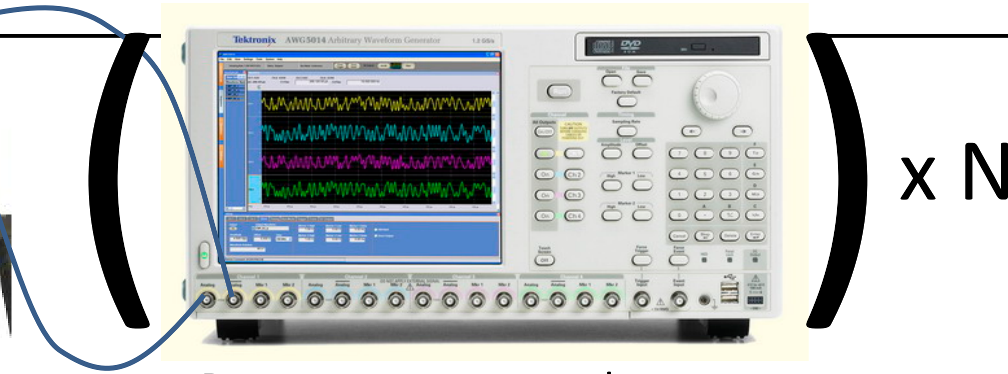


Brute Force Approach



Room temperature pulse generator

Scaling limitations

Control electronics
Thousands of racks

Wiring
1 coax cable per qubit
=> 1 m^2 scale wiring cross section
for 10^6 qubits

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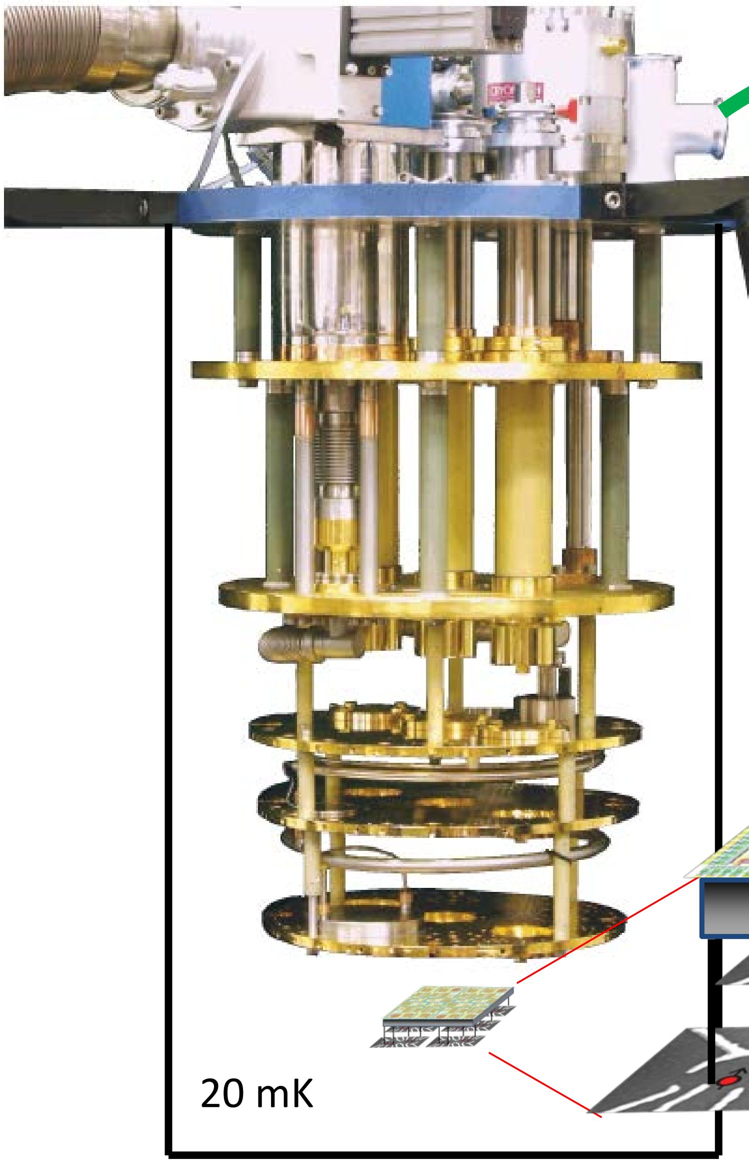
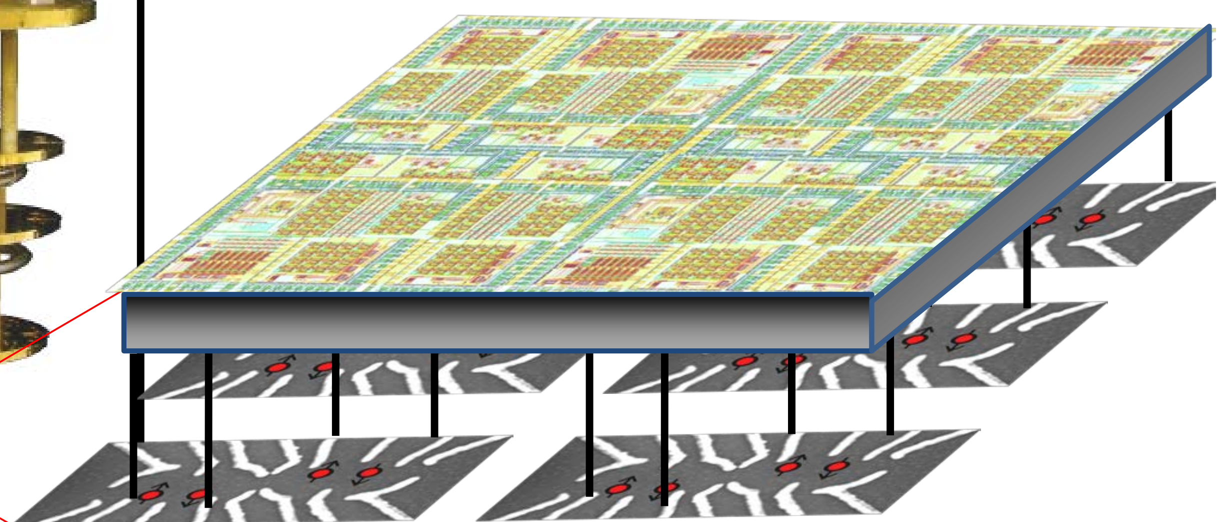
Vision of a Scalable QC



Fully integrated semiconductor quantum processor with low-power integrated control logic



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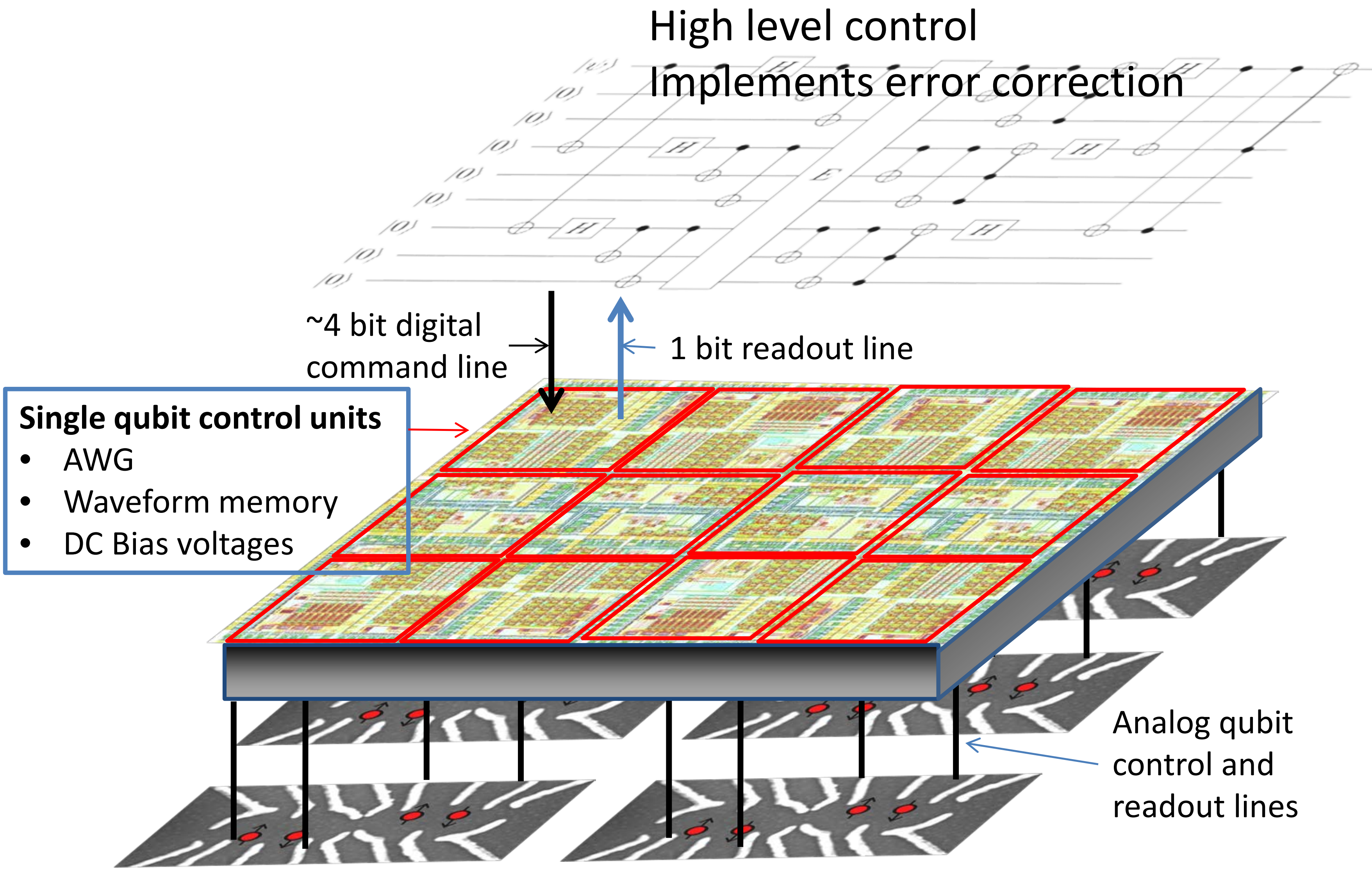
Low Level Architecture



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(Cooling) Power Budget

Premise: qubits operated at < 1 K

High cooling power, but hardly better than room temperature

4 K, 5 W

Still: 0.7 K, 100 mW

Likely most relevant for control electronics

Qubit level: 100 mK, 1 mW.

=> Can dissipate at most a few nW per qubit

Useful Circumstances

- Operation at $\lesssim$ 1 K
  => S = 0.2 mV/decade (Thermal limit. Disorder ?)
  => High mobility
  Use $V_{dd} \approx$ 10 mV (set by required output amplitude and speed)

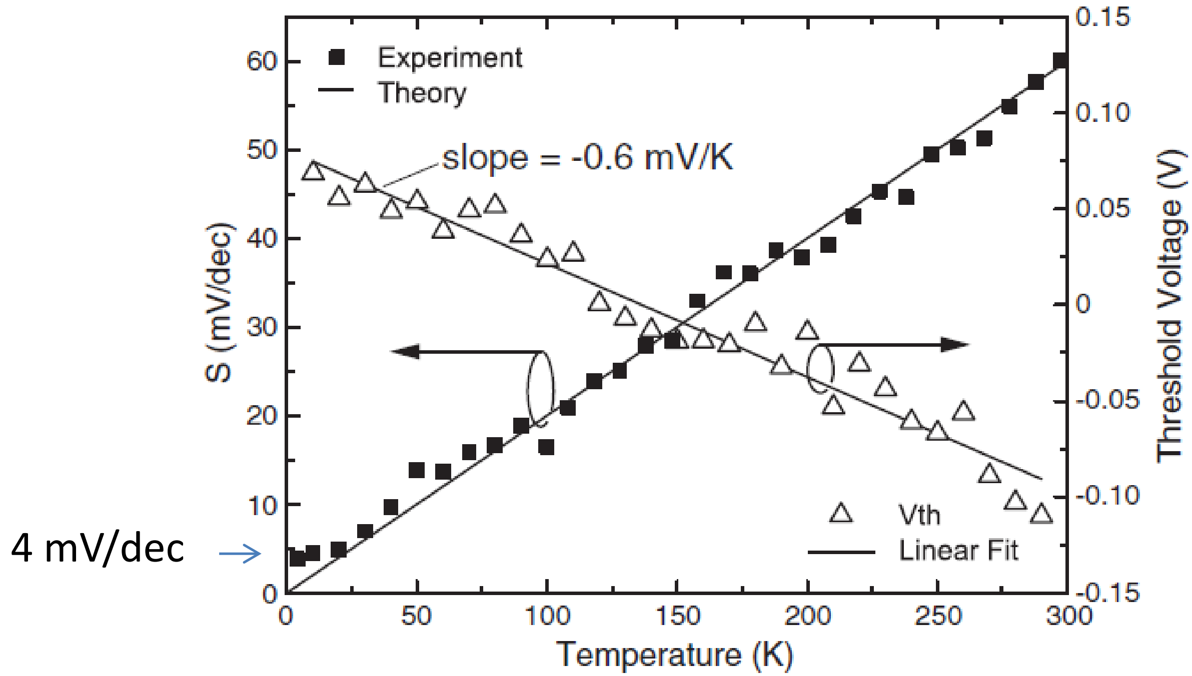
=> Could operate at 10^{-10} W per transistor (at f = 1 GHz, C = 1 fF)

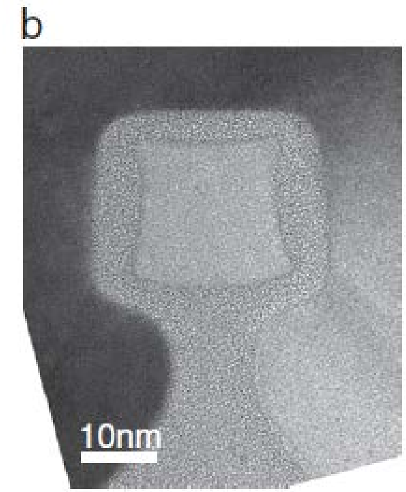
- Low leakage

- Purely capacitive loads (~ fF scale) a few microns away
  => No power-hungry signal transmission

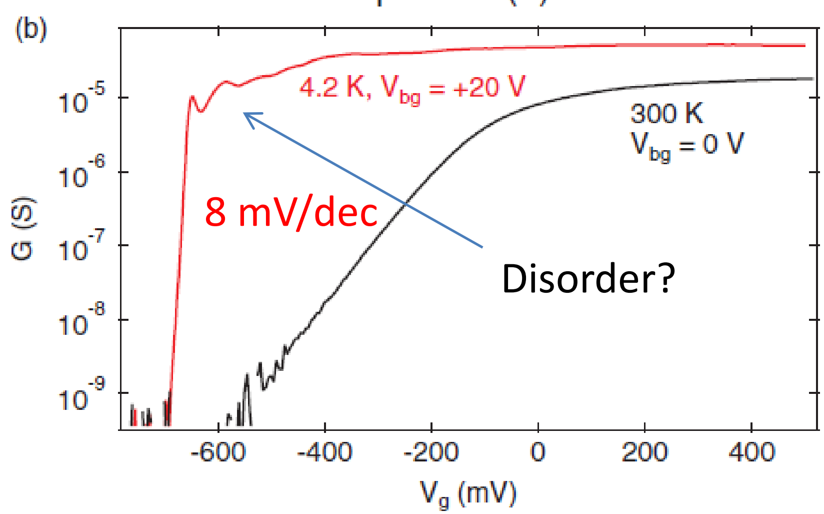
- Superconducting wires
  => Low dissipation, good thermal barriers.

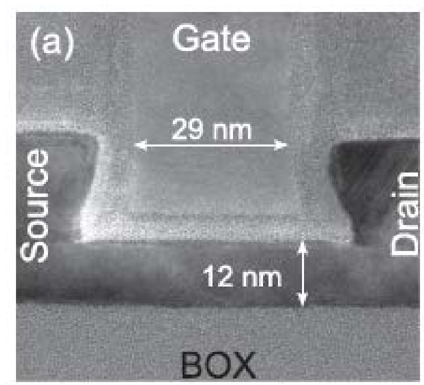
Steep Slope Transistors





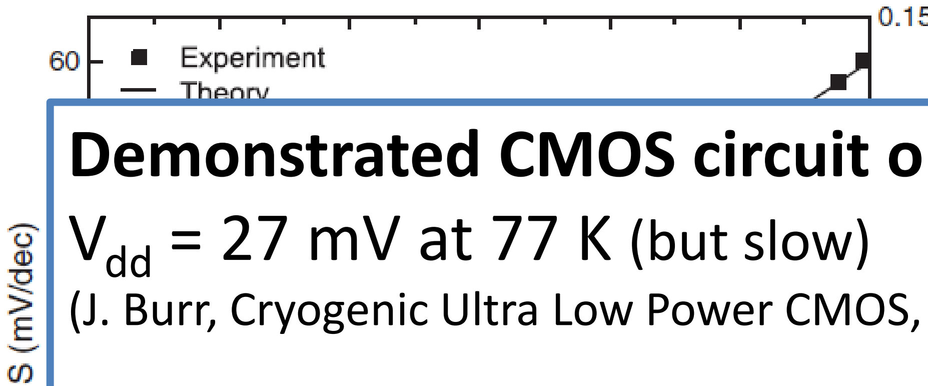
S. Habicht et al., Thin Solid Films **520**, 3332 (2012)

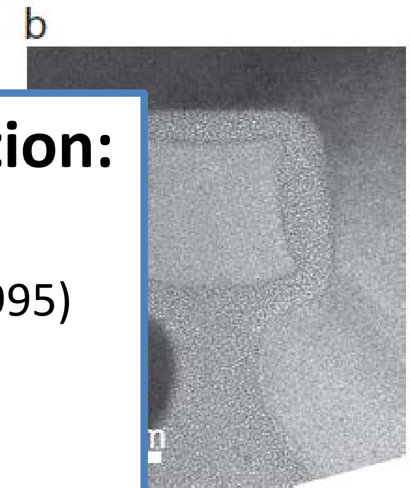




B. Roche et al. App. Phys. Let **100**, 032107 (2012)

Steep Slope Transistors





Demonstrated CMOS circuit operation:

V_{dd} = 27 mV at 77 K (but slow)

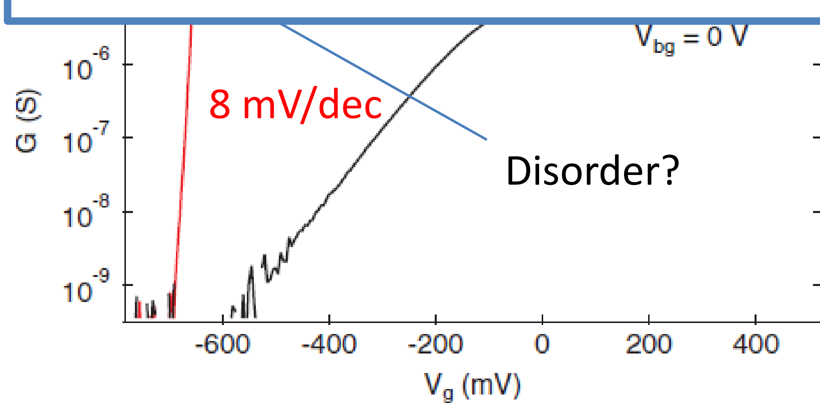
(J. Burr, Cryogenic Ultra Low Power CMOS, IEEE 1995)

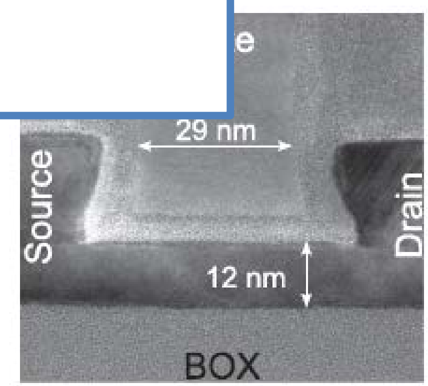
Possible issues

- Variability?
- Disorder limitation?
- Tuning of threshold voltage

4 mV/dec

…et al., Thin Solid …332 (2012)





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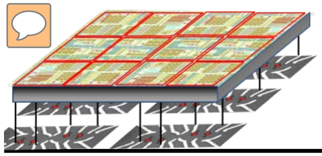
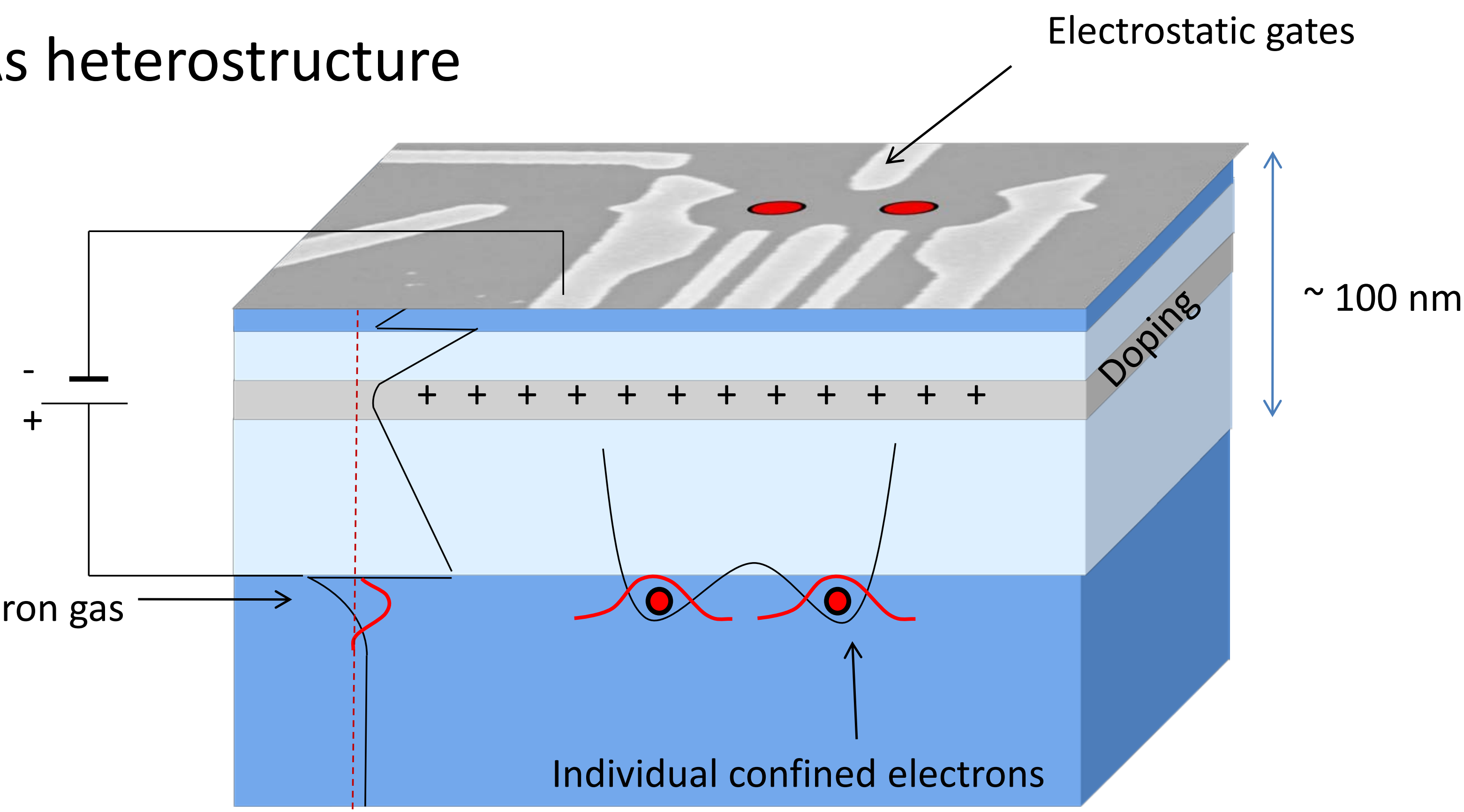


Gate-defined Quantum Dots

GaAs heterostructure



Scalable top down fabrication with standard lithography

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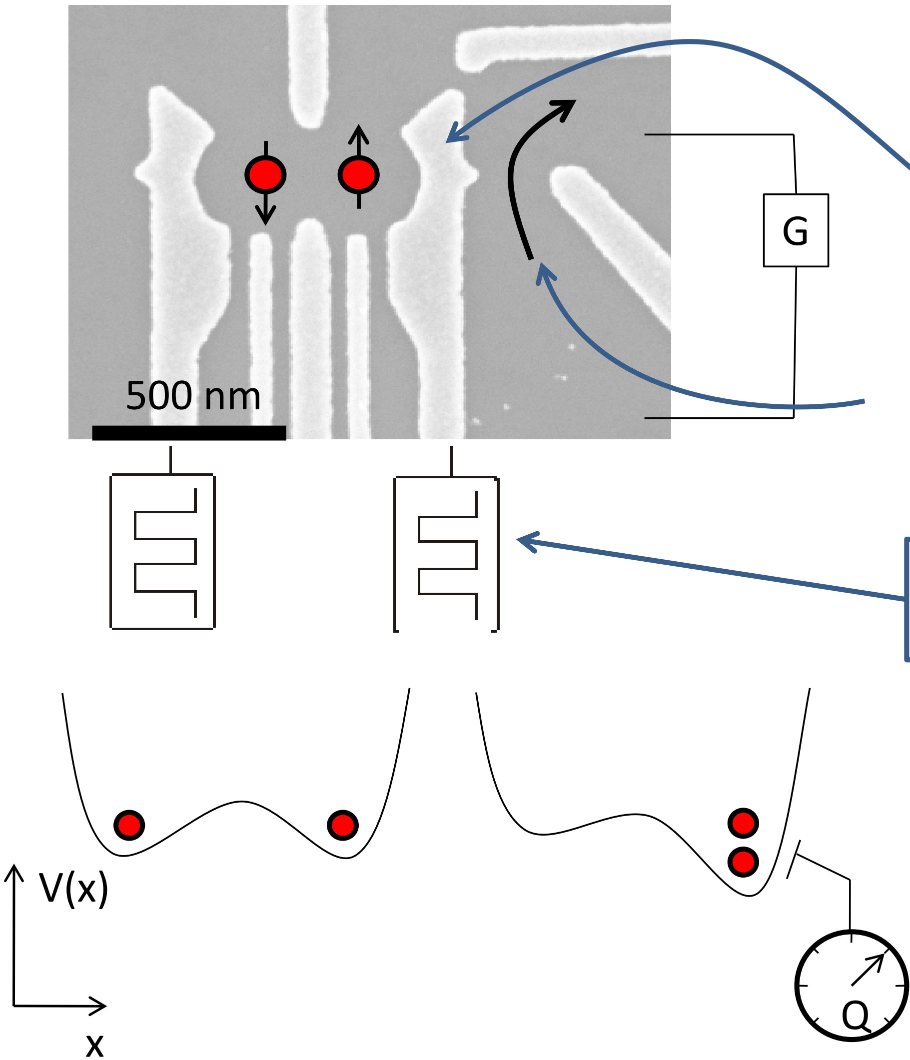
Control of Two-electron Spin Qubits

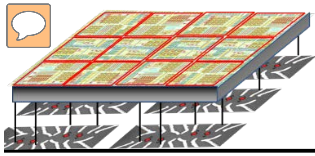


Resources needed

1 V level DC voltages to define and tune qubit

For readout: charge sensing
= 100 kΩ conductance measurement at 100 μV / 1 nA bias

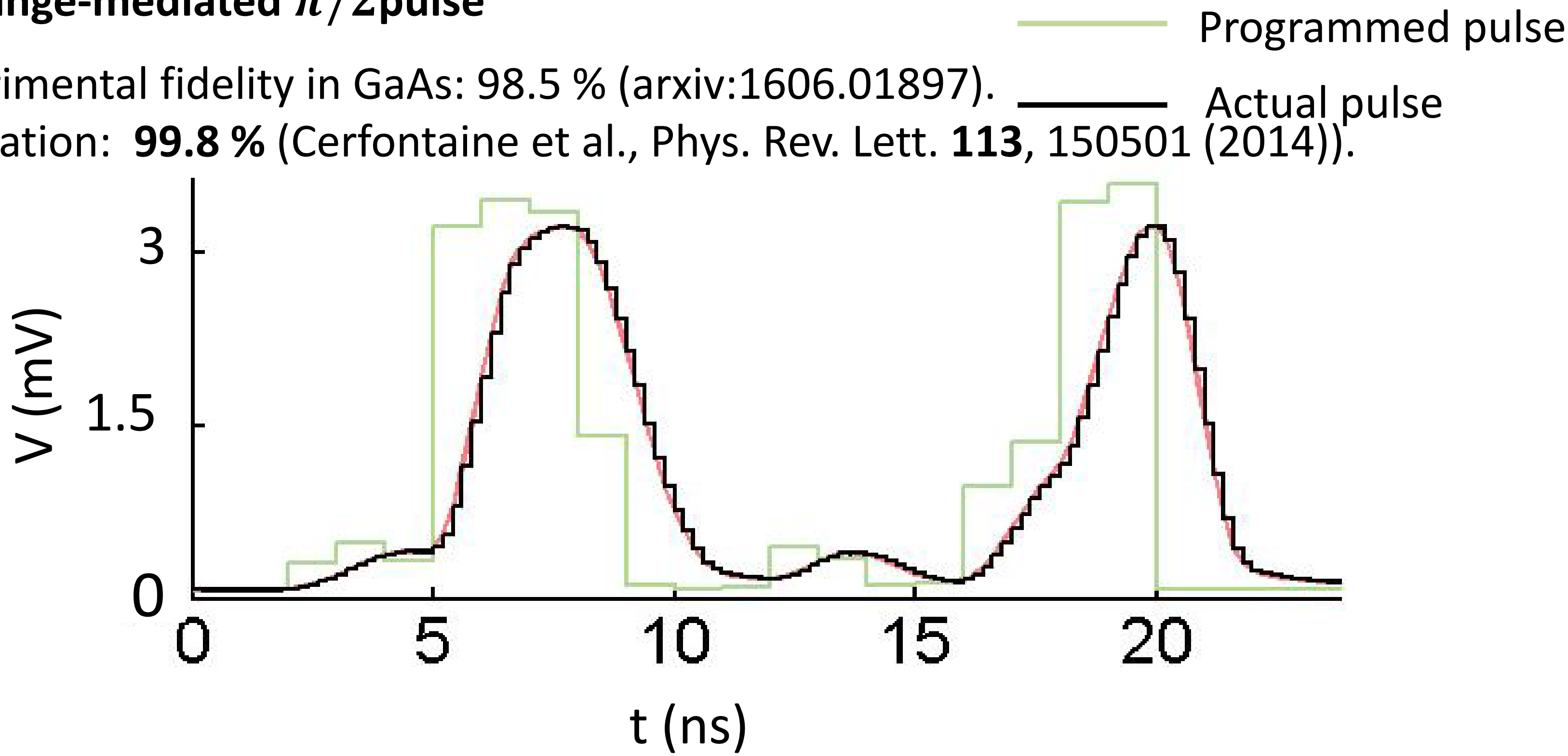
ns scale, mV level gate pulses for control



Anatomy of a Control Pulse

Exchange-mediated $\pi/2$pulse

Experimental fidelity in GaAs: 98.5 % (arxiv:1606.01897).
Simulation: **99.8 %** (Cerfontaine et al., Phys. Rev. Lett. **113**, 150501 (2014)).



Hardware requirements:

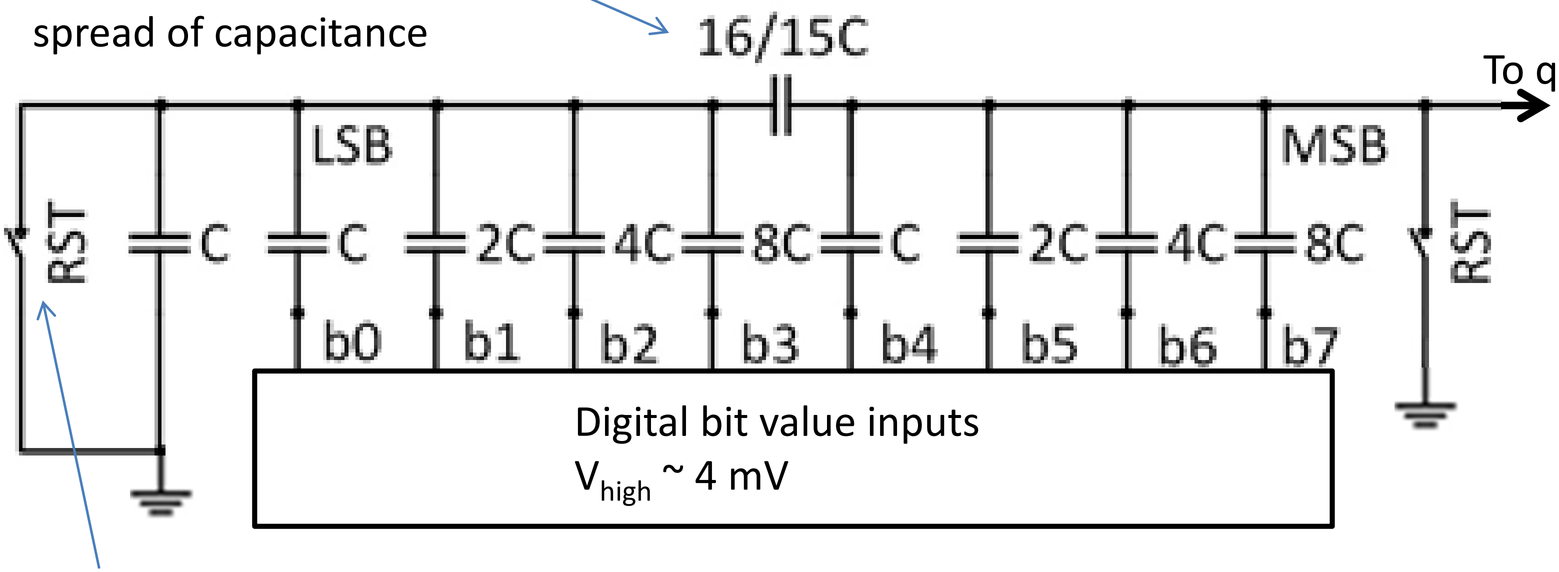
1 GS/s (could be reduced to ~ 300 MS/s)
5 mV output
~ 8 bit resolution
~ 16 samples per gate

Low Power DAC Concept

Capacitive voltage division

- No quiescent current
- No need for large integrated resistors
- Less senstive to channel resistances than resistive division

Decoupling capacitor for lower four bits reduces spread of capacitance



Reset switches to compensate for leakage

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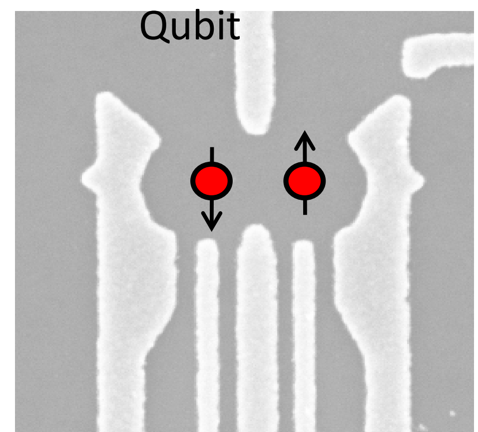
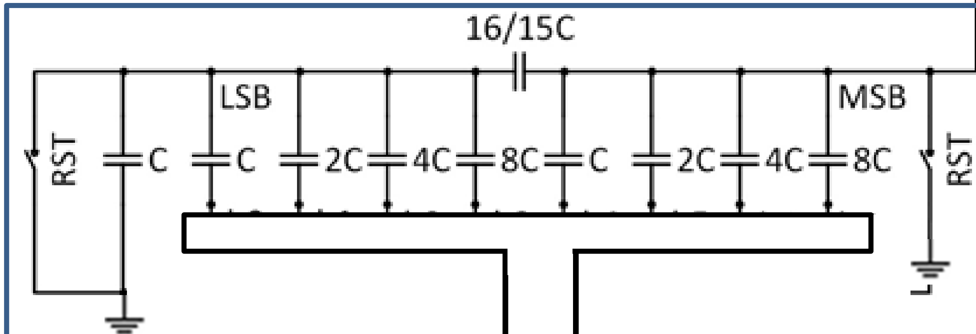
AC Control System

High level control

Instruction bus

DAC (~ 300 MS/s)





Memory
8 bit
16 samples per instruction
<u>16 instructions per qubit</u>
2 kbit per channel

All in ultra-low power cryogenic CMOS

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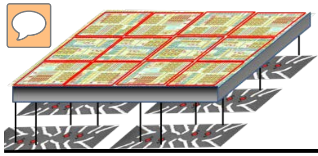
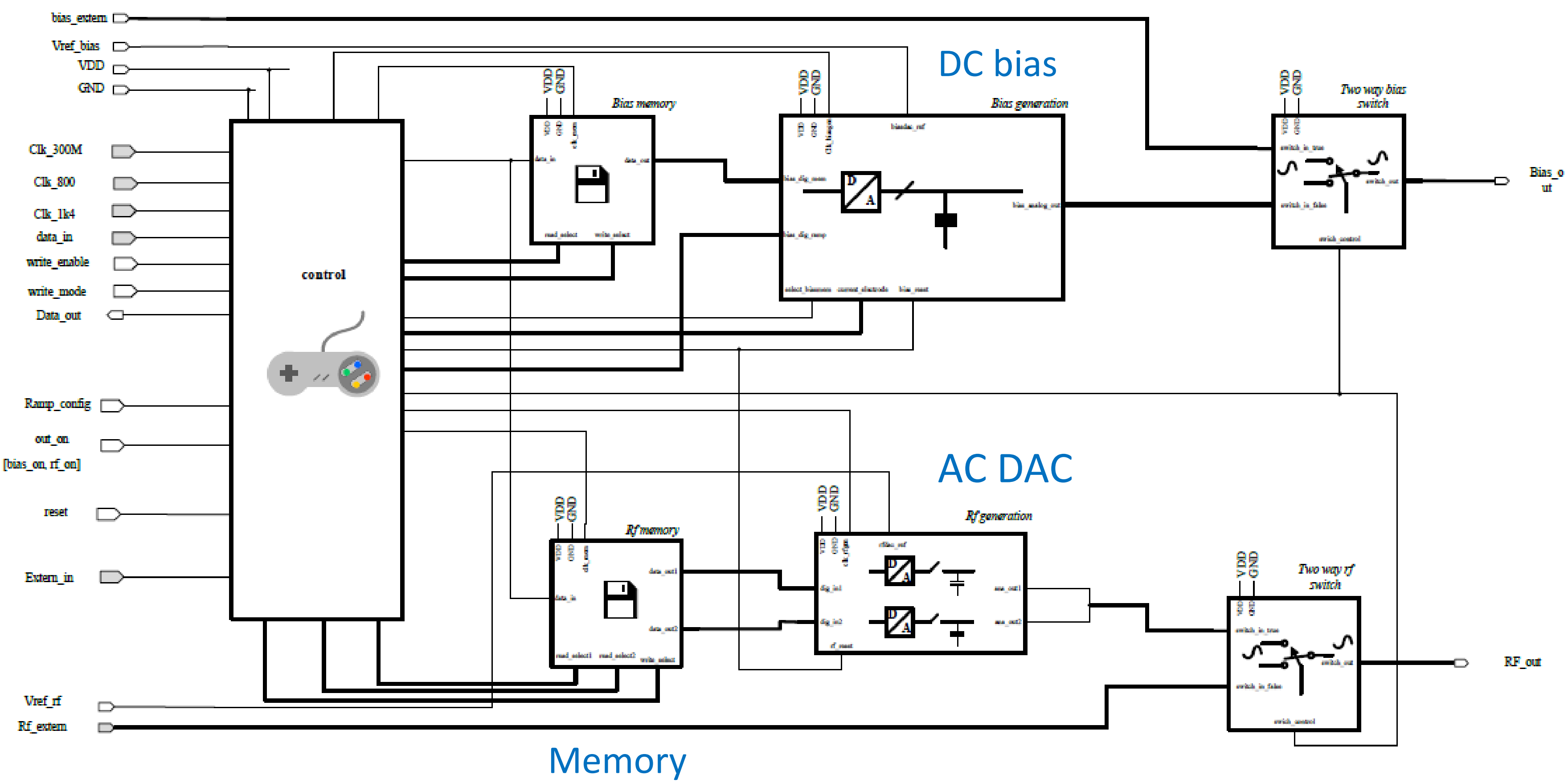


System Level Design Study



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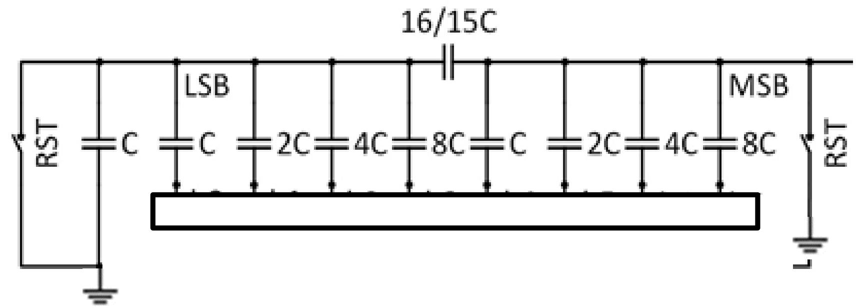
Noise and Size



Thermal noise

Output capacitance

$$= 16\,C \geq \frac{k_B T}{\langle \delta V^2 \rangle} = 0.5\ \text{fF}$$

for 0.2 nV/Hz output noise and T = 0.2 K

Corresponds to 500 µm² with 2 fF/µm² technology for DAC capacitors.

Transistor count

37.000 in control unit

<u>36.000 for 2 kBits of memory</u>

14.000 µm² = 120 x 120 µm at 0.25 µm² per transistor.

=> Unit nearly small enough

Power and Speed

Power dissipation (DAC only)

$$8\,C f_{samp}\,V_{dd}^2 = 2\text{ nW}$$

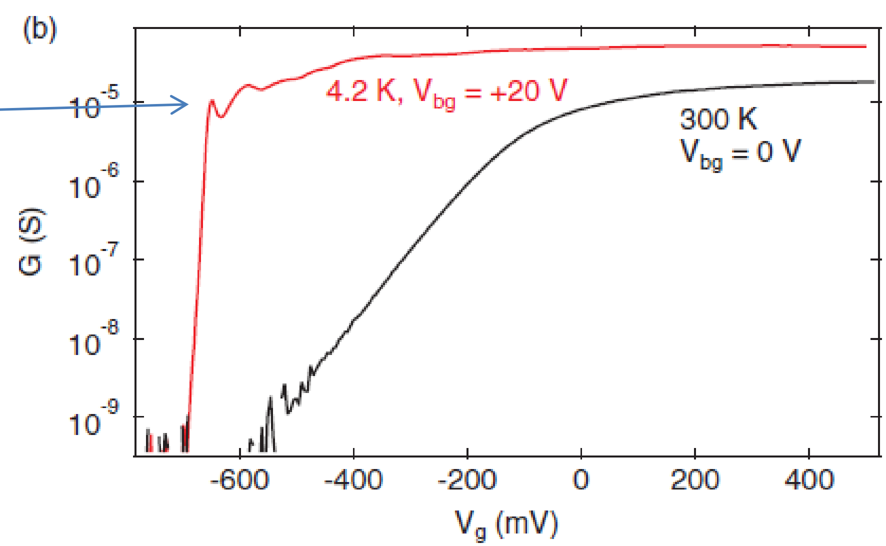
at $f_{samp} = 300\text{ MS/s}, V_{dd} = 4\text{ mV}$

Switching speed

$R_{channel} = 100\text{ k}\Omega$
$C_{\max} = 4\,C = 0.13\text{ pF}$
=> $\tau_{RC} = 13\text{ ns}$

=> Needs factor 10 improvement compared to this unoptimized device

B. Roche et al. App. Phys. Lett **100**, 032107 (2012)



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Conclusion

- Integrated qubit control poses challenging but not impossible requirements on classical control circuits

- ~ 1 nW per qubit seems possible at low T seems possible, but requires a lot of rethinking, e.g.:
  -New transistors or different optimization targets
  -Specialized circuit designs

Outlook

- Similar concept also suitable for DC bias

- Could potentially be extended to microwave Rabi control with ultra low power modulators
  => Applicable to other qubit types