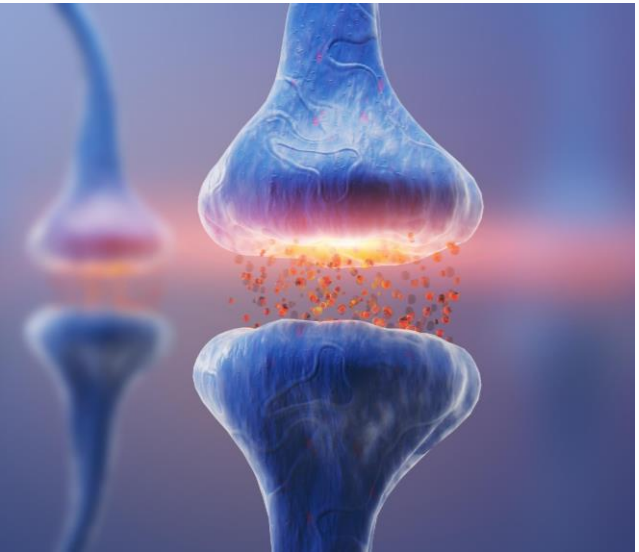
IEEE-CSC, ESAS and CSSJ SUPERCONDUCTIVITY NEWS FORUM (global edition), Issue No. 56 Sept 2024. Presentation given at WOLTE-16 2024, June 2024, Cagliari, Italy.

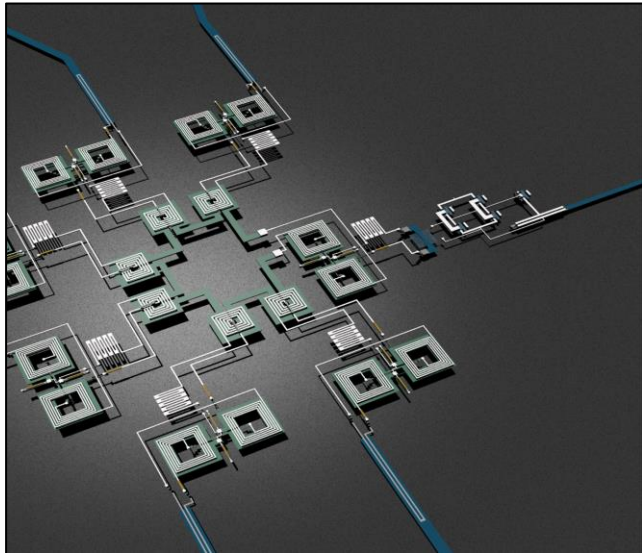
Superconducting Optoelectronic Circuits for Neuromorphic Computing



The NIST Physics and Hardware for Intelligence team

Presented by: Bryce Primavera

Workshop on Low Temperature Electronics (WOLTE16)
June 06, 2024
Cagliari, Italy



SOENs

Superconducting Optoelectronic Networks

Light for spike-based communication

Superconductors for computation and memory

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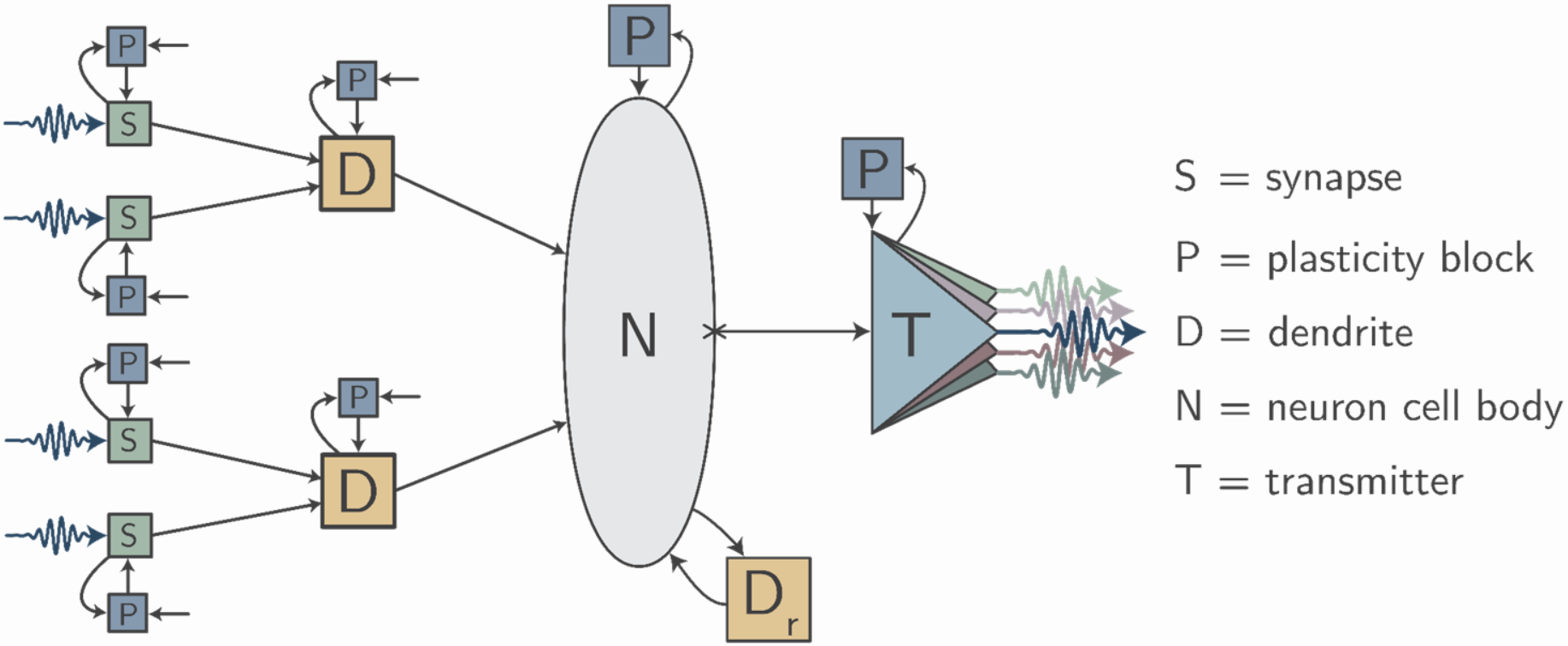
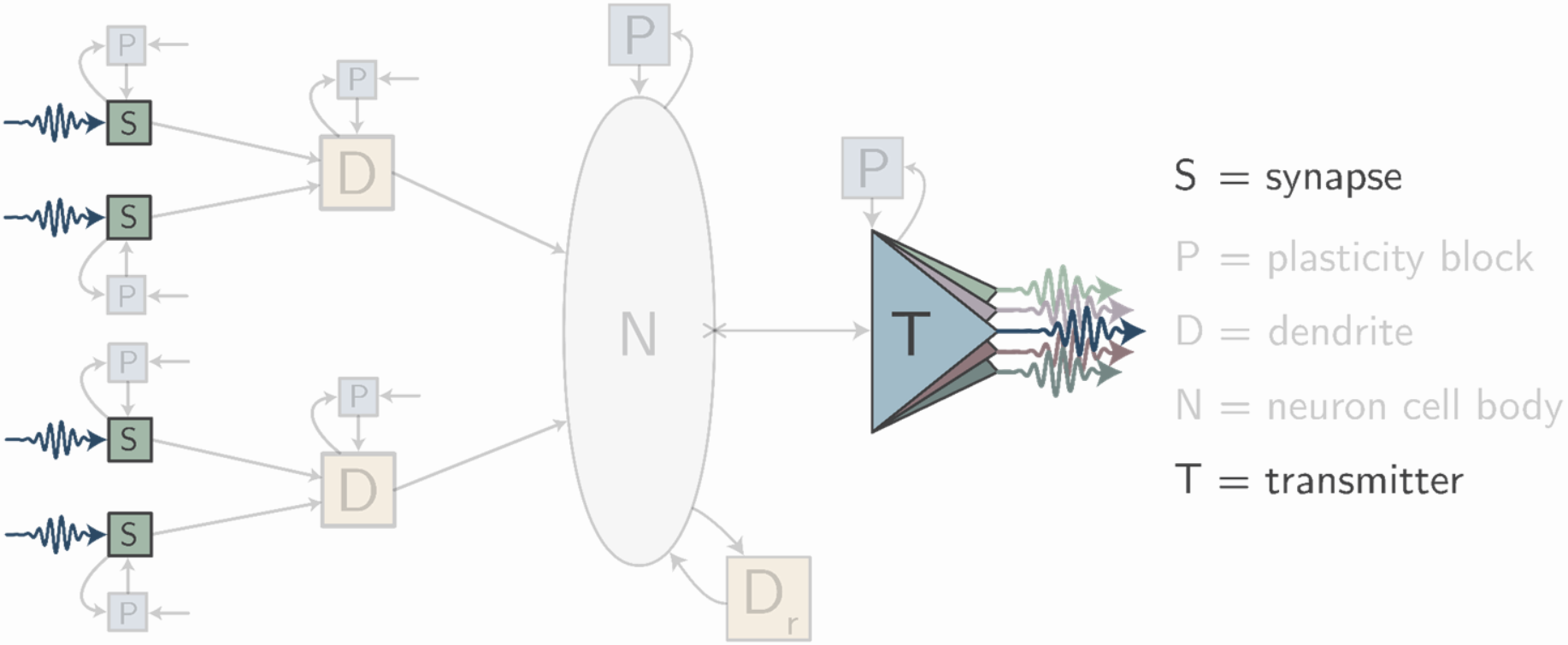
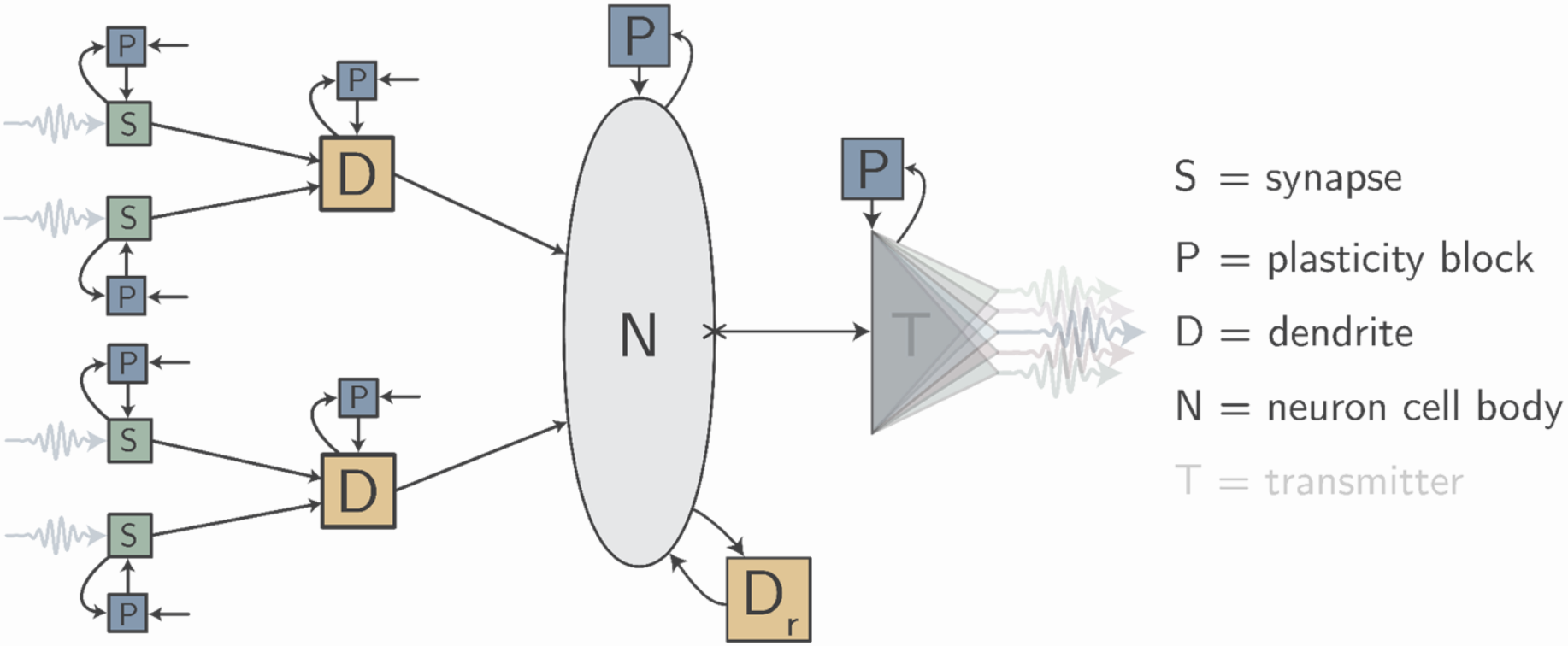
Superconducting Optoelectronic Neuron



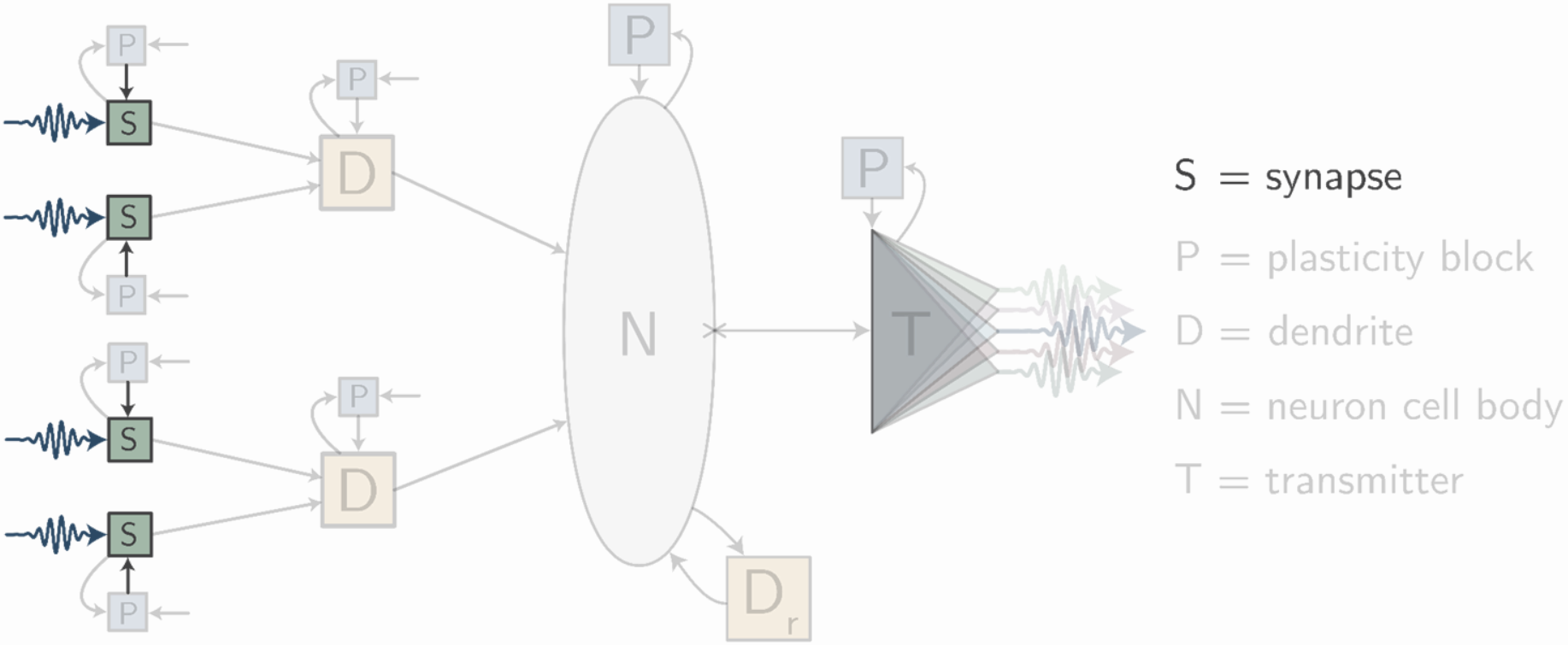
Optical Communication



Superconducting Computation and Memory



Part One: Synapses



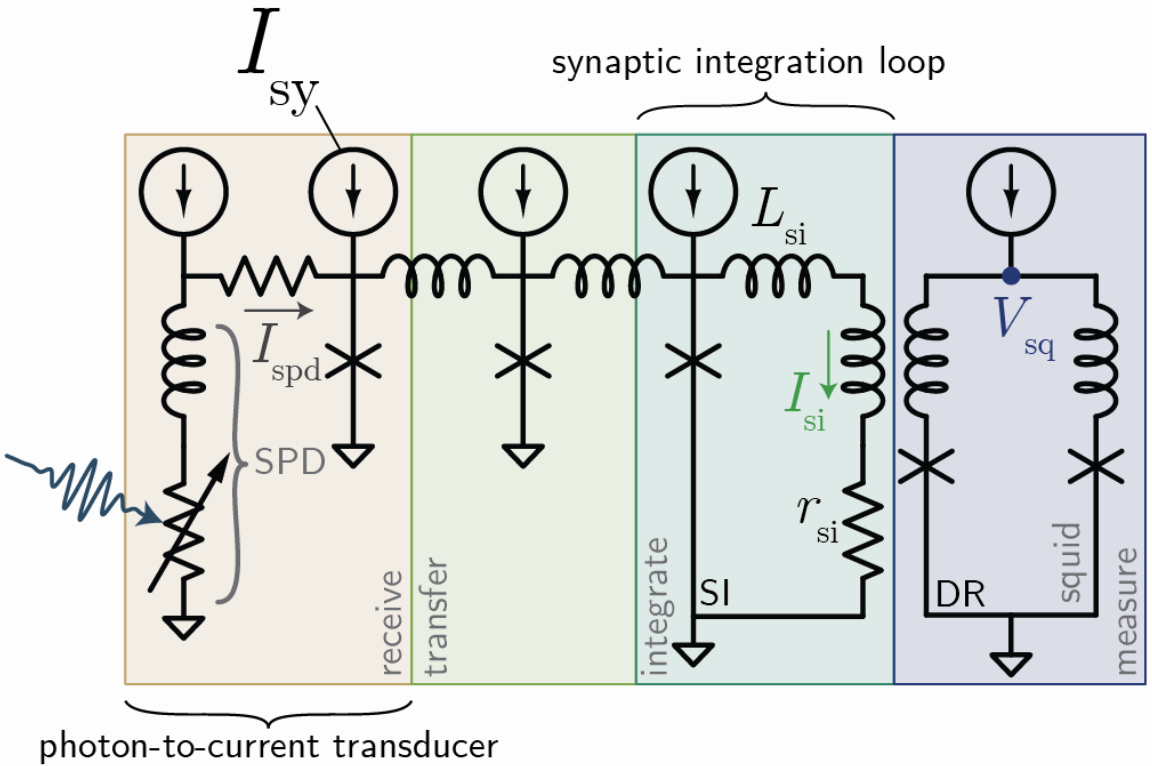
Synapse Circuit

Desired Qualities

Single photon sensitivity

Tunable synaptic weight

Leaky integration of synaptic signals



Khan, Primavera et al., Nature Electronics (2022)

Synapse Circuit

Desired Qualities

Single photon sensitivity

Tunable synaptic weight

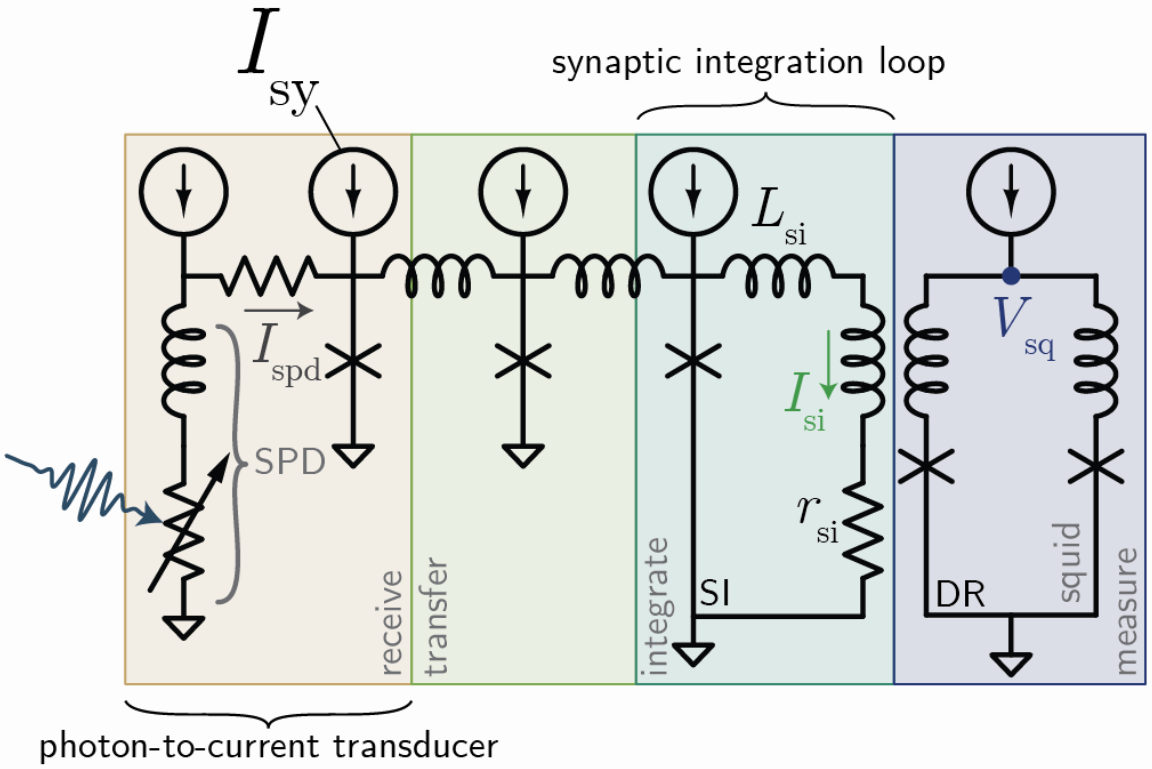
Leaky integration of synaptic signals

Operation

SPD drives JJ over I_c upon photon detection

Current is integrated in SI loop

On-chip SQUID readout of I_{si}



Khan, Primavera et al., Nature Electronics (2022)

Fabrication

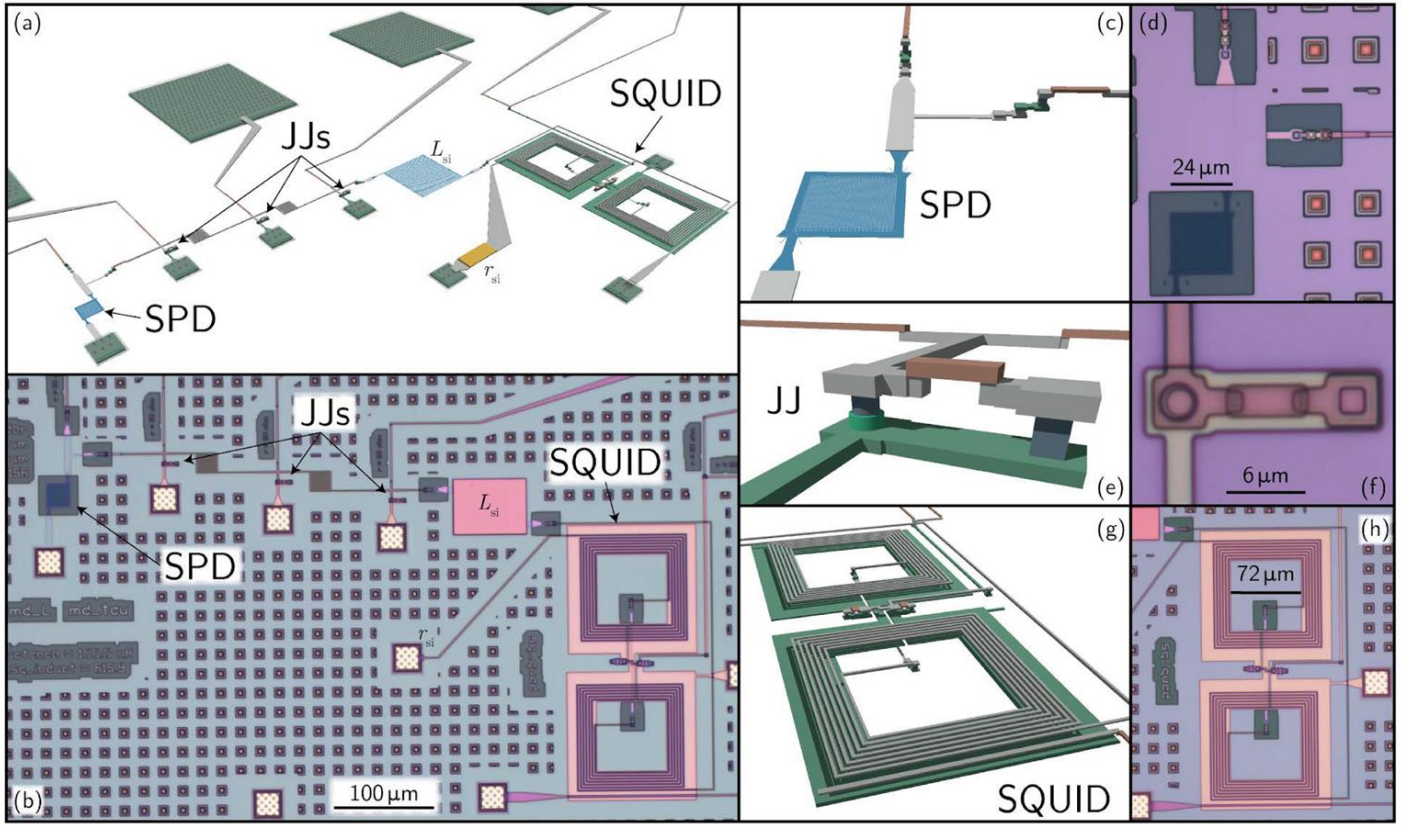
NIST JJ-SPD Process

14 layers

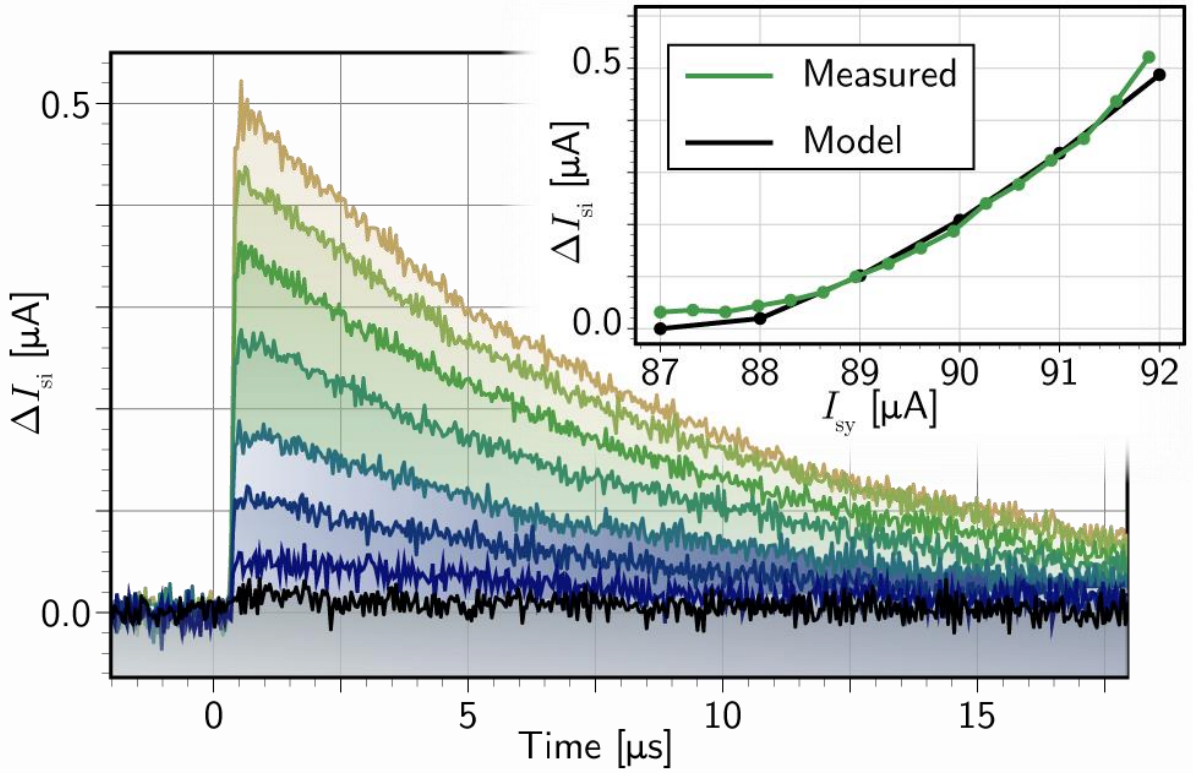
MoSi SNSPDs (2.3 K)

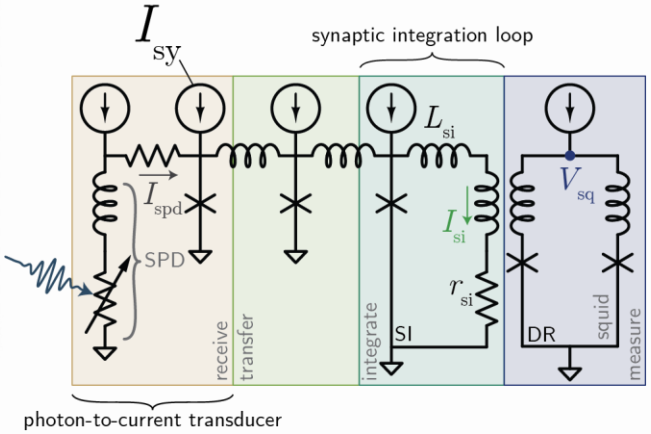
Nb/a-Si/Nb JJs

MoSi storage inductors

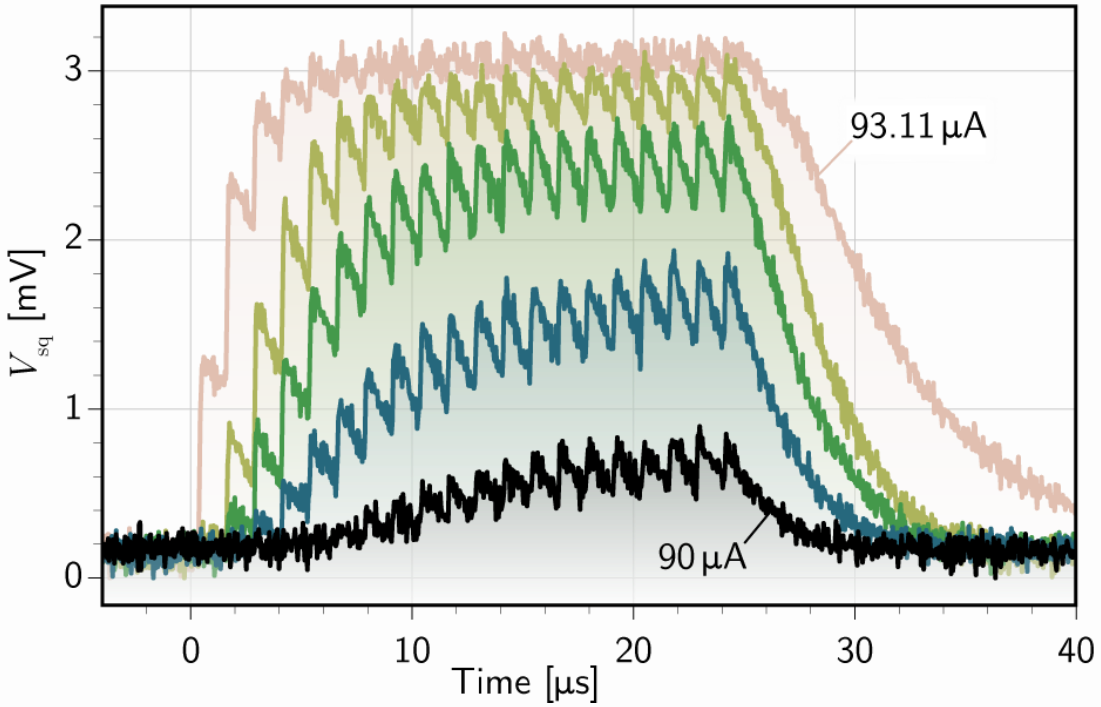


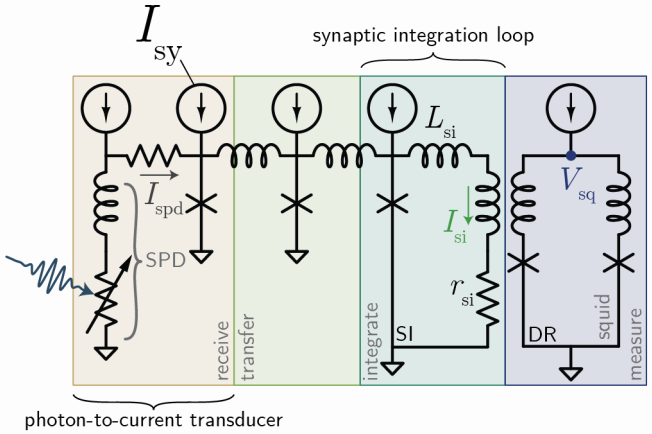
Synaptic Weighting



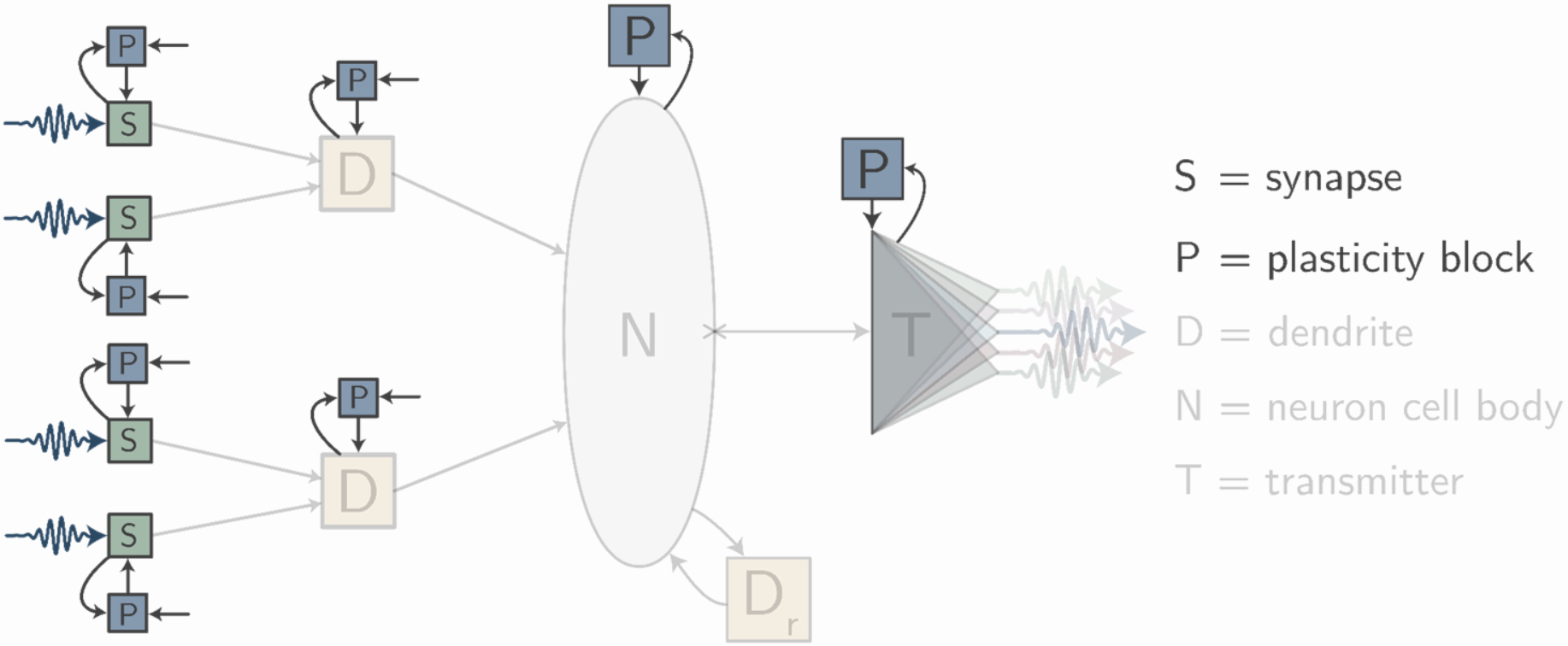


Weighting and Integration





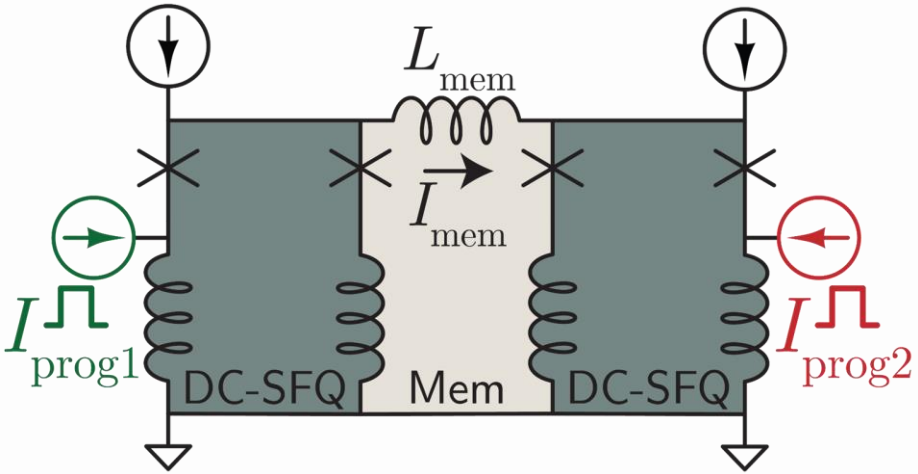
Part Two: Memory and Programmability



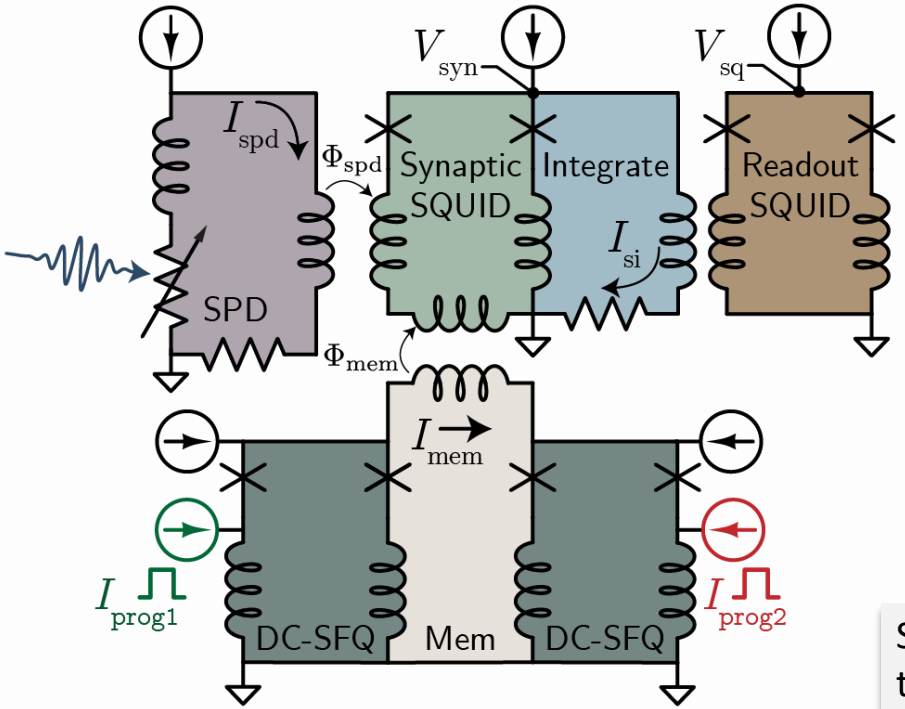
Integrated Superconducting Memory

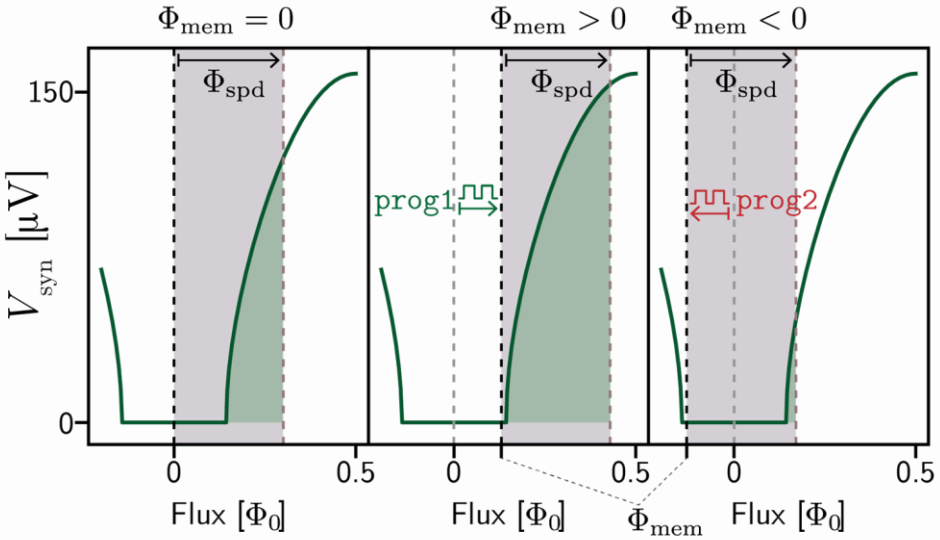
External current biases are not a scalable solution to synaptic weighting

Can we use the quantization of magnetic flux in superconducting loops as a local, multi-state synaptic memory?



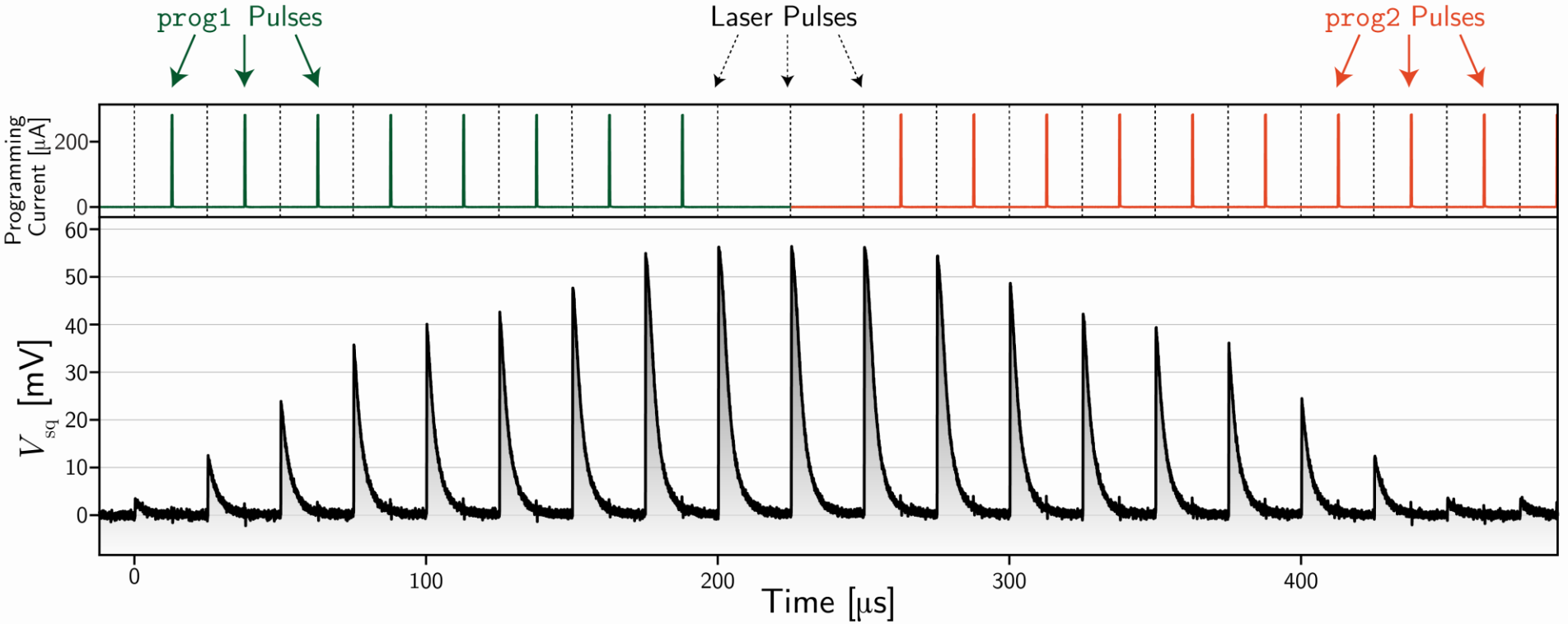
Programmable Synapse Concept





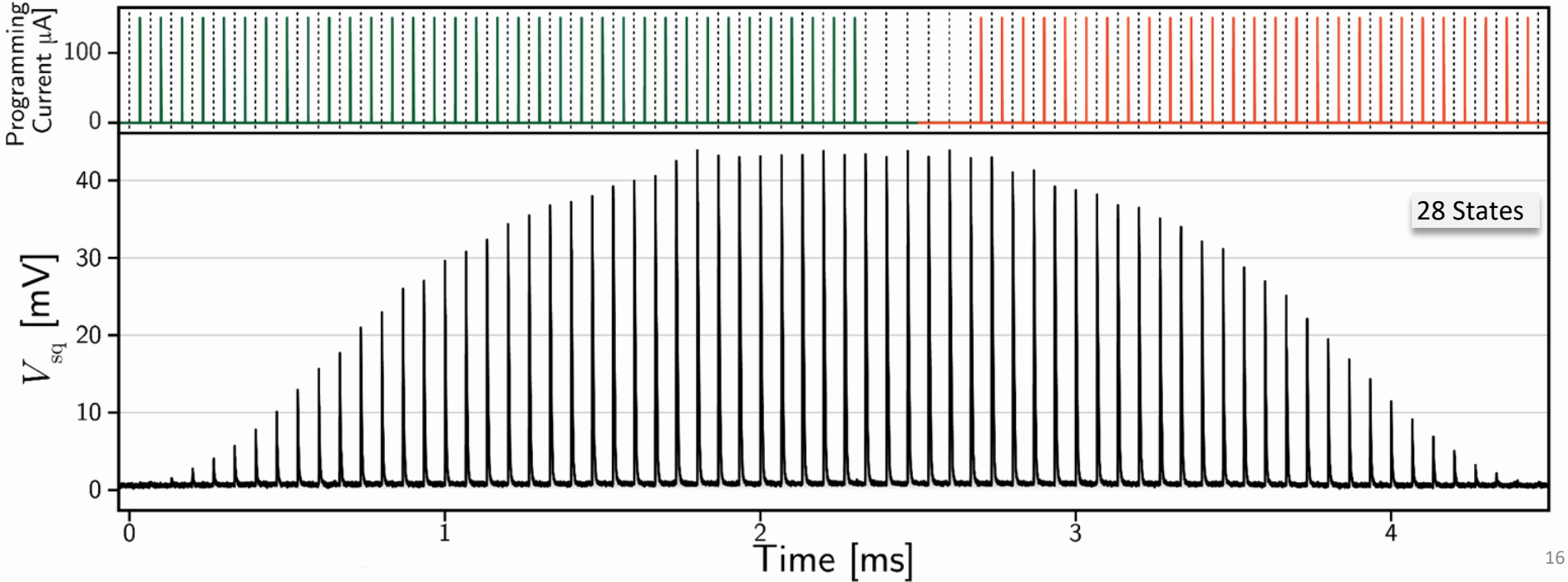
Synaptic weight is set by a flux bias from the memory cell to the synaptic SQUID

Programmable Synapse

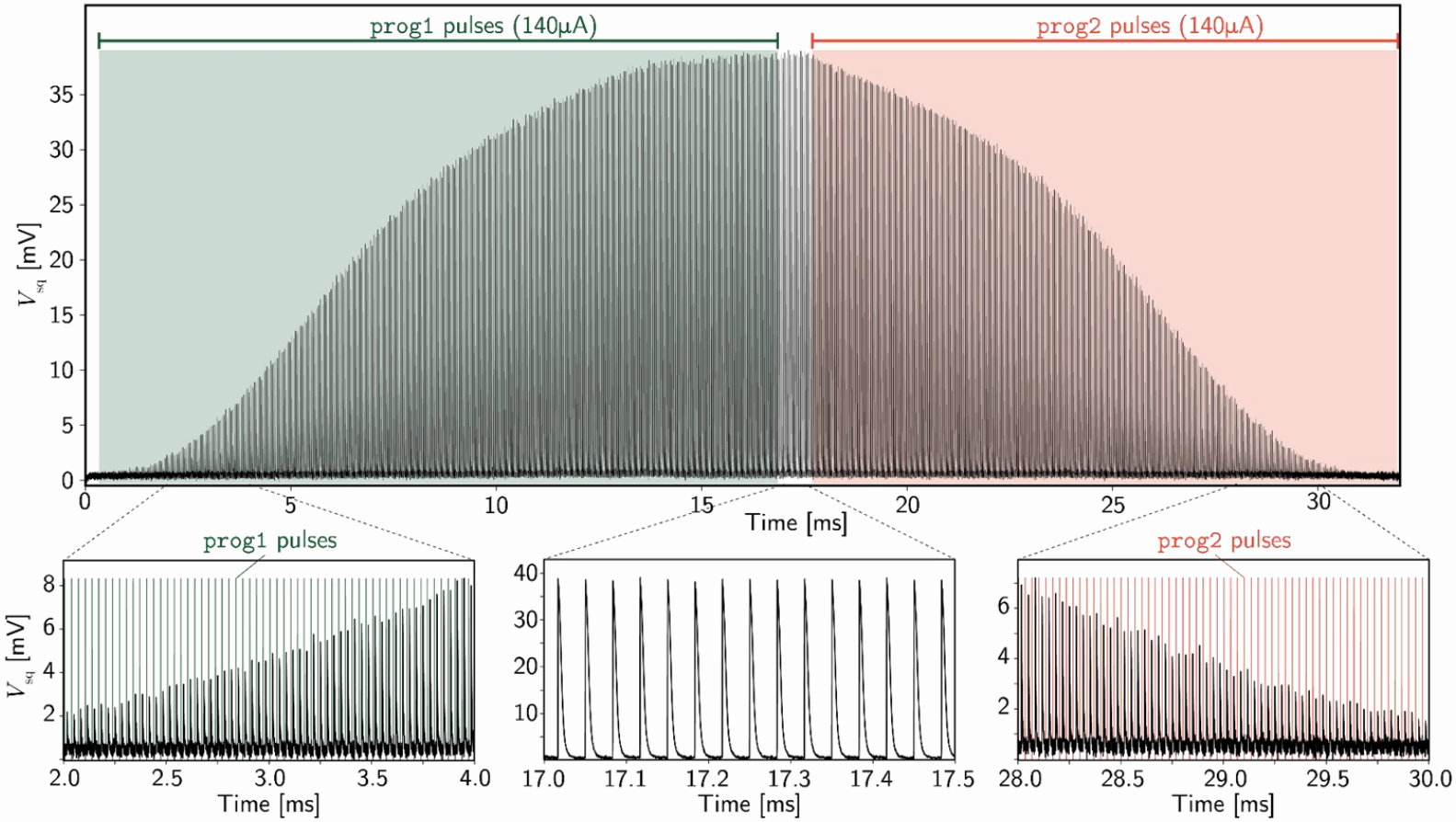


Programmable Synapse

The number of states is set by the inductance of memory loop



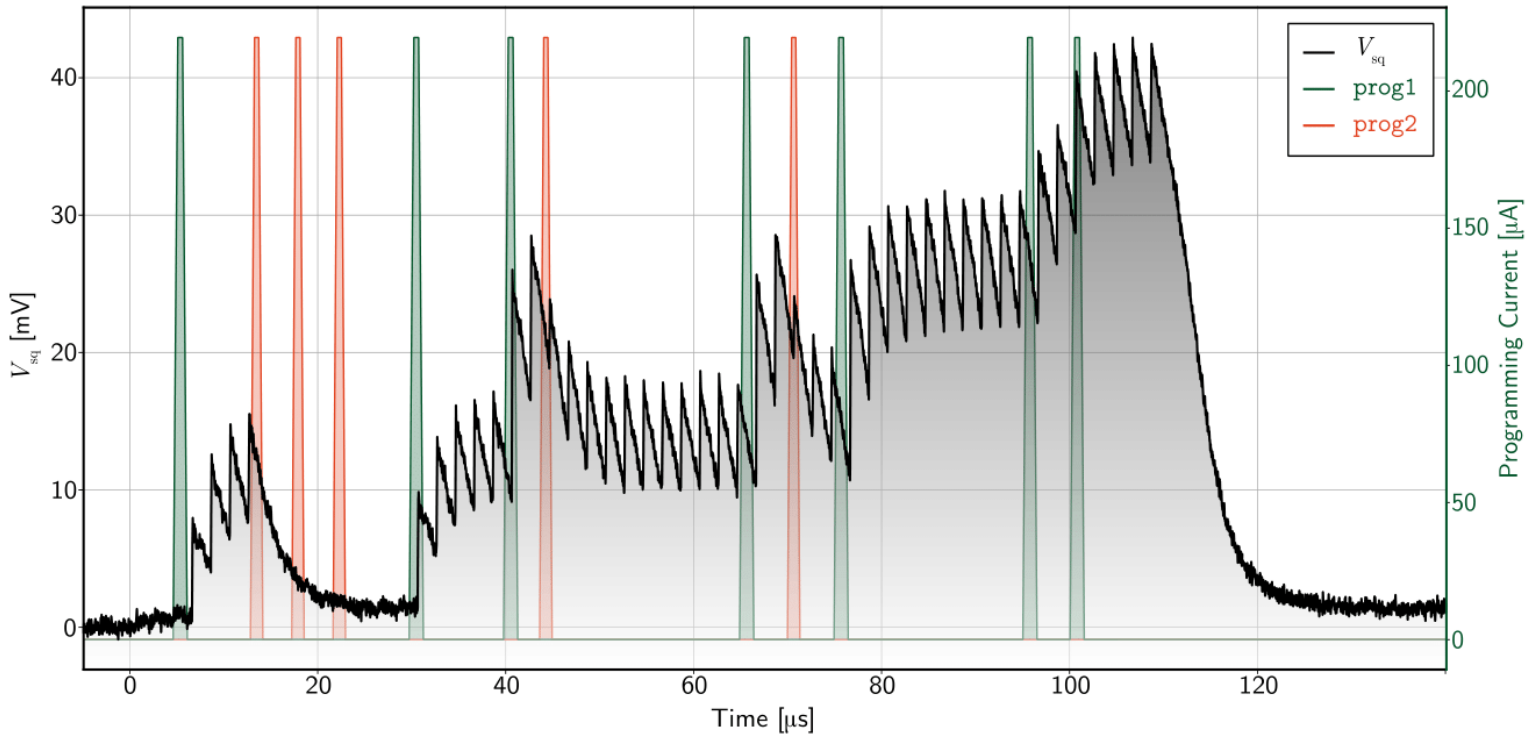
Programmable Synapse



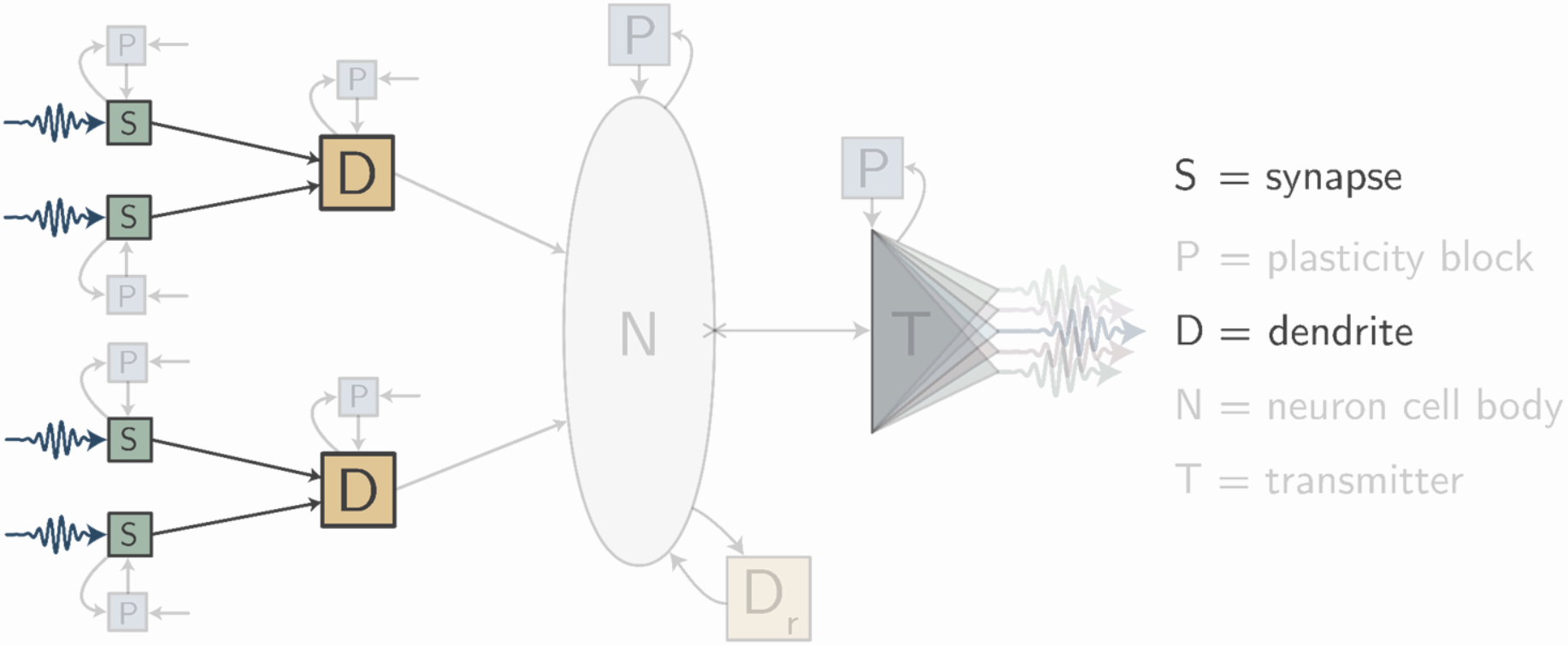
“On-the-Fly” Programming

Synaptic weight can be changed over timescales faster than the integration dynamics

Programming pulses do not disturb existing current in integration loop



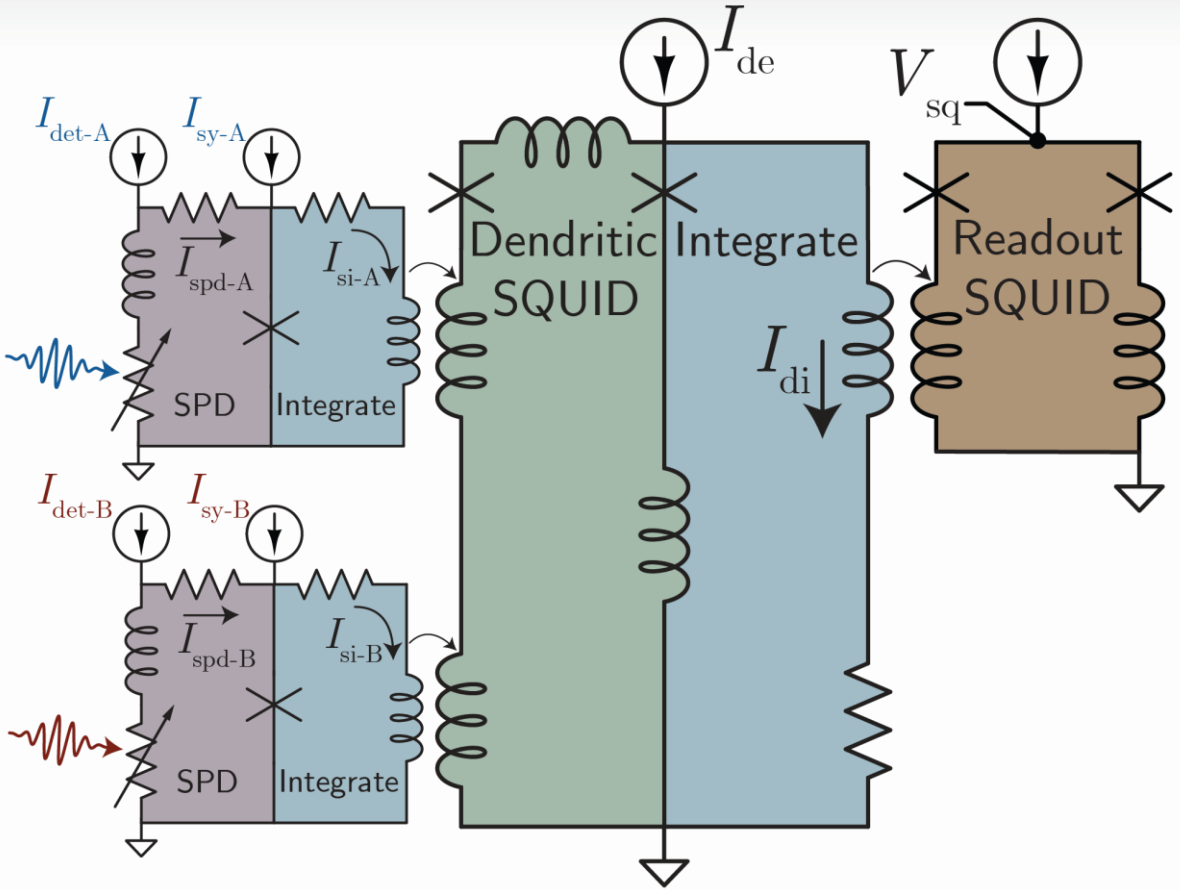
Part Three: Multi-Synaptic Dendritic Computation



Multi-Synaptic Circuits

First tests of multiple synaptic integration loops fanning into dendritic SQUIDs

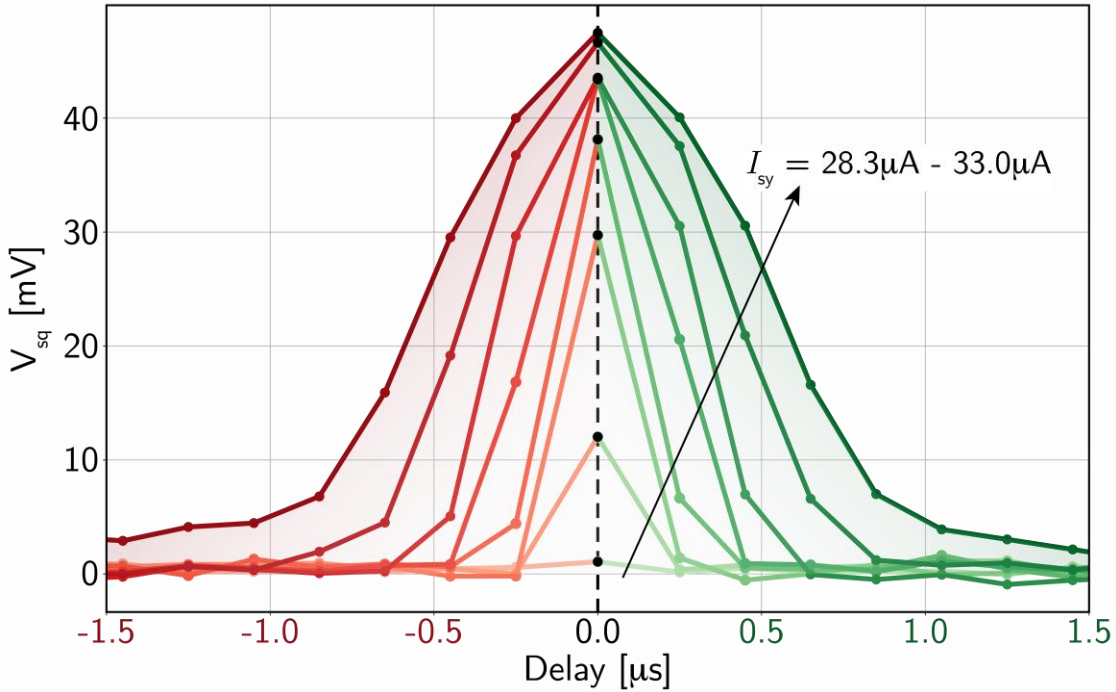
Synapses have independent weights and time constants

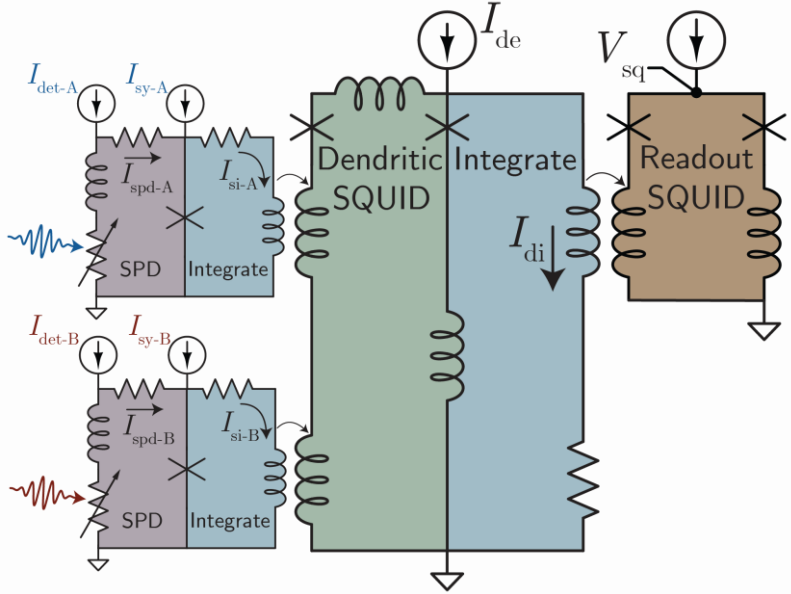


Coincidence Detection

Dendritic signal is a function of the **delay** between two synaptic events

Common computation within dendritic arbor of neurons

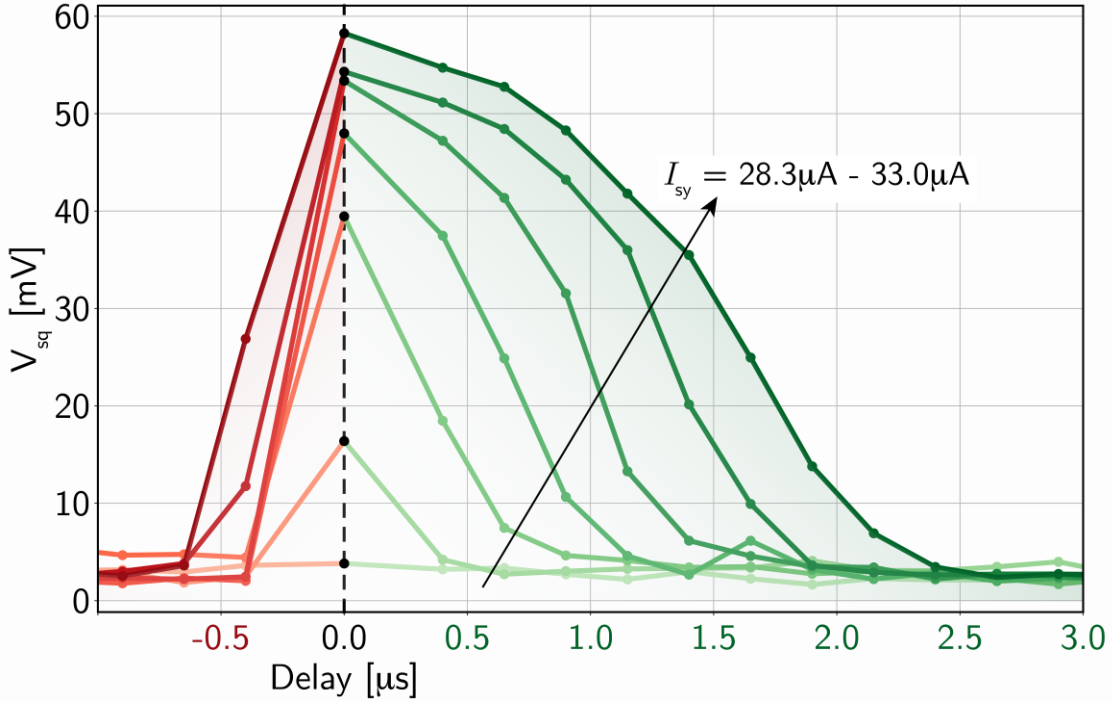


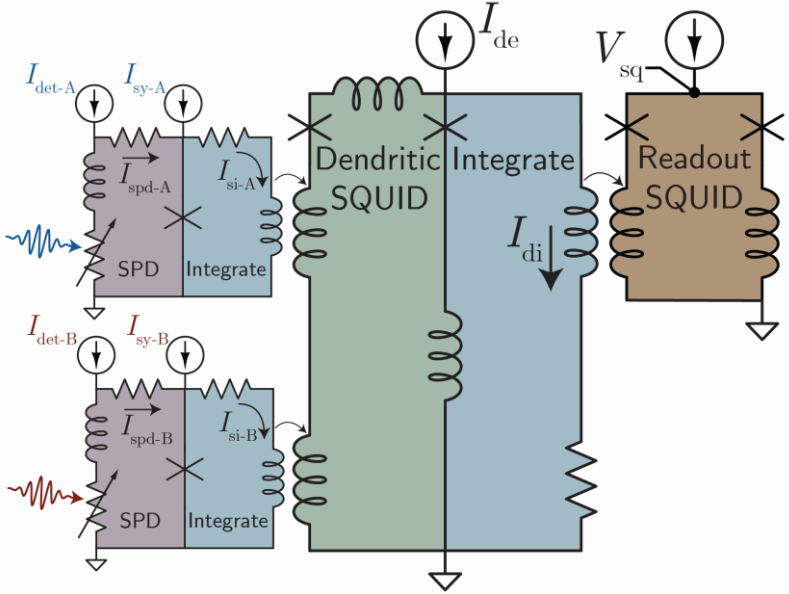


Sequence Detection

Dendritic signal is a function of the **order and delay** between two synaptic events

Important for implementing bio-inspired plasticity mechanisms

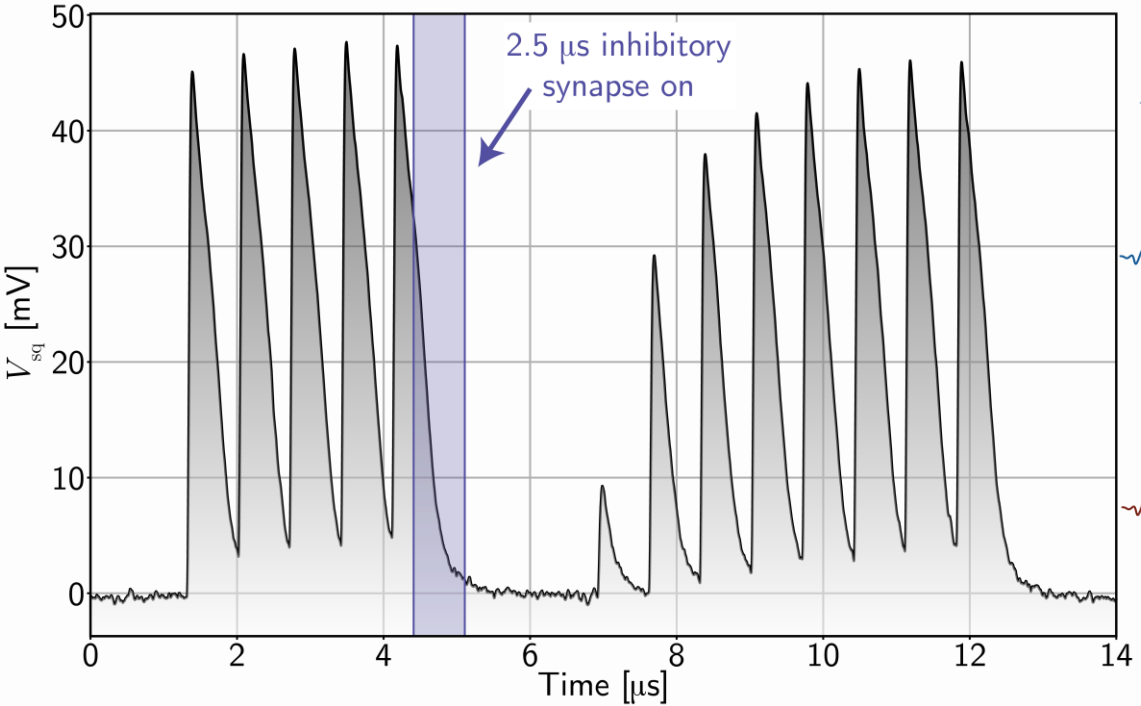


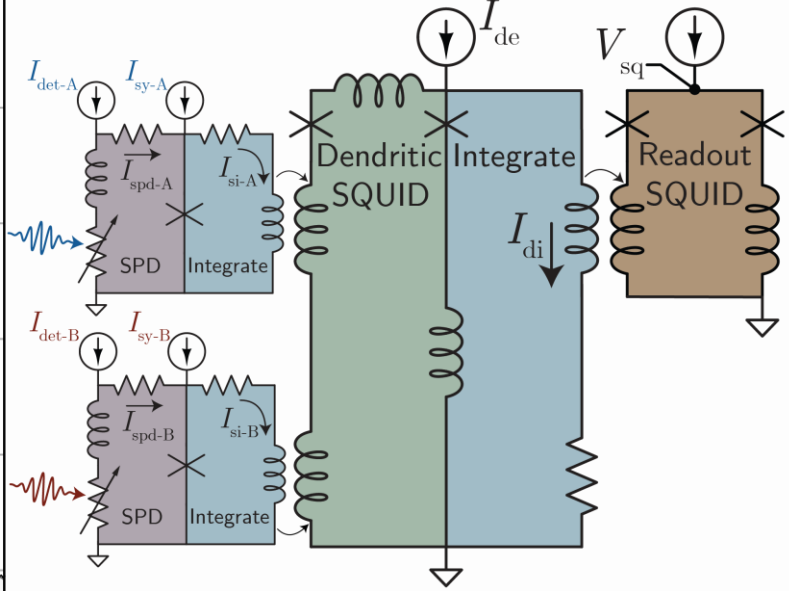


Inhibition

Using two synapses with opposite coupling into the dendrite gives inhibitory behavior

Similar schemes can be used for Short Term Plasticity (STP)





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