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Superconductivity at IBM – a Centennial Review: Part I – Superconducting Computer and Device Applications

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Abstract **- The hundred-year anniversary of the discovery of superconductivity coincided with the centennial of the founding of IBM. For more than half its history, IBM has had significant research and development activities in superconductivity. These included the two largest industrial programs aimed at developing superconducting digital computers. They also included a fundamental physical science program out of which came the discovery of high-temperature superconductivity. Significant fundamental and applied superconductivity research continues today within IBM, including work on superconducting qubits, which may portend a third major superconducting computer development program. This article reviews IBM's applied superconductivity work in the context of the evolution of the IBM Corporation. A companion article reviews the physics and materials science research activities.**

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I. INTRODUCTION – IBM's EARLY HISTORY AND THE BEGINNINGS OF THE IBM RESEARCH DIVISION

William J. Gallagher

The IBM Corporation traces its beginning to 1911 when the Computing-Tabulating-Recording Company (CTR) was assembled to sell a collection of products supporting businesses, including scales, time recording machines, and tabulating machines. Thomas Watson Senior was hired to run this company in 1914. Watson's strengths were in sales, which he had learned rising through the ranks at National Cash Register, and in envisioning new products and markets. He saw potential for products that did the work of clerks and bookkeepers, such as time recoding and tabulating machines, and particularly punched card machines. In 1924, reflecting his ambition and vision for the company, Watson had CTR's name changed to International Business Machines [1].

Watson himself had a personal interest in the education and scientific uses of tabulating machines, an interest not based on commercial potential. In 1929, after being approached by Columbia University, he had IBM machines placed in a newly formed Columbia University Statistical Bureau [2]. By 1931 a special tabulator was developed and placed into operation there. A young astronomy professor and frequent visitor to the Columbia Statistical Bureau, Wallace Eckert worked out a pluggable control system connection between two machines to implement numerical integration through a means of mechanical programming of problems, a step beyond just using the machines as calculators. By 1934, IBM machines began operating in this way under the auspices of the Columbia Astronomy Department. They were the only machines of this type and were in demand by users from many top astronomy departments at that time. To address this broader need, IBM by 1937 established what became known as the

Thomas J. Watson Astronomical Computing Bureau as a joint enterprise of the American Astronomical Society, the Department of Astronomy at Columbia University, and IBM. Among the visitors there was a Harvard graduate student, Howard Aiken, who convinced IBM to develop and build a machine called the Automatic Sequence Controlled Calculator (ASCC), which utilized electromechanical counters and could solve the differential equations involved in his thesis work. In a rather well known story, Watson felt IBM was snubbed in Harvard's 1944 announcement of the machine (there dubbed the Harvard Mark I). Columbia became the site where Watson developed further IBM computers for scientific purposes.

By this time, Watson Sr. realized IBM needed scientists to keep up with technological advances that could affect IBM machines. He invited Eckert to join IBM as the director of a new Department of Pure Science. Early in 1945, IBM founded the Watson Scientific Computing Laboratory at Columbia University, and Eckert joined IBM as its first director. (Eckert was IBM's first Ph.D. hire.) Among the lab's missions also were to assemble, develop, and provide "research and instructional resources…to be made available to scientists, universities, and research organizations around the world." Eckert was charged with developing the fundamental specification for a next IBM machine with capabilities to greatly exceed the ASCC. It was to employ vacuum tubes in the arithmetic unit, in the control circuitry, and in part of the storage, but use mechanical relays elsewhere [3].

In January of 1948 the IBM Selective Sequence Electronic Calculator (SSEC) was dedicated with about 250 times the performance of the ASCC. It had vacuum tube flip-flop circuits in arithmetic registers, backed by relay memory units fed by a continuous loop paper tape reader, and was in some sense the first stored program computer. As a spill over from these developments, which initially had scientific and educational motivation, military applications became important. Thomas Watson, Jr., who succeeded his father at CEO, foresaw that industry would be demanding such machines and even more advanced ones. In 1953, he announced the IBM 650 computer (initially with a magnetic drum memory but in 1955 a magnetic core memory add-on became available). It was the first mass-produced computer and over 2000 machines were produced over an eight year period. Meanwhile at the Watson Lab, IBM assembled a high-powered computer known as the Naval Ordnance Research Calculator (NORC). This machine was dedicated in January 1954 at the Watson lab and later delivered to the Naval Proving Ground at Dahlgren, VA in 1955. For 10 years, it was the most powerful computer in the world.

Bell Lab's announcement of the point-contact transistor spurred IBM to further broaden its basic research. In 1952, Eckert obtained approval from IBM and Columbia University to establish a solid state physics program. He had considerable freedom in recruiting and he in turn granted the staff he recruited considerable freedom in their research areas. By 1954 there were also 50 scientists working in IBM's Poughkeepsie Laboratory working in semiconductors, ferroelectrics, magnetism, and magnetic devices, and these were assembled into a new research organization there. In 1952 the San Jose Research Laboratory was opened. In 1955 a lab was set up in Zurich to undertake basic studies in fields such as magnetic thin films, fluid flow characteristics, and superconductivity. Stemming out of broad ranging discussions in 1955, in January of 1956 IBM organized a Research Division, reporting directly to corporate headquarters. It consisted of the Watson Lab at Columbia University, a portion of the Poughkeepsie Laboratory, the Zurich Laboratory, and the San Jose Laboratory [4].

Over this time period, the evolution of computer elements, and memory systems in particular, was anything but clear. Within IBM, there were at least seven avenues pursued for memory: magnetic tapes, magnetic drums, mercury delay lines, vacuum tube flip-flops for registers, Selectrons (tubes aimed at storing hundreds of bits), William tubes (CRT based storage), and magnetic cores. In the mid 1950's transistor reliability and repeatability were not at the

level that transistor memory development could be contemplated. Even in this milieu, there was an openness to other approaches that offered advantages.

II. THE CRYOTRON AND IBM's FIRST SUPERCONDUCTING COMPUTER PROJECT

William J. Gallagher

In this environment of an incipient Research Division with a fairly open mission, and of rapid growth of computation machinery with changing component technology, IBM researchers first learned about the cryotron. Dudley Buck of MIT presented his new device at a summer 1955 meeting of the American Institute of Electrical Engineers [5]. Buck described a basic device consisting of a niobium control wire wound around a one-inch long tantalum wire, with the magnetic field from the control wire modulating a superconducting to normal metal transition in the tantalum wire. He further showed how the device could be configured to show threshold current and power gain and how cryotrons could be combined to function as flip-flops, logic gates, and more complicated circuits. Buck's bulk cryotrons were slow, but he noted that miniaturized versions could be faster, although with significant gain trade offs.

Trip reports about Buck's presentation triggered immense interest at the Watson lab and elsewhere within IBM in conjunction with a low-temperature research program that had begun the year before. James Crowe at IBM's Kingston's Military Product Division devised a memory cell that utilized cryotrons to trap flux in holes placed in superconducting films [6]. He showed these could operate in 10 ns, about 100 times faster than the ferrite-core memories that were just starting to be used. Richard Garwin at the Watson Lab developed a model for thin film persistent supercurrent memory and predicted that a memory of $3x10^8$ bits could be built in one cubic foot with a cycle time of 10 ns [7]. In October of 1956, Garwin outlined to IBM a program aimed at demonstrating a large superconducting computer that could operate with the 10 ns cycle time [8]. The superconducting computer effort, which had already been growing, was placed under Garwin and involved approximately 100 staff by the end of 1956. It was located at various sites in New York including the Watson lab, the Poughkeepsie Research Lab, the Kingston Military Products Division and in temporary Research labs in upper Westchester County, near the site where IBM was to build its Research Division headquarters.

While Garwin proposed the focused program and organized its build up, he only directed it for a few months. In the first days of 1957, Garwin was approached by Columbia Professor Leon Lederman with news of preliminary results by Professor C. S. Wu of her experiment confirming parity violation in the decay of polarized Co^{60} nuclei. Garwin, who was already familiar with the parity violation ideas of Yang and Lee from attending seminars at Columbia, immediately joined forces with Lederman and his graduate student Marcel Weinrich at Columbia's Nevis Cyclotron Laboratories and in a matter of four days executed an experiment showing convincingly that parity was not conserved in meson decays [9]. To pursue this science further, Garwin asked to be relieved of his responsibility for running the superconducting computer program, and he was. This freedom for its scientists to switch back and forth from technology focused activity to fundamental science studies has remained a characteristic of IBM Research throughout its history. Garwin's switching was probably the earliest instance of this and undoubtedly the most extreme and abrupt example.

The rapid and sustained growth of the superconducting computer project was a result of the freedom enjoyed by researchers in the Research Division and of the availability of significant funding from IBM as well as from government sources. IBM had responsibility for the computers in the U. S. Air Force's Semi-Automatic Ground Environment (SAGE) program for

identifying and tracking aircraft. Beginning in 1956 in IBM's Kingston lab, superconducting technology was investigated along with thin film magnetic memory for potential enhancements to the SAGE system. By 1958, however, it became clear that a cryogenic computer could not be developed rapidly enough for the SAGE enhancement [10]. During this same time period, however, the U. S. National Security Agency (NSA) had a program, Project Lightning, aimed at advancing computing technology by three orders of magnitude, to nanosecond cycle times [11]. Project Lighting initially looked at three technological approaches, but when its Phase II program began in 1958, 85% of the funding was directed at cryogenic technology, the technology IBM was pursuing [10]. During this phase, joint work between IBM Kingston and IBM Research resulted in the successful integration of 135 cryotrons into a 40 bit memory chip [12]. Overall progress, however, was not as rapid as hoped. At IBM, Project Lightning ran through a phase III ending in 1961. IBM's final report under Project Lightning [13] noted that yields were erratic, and stated that the most important obstacle to progress was obtaining reliable insulating films. Film stress and source "spitting" were described as challenges for SiO films, the material used for insulating films at that time.

At this time IBM revamped its processing effort with a group led by Holly Caswell at the newly opened Thomas J. Watson Research Center in Yorktown Heights. After about 18 months, in the fall of 1962, that group reported good yields for circuits containing about 30 cryotrons [10]. However, at this time studies of individual in-line cryotrons (devices with control lines running parallel to the output line rather than crossed-film devices with perpendicular current flow) by Andrew Brennemann, James McNichol, and Donald Seraphim [14] also in Yorktown reported performance up to 100x slower than expected due to long time tails in building up to their normal-state resistance. This group showed that these long duration tails were due to latent heat effects and slow normal-metal superconducting phase boundary propagation between sparse nuclei. Due to this slow performance, the target of the Research program changed to low cost memory rather than high performance logic and memory.

Over this same period of time (1961-1963), there was an Air Force sponsored program led from Kingston aimed at a "Cryogenic Associative Processor." Designs were developed [15], but fabrication yield remained an issue and precluded the demonstration of design with 2300 cryotrons [16].

The cryotron project continued with its focus on memory until early 1965. Yield and reliability objectives were not achieved and by then cost and performance projections were no longer attractive compared to projections for magnetic cores and magnetic film memory. In the project's final report, Holly Caswell explained that the requirement for integrated thin film technology, which was initially thought to be an asset, actually turned out to be the downfall of cryotron technology. At that point in time, integrated fabrication technology was not mature enough to provide the degree of control required to yield functional integrated circuits [17]. At each critical program juncture, it was the maturity of the fabrication technology that held back the technology until there was no window of opportunity left.

Throughout the time of the cryotron program, there was a recognized tension among IBM management over how to run such a large exploratory endeavor, whether to run it as a loose collection of subprojects aimed at scientific frontiers and solving certain technical problems, or to have more focused top-down direction with targeted demonstrations. Garwin was critical of the "physicist's view" of his immediate successor directing the cryogenic computer program as working too much on interesting fundamental aspects [18]. This management style debate was never resolved and it remains hard to know if a different management approach might have led to technical success in IBM's cryotron program within the window of opportunity before semiconductor technology became dominant. It is also amusing to note that for the last year of the cryotron program, its manager, Holly Caswell, reported to Joe Logue. Logue had a career filled with leading and managing new IBM technology efforts to

success. He would later direct the IBM Josephson computer program in what turned out to be its final years, succeeding a management team of which he himself was quite critical [19].

III. THE JOSEPHSON TECHNOLOGY PROJECT AT IBM

Erik P. Harris and Mark B. Ketchen

A. Historical Overview

In this section some of the interesting technical and programmatic issues concerning IBM's efforts through the 1970s and early 1980s to develop a high performance computer technology based on superconducting Josephson junction technology are discussed. We begin with a brief historical overview of the development of Josephson logic and memory devices, starting with the discoveries of the tunnel effect between superconductors and of the Josephson effect and culminating in development of Josephson logic and memory devices and circuits at IBM in the late 1960s and 1970s. Following this introduction, we outline some of the basic properties of Josephson devices. Our emphasis will be on IBM latching logic devices and circuits. Josephson device operation has a simple mechanical analog in the rectilinear motion of a particle in a "washboard" potential, and this mechanical analog is used to explain latching versus non-latching behavior in Josephson devices and circuits. We examine several other important dynamic properties in the light of the above mechanical analog, including turn-on delay, the phenomenon of punchthrough, and the effect of thermal noise on the operation of Josephson devices. We next present a brief overview of IBM Josephson fabrication technology, beginning with the Pb-alloy technology developed in the 1970s and continuing with the Nb/Pb alloy edge junction technology practiced at IBM commencing in the early 1980s. We next briefly review some of the architectural issues for a Josephson computer along with some of the circuit development challenges. We then describe the Josephson Cross Sectional Model Experiment which was the most complex Josephson system demonstrated in the project. Finally, we discuss the last two years and the conclusion of the project.

In the waning years of the cryotron memory program at IBM, new developments were occurring that would create renewed interest in the possibility of high-speed, low-power superconducting logic and memory devices. In 1960, Ivar Giaever [20] demonstrated that electronic tunneling could occur in junctions between normal and superconducting electrodes that are separated by a thin insulating layer, and that the current voltage (*I-V)* characteristics of such tunnel junctions exhibit the superconducting energy gap that was predicted by Bardeen, Cooper, and Schrieffer in 1957 [21]. Giaever also studied tunneling between two superconductors and showed how the shape of the finite voltage current-voltage characteristic displayed even sharper features associated with the energy gap [22]. Soon thereafter, Brian Josephson [23] predicted that lossless supercurrents could flow in tunnel junctions in which both electrodes were superconducting, and that these supercurrents would be highly sensitive to applied magnetic fields because of quantum interference effects. Such tunnel junctions have come to be known as Josephson junctions, and the Josephson effects were first demonstrated experimentally by Anderson and Rowell at Bell Labs in 1963 [24]. The Josephson junction concept was soon broadened to devices in which two or more junctions are connected together with superconducting loops. These circuits demonstrate extreme sensitivity to magnetic flux in the loop because of quantum interference effects and are known as Superconducting Quantum Interference Devices, or SQUIDs [25].

Work on superconducting devices and circuits based on the Josephson effect was begun at IBM in 1964 by Juri Matisoo, who reported the successful demonstration of a device he called

the "tunneling cryotron" in 1966 [26]. It bore some resemblance to the earlier Buck cryotron in that a superconducting element was switched from a zero-voltage state to a resistive state by the application of a magnetic field. However, in this case the switching element was a Josephson junction, so that the switching was much faster. The voltage across the switching element in the resistive state could be the energy-gap voltage of a few millivolts rather than the microvolts achieved with the cryotron, and the sensitivity to magnetic field was much greater through the utilization of quantum interference rather than a superconducting-to-normal thermodynamic phase transition.

Switching elements utilizing the Josephson effect can exhibit latching or non-latching behavior. Non-latching devices that have been switched to the voltage state restore to the zero-voltage state when the supply current is reduced below the critical current level at which they were switched to the voltage state. Latching devices remain in the voltage state when the supply current is reduced to near zero – well below the level that was required to switch them to the voltage state in the first place. Devices with significant capacitance and low conductance, such as tunnel junctions in a typical circuit setting, demonstrate latching behavior.

It was clear that Josephson devices (both single junctions and multi-junction SQUIDS) would be interesting candidates for fast, low-power, latching logic circuitry. It was also evident that the SQUID concept could be the basis for memory circuits involving the storage of information as a persistent current that encloses one or a few flux quanta in a superconducting loop – a quantum interference analog to the older Crowe cell. Josephson logic and memory technology was seen as a possible enabler of future high-speed computer systems [27, 28], and IBM's effort in Josephson technology grew steadily in size and scope in the late 1960s and 1970s. Many outstanding young scientists and engineers were attracted to IBM's research labs in Yorktown Heights, New York and Zurich, Switzerland to participate in the effort. The program, with funding support from the U. S. federal government, grew to well over one hundred people during this period, and many significant accomplishments were achieved [29]. These included the development by James Greiner of a process for the reproducible fabrication of Pb-based tunnel junctions [30]; the development of Pb-alloy thin films for tunnel junctions and circuits that could withstand thermal cycling between room temperature and cryogenic temperatures [31]; the demonstration of sub-100 ps Josephson interferometer logic gates in 5 μm and 2.5 μm technology ground rules [32- 33]; the design and experimental verification of the circuit elements needed for a Josephson 4K-bit nondestructive-readout cache memory to be built in 2.5 μm technology [34]; and an AC power distribution scheme that resets the latching circuitry to the zero voltage state when the power reverses polarity at the end of each logic cycle [35]. A program goal was set to design and build a small prototype computer called the Josephson Signal Processor [36], or JSP, which would employ these technology elements and which was modeled on a previous IBM Research prototype computer known as the Research Signal Processor. While the JSP was never built, a Cross-Sectional Model (CSM) of this prototype computer was successfully demonstrated in the early 1980s [37] and will be discussed in more detail later. We now turn our attention to some of the basic properties of Josephson devices that are of importance in the operation of latching logic circuitry.

B. Basic Josephson Device Properties

Josephson latching logic circuits employ Josephson switching devices (either single junctions or SQUID devices) with current supplied from an AC power source and connected to subsequent logic stages by means of terminated transmission lines. The earliest Josephson logic devices were single junctions with smallest lateral dimensions of 25 μm or greater. Scaling to smaller dimensions was difficult for single-junction devices while preserving threshold cha-

racteristics that provide gain (i.e., output currents large enough to switch load devices) and sufficient operating margins (i.e., allowance for parameter variations across a chip or in a system and for noise) to permit use in integrated circuits. This led in the 1970s to the development of multi-junction interferometer logic devices [32, 33] in which the junctions could be as small as technology ground rules would allow, and most of the device area was taken up by the inductive loops in the interferometer. An example is the three-junction interferometer, the circuit diagram for which shown in Figure 1 (a), and the layout in Figure 2. It actually contains four small junctions, each with critical current I_o, but two of the junctions are very close together and act as a single junction with critical current $2I_o$. The threshold characteristic of the interferometer is shown in Figure 1 (b). Interferometers with that threshold characteristic provided enough current to switch subsequent logic stages and had operating margins that were seen as being sufficient for practical use in integrated Josephson circuitry. The critical currents for such an interferometer are set in relation to the impedance of an output transmission line connected to the interferometer that is terminated in a matched load. A circuit of this type is shown in Figure 1(c). For a superconducting line over a superconducting ground plane in 5 μm technology, typical transmission line impedance (Z) is about 6 Ω. The interferometer

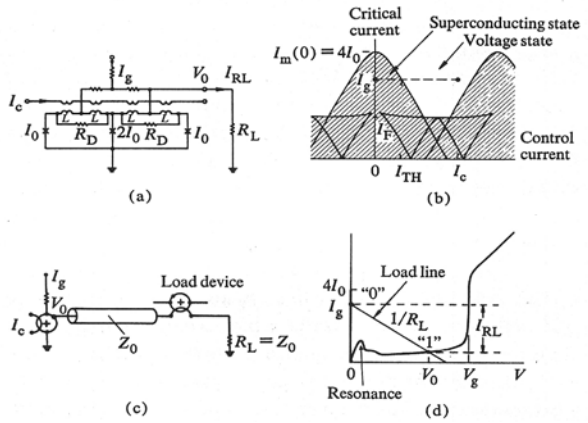

Fig. 1. (a) Circuit diagram for 3-junction split-feed interferometer. (b) Threshold characteristic of the 3-junction interferometer. (c) Circuit schematic of 3-junction interferometer as a switching device connected to matched superconducting transmission line and another switching device connected as a load device. (d) *I-V* curve of the interferometer switching device and load line. Resonances in the *I-V* curve are suppressed by damping resistors placed across the inductors as shown in (a) [38].

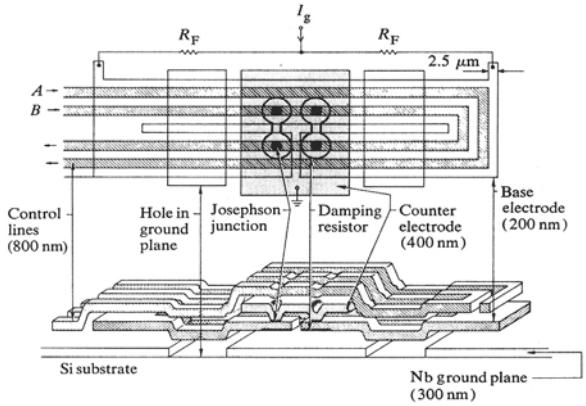

Fig. 2. Layout and vertical structure of 3-junction interferometer in 2.5 μm ground rules. The interferometer actually has four small junctions of critical current I_o, but two of them are very close together and act as a single junction with critical current $2I_o$ [38].

critical current ($4I_o$) will then need to be a little less than the energy gap voltage ($V_g \approx 3$ mV) divided by this impedance, or about 400 μA. A typical *I-V* curve for such a circuit is shown in Figure 1(d). The small junctions in the interferometer will have critical currents (I_o) of about 100 μA. Scaling to smaller dimensions increases Z and decreases I_o, so that in 2.5 μm technology $Z \approx 12\ \Omega$ and the small junction critical currents are about 50 μA.

Scaling interferometers to smaller ground rules with unchanged threshold characteristics requires maintenance of a constant value of (LI_o/Φ_o), where L is the loop inductance and Φ_o is the flux quantum = 2.07 mV-picoseconds. As ground rules are reduced and I_o decreases, L must increase and will require more minimum lithographic squares. The desire to get more inductance in a smaller space led in the late 1970s to the development at IBM of the "holey interferometer" [33] with holes in the ground plane to increase the inductance of the lines passing over them. The layout and vertical structure of such an interferometer in 2.5 μm ground rules are shown in Figure 2.

Many aspects of the dynamic behavior of Josephson devices can be understood in terms of a simple mechanical analog: the damped rectilinear motion of a particle in a "washboard" potential [39]. Consider the simple circuit of Figure 3 containing a Josephson point junction with critical current I_o driven by a current source I_g and connected to a resistive load R and shunt capacitance C. The current through the Josephson junction and voltage across it obey the familiar Josephson relations: $I = I_o \sin \varphi$, and $V = (\Phi_o/2\pi) d\varphi/dt$, where φ is the quantum phase change across the junction. The electrical behavior of the circuit is therefore described by the following equations:

$$C\, dV/dt = (I_g - I_o \sin \varphi) - (V/R)$$
$$V = (\Phi_o/2\pi)\, d\varphi/dt$$

The equations describing the damped rectilinear motion of a particle of mass m with momentum p in a medium with viscosity η, and subject to a potential U are as follows:

$$dp/dt = -(dU/d\varphi) - \eta\, p$$
$$p = m(d\varphi/dt)$$

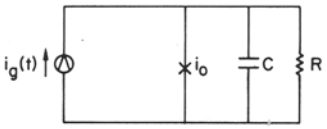

Fig. 3. Circuit diagram for Josephson point junction driven from current source and connected to resistive load and shunt capacitance.

The formal equivalence is established by setting $m = (\Phi_o/2\pi)^2 C$, $\eta = (RC)^{-1}$, $U(\varphi) = (\Phi_o/2\pi)(-I_g\varphi - I_o \cos \varphi) + U_o$, and particle velocity = $d\varphi/dt$. The "washboard" analogy arises from the $\cos \varphi$ term in the potential, and adding drive current increases the tip of the washboard through the $I_g\varphi$ term in the potential.

Let us now consider some properties of Josephson devices that can be described in terms of this mechanical analog:

Latching Versus Non-Latching Behavior: Suppose the source current is gradually increased from zero. This corresponds to increasing the tip on the washboard. The particle will remain in one of the corrugations until the tip exceeds a critical value that corresponds to the supply current exceeding the critical current I_o. The particle will begin to roll downhill gaining velocity, corresponding to voltage developing across the junction and current beginning to flow in the load resistor. If the tip on the washboard is then reduced the behavior will depend on the mass of the particle and the viscosity of the medium. If the particle has a very small mass and the medium is highly viscous, the particle will fall back into a corrugation when the tip is lowered just below the original critical value. This corresponds to non-latching behavior of Josephson devices with very small shunt capacitance and load resistance; such devices re-

vert to the zero-voltage state when the supply current is reduced below the critical value. If, however, the particle is massive and the medium has low viscosity, then the particle's kinetic energy will keep it rolling downhill even when the tip is less than was needed to start the particle rolling in the first place. This corresponds to the latching behavior seen for Josephson tunnel junction devices that have significant capacitance and are connected to large load resistances.

Turn-On Delay: If the supply current is set just below the critical current, and then increased so that it just slightly exceeds the critical value, there will be a delay time before the load current begins to grow with an *RC* rise time, and this delay time is known as the "turn-on delay" [40]. In the washboard analogy, when the tip exceeds the critical value there are no longer any stable minima for the particle but the particle will accelerate only very slowly until it rolls over the edge of the first corrugation, and this accounts for the existence of turn-on delay. The turn-on delay scales as $(C/I_o)^{1/2}$, is largest at small overdrives, and decreases with increasing overdrive [40]. It will scale as the square root of the linewidth as technology is miniaturized, while the *RC* output rise time will scale directly with linewidth. Hence turn-on delay is expected to become an increasing fraction of total gate delay as a result of miniaturization. The delay components of Josephson logic circuits are shown schematically in Figure 4. The turn-on delay t_o of logic gates in 2.5-μm technology is typically about 25-50% of the gate delay t_g, and is about 15-25 % of the total logic delay in a typical circuit environment, where the total logic delay includes the time-of-flight propagation delay and the crossing delay when the output signal crosses a load device.

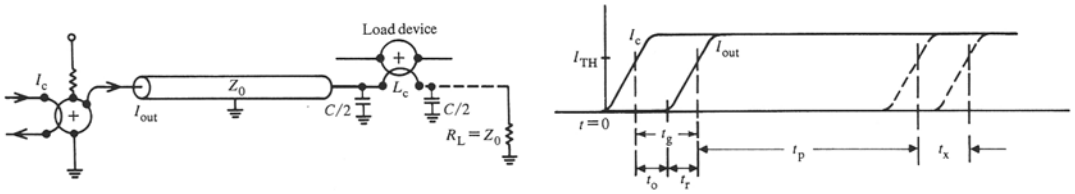

Fig. 4. Delay components of Josephson logic circuits, where t_o = turn-on delay, t_r = rise time, t_g = gate delay, t_p = propagation delay, and t_x = crossing delay. Note that the gate delay $t_g = t_o + t_r$, and the total logic delay $t_D = t_g + t_p + t_x$. The circuit at the left would represent a 2-input OR circuit if a second control line were added over the input gate [38].

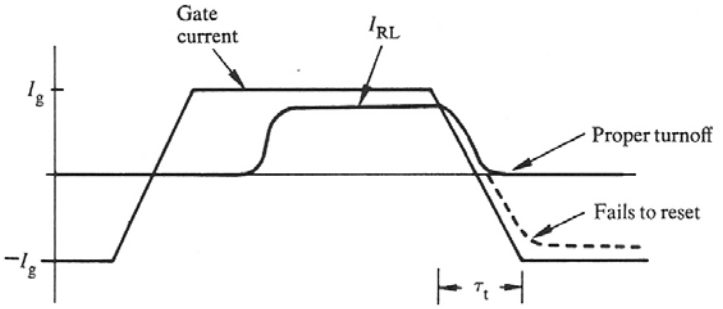

Fig. 5. An AC power supply is used to allow the output current I_{RL} of a Josephson logic circuit to reset at the end of each logic cycle. Failure to reset is called "punchthrough" [38].

Punchthrough: Recall that latching Josephson circuits are operated from an AC power supply to allow the latching circuitry to reset to the zero-voltage state when the power supply reverses polarity at the end of each logic cycle, as shown in Figure 5.

In 1971, Ted Fulton and Bob Dynes of Bell Labs found that if the supply current was swept too rapidly through zero, circuits would sometimes fail to reset [41]. Fulton and Dynes called this phenomenon "punchthrough," and predicted that there would be a critical rate of change of supply current above which punchthrough might occur, but below which it would

never occur. However, later work by Bob Jewett and Ted Van Duzer [42] at University of California at Berkeley and by Erik Harris and Wen Chang [43] at IBM showed instead that there should be an exponential punchthrough probability tail that extends below the supposed critical rate of change of supply current. Again, the washboard analogy can be helpful in understanding why this would be expected. Imagine that the critical amount of tip on the washboard is exceeded, so that the particle rolls downhill over the corrugations. If the tip is gradually reversed, one would expect that the particle would come to rest in one of the corrugations during the reversal. But because of the smooth sinusoidal shape of the corrugations, there is a small non-zero chance that the particle will come to rest in unstable equilibrium near the top of a corrugation during the reversal process. If this happens, and the particle "dwells" there for a sufficient amount of time before its motion changes direction, the tip may increase enough in the opposite direction to allow the particle to roll freely downhill in the opposite direction, and this is the mechanical analog of punchthrough. It is probabilistic because the chance that it will occur depends on randomly set initial conditions. The sinusoidal shape of the corrugations accounts for the exponential shape of the punchthrough probability tail. The existence of such a tail was demonstrated experimentally at IBM in 1982 [44].

The presence of this punchthrough tail has important engineering consequences. The rate of change of the AC supply current for a Josephson latching logic system during polarity reversal (and hence the duty factor of the logic, calculated by subtracting the power supply transition time τ_t from the cycle time and taking the ratio of the result to the total cycle time) must be kept low enough so that the occurrence of punchthrough will be tolerably infrequent. For latching logic fabricated in 2.5 μm Josephson technology, a 75% duty factor with a 2 nanosecond clock cycle time might be satisfactory for a large system, but a 75% duty factor with a 1 nanosecond clock cycle time would probably not be satisfactory.

Noise-Induced Switching: Thermal noise becomes increasingly important in Josephson circuitry as critical current levels are reduced, as unwanted thermally-activated switching can occur when junctions are biased below the critical current [45, 46, 47]. The probability that an unwanted switching event will occur increases as the bias current is raised to near the critical current. In the washboard analogy, thermal excitation can cause the particle to escape from a corrugation, which is a metastable state when the supply current is less than the critical current. In the case of light damping, once the particle has escaped it will continue to roll downhill and will not settle into a neighboring corrugation. The escape rate from the zero-voltage state increases exponentially as the bias current is increased toward the critical current [45]. A noise margin below the threshold current must be allowed to reduce the probability of unwanted switching to a tolerable level. For devices with critical currents of 200 μA in a system with several hundred thousand logic devices operating at 4.2 K, a noise margin of 15-20 μA would be warranted. As circuits are miniaturized and critical currents are reduced, the required noise margin becomes an increasing fraction of the critical current, and sets a practical lower limit on Josephson device critical currents of about 100 μA at 4.2 K.

C. Josephson Fabrication Technology

As mentioned earlier, a key achievement of the IBM Josephson program in the 1970s was the demonstration by Jim Greiner and colleagues of a reproducible process for fabricating Pb-alloy Josephson tunnel junction devices and circuits with well-controlled parameter spreads across a chip and wafer. The Josephson circuits that we have discussed thus far, including those used in the Cross-Sectional Model experiment, employed Pb-alloy tunnel junctions that were fabricated using this process [48]. However, devices and circuits fabricated with soft superconductors such as Pb alloys suffer from a limited ability to withstand thermal cycling from room temperature to cryogenic temperatures. Progress was made in the 1970s at IBM in

improving junction thermal cyclability through metallurgical improvements such as the use of Pb-In-Au alloys for the base electrode and interconnecting lines in integrated circuits along with Pb-Bi alloys for the junction counter-electrodes. But even with these improvements, it was recognized that thermal cycling would be a limiting factor for the reliability of digital systems containing large numbers of Pb-alloy junctions. It was known that Josephson devices and circuits made with hard superconductors such as Nb would be far better in withstanding thermal cycling than Pb-alloys, but the high dielectric constant of Nb oxide led to planar junction capacitances that were unacceptably large. To get around this limitation, techniques were developed at IBM and elsewhere to fabricate junctions on the edges of Nb films with small but controllable areas [49]. This allowed the development at IBM of reproducible processes for producing reliable Nb edge junctions with Pb-In-Au counter-electrodes for integrated circuits, with junction capacitances that were low enough to be suitable for fast digital circuitry.

In 1981, IBM began the bring-up of a Josephson development line at its facilities in East Fishkill, NY. The goal of this effort was to demonstrate that a Josephson integrated circuit process using Nb edge junctions with Pb-In-Au counter-electrodes could be practiced in a disciplined line environment with fabrication tolerances that would be consistent with circuit design requirements, and to assemble a large enough body of data to determine that adequate yield could be obtained in the fabrication of integrated circuit chips [50]. Line bring-up was completed in 1982, and in 1983 effort was focused on the fabrication of line qualification test vehicles with full vertical structures to assemble the needed data base. By mid-1983, most of the tolerance objectives of the line had been met. On-chip variations of junction critical currents were observed to be in the ±10-15% range for suitable populations of chips containing arrays of 1000 to 2000 interferometers [51]. There were still some issues to be dealt with. For example, on-chip systematic pattern-dependent variations in critical current were not well understood, and these variations had implications for high-density cache memory chip layouts. Overall, though, the bring-up and qualification of the development line with a Nb edge junction process was successfully completed by the middle of 1983. In subsequent years, after the end of the IBM Josephson program, a similar Nb edge junction process was used at IBM for SQUID studies and other scientific applications [52].

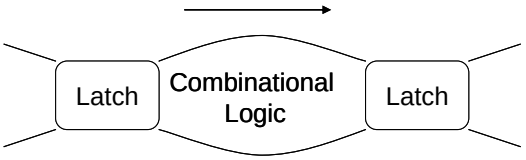

Fig. 6. Combinational logic situated between two latches.

D. Architecture and Test Chips

IBM's vision for the architecture of a Josephson computer was that of a standard Von Neumann finite state machine, very much patterned after IBM's silicon bipolar mainframes of that day – just much faster and more compact [28, 36, 53]. Figure 6 shows a block of combinational logic between two data latches. At the beginning of a cycle information that was stored in the first latch is gated out into the logic block. During the active portion of the cycle logic operations are performed and the output is captured by the next latch before the end of the cycle. In the case of the Josephson computer the logic was "latching logic", typically AND and OR (see Figure 1) gates with no inverters. At the end of a machine cycle, all of the logic gates had to be reset in preparation for the beginning of the next cycle. This was accomplished by powering the logic with a roughly trapezoidal bipolar waveform as shown in Figure 5. The power supply waveform which also served as the system clock was locally gener-

ated by clipping a sinusoid with a stack of large area Josephson junctions. Logic gates that had switched from the zero-voltage state to the finite voltage state during the active part of the logic cycle reset to the zero-voltage state as the power supply transitioned through zero. Meanwhile the latches capture and store the data from the logic in the form of persistent circulating currents as the polarity of the power supply reversed. The CPU consisted of a large collection of latches and logic blocks configured in such a manner that elements of a stored program could be executed. It was of course periodically necessary to obtain data and instructions from memory in order to actually run a calculation. The logic, memory, and power supply all work together synchronously to perform as a computer.

At IBM in the late 1970s, following initial work at 5 μm [32], a number of test chips were fabricated in 2.5 μm minimum feature size technology to demonstrate various circuit concepts in memory [34] and logic [33], along with other experiments investigating packaging and power distribution [35, 54, 55]. The four-junction interferometer shown in Figure 2 comprises an OR gate, representative of Josephson latching logic gates. In experiments involving chains of such devices delays as small as 13 ps/stage were demonstrated. Such delays were unprecedented at that time and are in fact comparable with those of modern silicon CMOS technology at the 90 nm technology node. SRAM consisted of an addressable array of cells, each consisting of several Josephson junctions and a superconducting loop configured such that a logical "1" or "0" was represented as the presence or absence of a circulating current, the magnitude of which corresponded to a single enclosed flux quantum, Φ_o. Addressing and readout circuitry consisted of an intricate assembly of Josephson logic circuits and transmission lines. A 4-kbit chip with a 1 ns access time was the design target for the program in the late 1970s and early 1980s. The design of such a chip involving many different device types and stringent relative timing constraints proved to be an extremely difficult technical challenge. The trapezoidal ±12 mV power supply waveform was locally derived from a sinusoidal waveform applied to four-high stacks of large area Josephson junctions with critical currents suppressed by a magnetic field generated by dc current flowing through a nearby control line. To minimize the total ac current that had to be delivered to the cryogenic environment to power a large number of Josephson devices, a very efficient planar superconducting transformer distribution system was devised [35].

E. The CSM Experiment

As a logical step along the way towards building an envisioned Josephson computer, the JSP, it was decided to demonstrate a small prototype system that would explore on many fronts the problems and solutions that Josephson technology has to offer [37, 56]. This system included not only circuitry on chips but also a full three-dimensional multi-chip card-on-board package, power distribution system, and associated I/O. The cross sectional model (CSM) experiment featured a critical system path through the proposed prototype machine including a jump control sequence and cache access in each machine cycle [36]. This path, situated on three different chips and intervening package segments, contained approximately 10 levels of logic, a simulated cache access and various drivers and receivers associated with chip-to-chip communication. Figure 7(a) shows the schematic of the critical path of the proposed Josephson machine on which the design of the CSM experiment was based, while Figure 7(b) shows an exploded view of the CSM assembly. The chips and package parts were fabricated on silicon substrates in Pb-alloy technology with 2.5 μm and 5 μm minimum feature sizes respectively. Solder and pluggable connectors were used to attach these parts together and to provide electrical connections between parts [57]. The signal path involved three chips and four chip-to-chip crossings, two of which included card-to-card crossings. At the time of the CSM experiment the cache design and demonstration was running late and it was decided to simulate the

cache access with a 1 ns long transmission line. Each card housed two 6.35 mm x 6.35 mm chips that were connected to the card with 228 solder ball connectors. Feet on either side of each card were connected with right angle solder fillets and arrays of micro-pins were located on the underside of the feet as well as on the adaptor and on a wiring module that was plugged into the adaptor from its underside. A board with an array of Hg filled microsockets positioned on top of the adaptor engaged the pins on the adaptor and wiring module underneath and the card pins on top, enabling electrical connections among the various package parts. A wiring schematic for the CSM package is shown in Figure 8(a). The I/O cable divided into two 40-line sections connected to opposing sides of the adaptor onto which the other package parts were assembled. The flexible I/O cable had a Cu ground plane with 50 Ω Cu striplines and Kapton insulation [58]. A photograph of the assembled CSM experiment is shown in Figure 8(b). This entire assembly was cooled in a liquid Helium bath at 4.2K within a carefully engineered cryoinsert [59] and dewar system at an ambient magnetic field of a few microgauss.

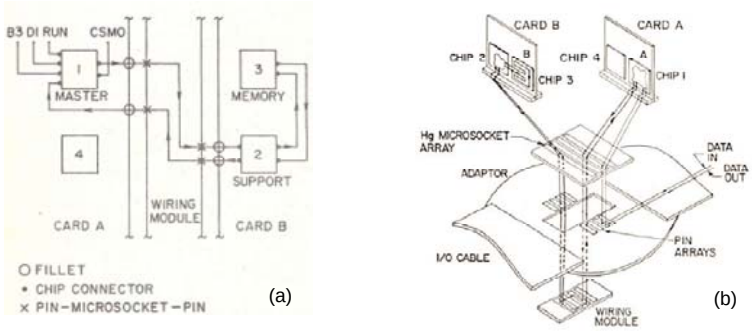

Fig. 7. (a) High level CSM schematic, and (b) exploded view of the CSM experiment [60].

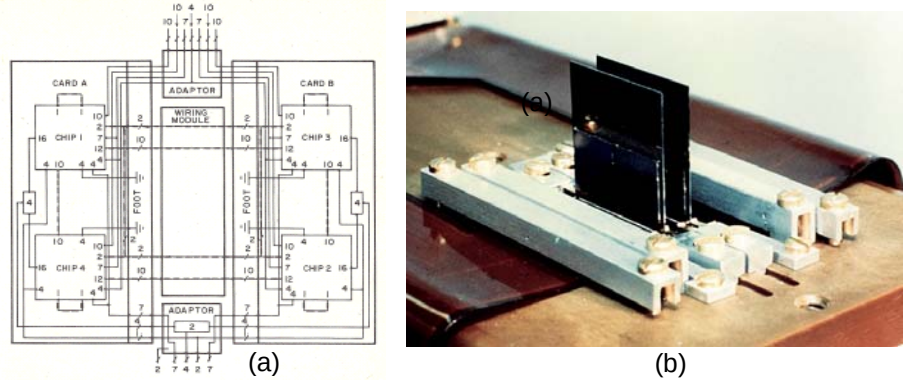

Fig. 8. (a) CSM package wiring schematic, and (b) photograph of CSM assembly [60].

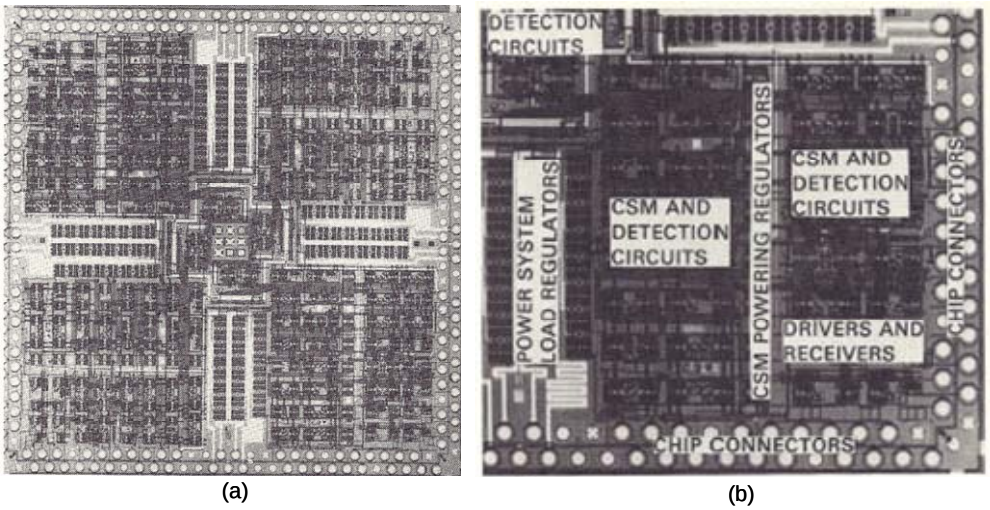

Fig. 9. (a) Four-fold redundant CSM chip, and (b) expanded view of chip quadrant [60].

A single CSM chip was designed such that each of its quadrants contained all the circuitry necessary to perform the functions of the master, memory support, and memory chips of the final assembly. A photograph of the 4-way redundant CSM chip is shown in Figure 9(a) along with an expanded view of the CSM chip quadrant in Figure 9(b). In addition to the logic circuitry and transmission lines necessary to implement the critical path functions, the CSM chip was instrumented with on-board detection circuits including a Josephson sampling oscilloscope that enabled precise waveform and timing measurements of signals as well as power supply waveforms [61, 62, 63]. This was a four trace sampling oscilloscope with a common time base, each trace having inputs from different strategic power supply and signal locations. This capability, with a few ps time resolution, proved to be invaluable in characterizing the high speed electrical performance of the system. Chips were first tested individually at 4.2 K with a special chip test adaptor and intervening spring loaded connectors to identify "good" path sections. Package pieces were individually probed at room temperature to verify continuity and check for shorts. Pinned feet were soldered onto cards and then chips were attached to cards in the proper orientation (as determined by test results) with a lower melting point solder. The entire system was then assembled and cooled to 4.2 K in a very specific manner to minimize the likelihood of trapped magnetic flux. Many iterations were required over an extended period of time, but in the end a fully functional path was found and then thoroughly analyzed. Figure 10(a) shows representative data waveforms with the system run-

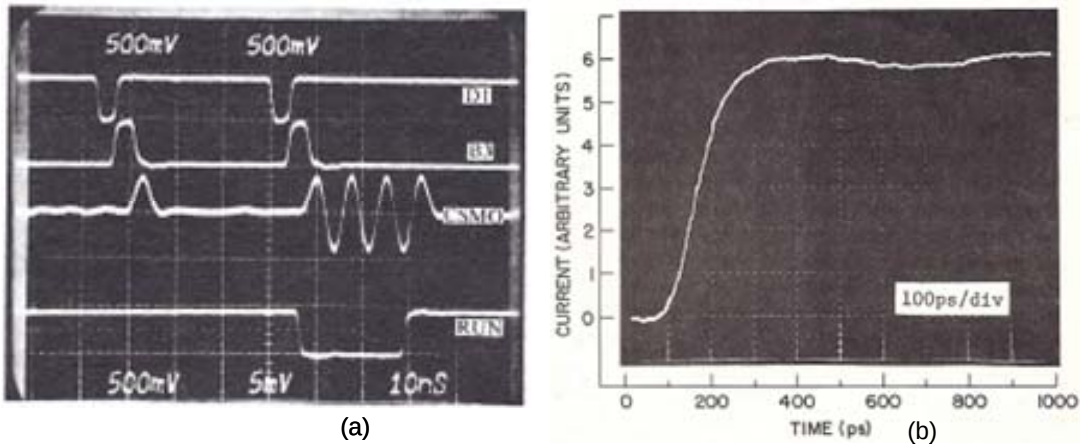

Fig. 10. (a) Representative data patterns showing correct operation of the CSM path with a 3.7 ns cycle time [60]. (b) Driver output waveform measured with the on-chip sampler [64].

ning at a 3.7 ns cycle time and Figure 10(b) shows an output waveform from an off-chip driver as measured with the on-chip sampling scope.

Successful execution of the CSM experiment was a major achievement for the IBM Josephson program. The minimum cycle time of 3.7 ns was close to the 300 MHz target and verified that, with the exception of memory, the essential components for a Josephson signal processor could in fact be designed and demonstrated. It is fair to say that against the backdrop of the technical and commercial successes of silicon technology, the credibility of the entire program rested on the success of the CSM experiment and failure would likely have ended the program immediately thereafter. With success came intense focus on what were viewed as the two main obstacles to scaling up: designing a robust sub-ns access 4K-bit cache memory chip and establishing a fabrication line capable of yielding significant numbers of chips with adequate control of parameters, especially junction critical currents and resistor values. The final two years of the program were centered on overcoming these obstacles.

F. The Final Two Years and Conclusion of IBM's Josephson Program

During those two final years a fabrication capability that met the specified criteria was established at the IBM East Fishkill site, as previously described. While critics had long argued that a technology relying on tunneling through a thin barrier could never be controlled to the precision necessary to build computer chips, IBM's experience in East Fishkill clearly showed otherwise. Memory chip design, on the other hand, proved to be a very different story. Despite extensive efforts in both Yorktown and Zurich a robust cache design proved to be elusive and was never accomplished in the program.

On September 23, 1983 came the decision by IBM to end the Josephson computer program [51,65]. At the top of the list of issues that entered into this decision was the unprecedented financially self-sustaining advance of silicon technology. By 1983 it appeared that even if the memory problem could be solved, the performance advantage of Josephson technology over silicon bipolar for high performance computing would only be a factor of three or so at introduction, and would likely diminish further over time. Behind this of course were some nagging technical problems. On the logic side, the basic latching logic approach seemed fundamentally limited in cycle time by punchthrough phenomena as discussed earlier. It was difficult to see how a practical cycle time of under 1 ns or so would ever be possible. In the intervening years non-latching single flux quantum logic that gets around this problem has been explored and demonstrated [66]. Thermal noise was another major issue which seemed to set a practical limit on device critical current to about 100 μA at 4.2 K. This imposed a "constant current" scaling feature that leads to ever increasing power dissipation with scaling. Interestingly this is exactly the same behavior that led to the demise of silicon bipolar technology as a high performance computer technology a decade or so later [67, 68]. High performance Josephson cache memory remains a problem to this day. The memory problem is both one of extremely tight design margins for known approaches and also the fixed "size" of the flux quantum Φ_o that severely limits scalability.

Work on Josephson technology continued for a number of years at several laboratories in Japan after the end of IBM's program. Noteworthy accomplishments include a 1.1 GHz clock 4-bit microprocessor first demonstrated in 1988 by Fujitsu [69], a 1kbit memory chip first demonstrated in 1987 by NEC [70] and a 4K-bit memory first demonstrated in 1988 by Fujitsu [71]. On the performance side it is worth pointing out, however, that by this time a sub-ns 5K-bit cache chip was demonstrated at room temperature with silicon bipolar technology at IBM [72]. Finally we will emphasize once more that fabrication technology, while an enormous challenge, was not in the end viewed as a limiting factor. Over the years the edge junc-

tion technology championed by IBM has given way to Nb-AlO_x-Nb trilayer based technology facilitated by dry etching and chemical mechanical polish (CMP) planarization [73], as discussed in the following section on analog SQUIDs. Using similar approaches magnetic RAM technology which uses similarly thin-barrier tunnel junctions has successfully yielded 16 megabit memory chips [74] for use at room temperature, unambiguously verifying the viability of tunnel junctions for VLSI technology.

IV. SUPERCONDUCTING QUANTUM INTERFERENCE DEVICES AT IBM

Mark B. Ketchen and William J. Gallagher

A. Low-T_c SQUIDs

A Superconducting Quantum Interference Device, or SQUID, consists of a superconducting loop of inductance L interrupted by one or more Josephson junctions [23, 25]. SQUIDs were essential devices in IBM's effort to build a Josephson digital computer but are also used as analog detectors of very small changes in magnetic flux. A "dc SQUID" has two identical series connected Josephson junctions each of critical current I_0 and resistively shunted to render the current-voltage (*I-V)* characteristics non-hysteretic [75, 76]. With a dc bias current $>2I_0$ the voltage across the SQUID is a smooth periodic function of the magnetic flux threading the loop with a periodicity of Φ_0, where Φ_0 is the flux quantum, 2 x 10^{-7} G-cm^2. Sensitivities of order 10^{-6} $\Phi_0/\sqrt{\text{Hz}}$ or better have made such devices useful in a wide variety of applications ranging from highly sensitive magnetic measurements in the laboratory to clinical biomagnetic measurements to underwater magnetic anomaly detection.

Single junction rf biased low-T_c SQUIDs for use in magnetic detection systems [77] were among the first superconducting devices to be commercialized. John Clarke as a graduate student at Cambridge [78] and then as a professor at the University of California at Berkeley championed the advantages of the non-hysteretic dc SQUID for similar applications. In the mid 1970s he and his group at Berkeley demonstrated superior performance of a dc SQUID design having a thin film cylindrical inductive loop along with shunted Josephson junctions patterned on a 3 mm diameter quartz cylinder using shadow masks fabricated in a machine shop with 50 to100 μm minimum dimensions [79].

Work on low-T_c dc SQUIDs at IBM began during a month-long visit by John Clarke to Yorktown late in the summer of 1977. Two of Clarke's former students, Richard Voss and Mark Ketchen were already at IBM, soon to be followed by Claudia Tesche and Roger Koch. All of these former Clarke students together with a number of other IBMers subsequently made many contributions to the field of dc SQUIDs in both low-T_c and high-T_c technologies. The initial work at IBM focused on leveraging existing IBM technology such as digital Josephson fabrication capability and advanced electron beam lithography to demonstrate improved performance, eventually approaching quantum noise limited operation [80, 81, 82]. Subsequently important new device features and new innovative designs were explored and a number of different applications were perused ranging from detectors for challenging solid state physics experiments [83] to magnetic field gradiometers for magnetic anomaly detection [84] to magnetic monopole detectors [85] to sensors for scanning SQUID microscopes [86]. Three of the IBM advances in dc SQUID design and fabrication growing out of these efforts in the low-T_c arena that have had an enduring impact will be briefly described.

Washer SQUID with Spiral Input Coil: The first of these is a planar dc SQUID design that incorporates a tightly coupled input coil. Early practical SQUIDs, both rf and dc, were very three-dimensional in nature, typically cylindrical or toroidal. Such structures could be well

coupled to with a wire wound input coil which would then match well to a larger input coil structure to give enhanced sensitivity to, for example, magnetic fields or magnetic field gradients. Design considerations limit the SQUID inductance L for most designs to a few pH to a nH, which in turn limits the SQUID pickup loop area to a few mm^2 at most. By using a flux transformer consisting of an input coil of inductance L_i connected to a pickup loop structure of similar inductance, the magnetic field sensitivity scales as $\sqrt{\Phi_n^2/2k^2L}$ [87, 88], where k is the coupling constant between the L and L_i and $\Phi_n^2/2L$ is the SQUID's intrinsic energy sensitivity, having a lower limit in the vicinity of Plank's constant h. It was originally believed that to get good coupling would require an inherently three dimensional SQUID inductance, but this was discovered not to be the case by MIT co-op student Jeff Jaycox working with Mark Ketchen. Using thin film transformers from the Josephson program as a starting point [35] along with 2D and 3D inductance calculation programs that had been pioneered by IBM's Wen Chang [89] they came up with the now pervasive washer with spiral input coil configuration [90,91] that has been for over 30 years the basis of all high performance coupled SQUID designs. The basic idea is shown in Figure 11. The SQUID inductance L consists of a square washer with a ground-planed slit connecting to the two series Josephson junctions at an outside edge as indicated. Simulations indicated that the inductance of such a structure is dominated by the hole with a value of 1.25 $\mu_0 d$ for a square hole of width d independent of the

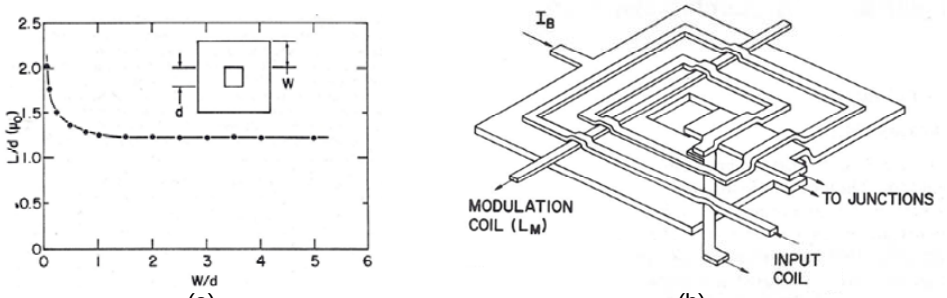

Fig. 11. (a) Simulated inductance of a square superconducting washer [92], and (b) design of a square-washer SQUID with a spiral input coil [93].

washer width w, once $w>d$. The input coil then takes the form of a thin film spiral wound on top of the washer. Such an n-turn spiral input coil has a self inductance of about n^2L and a m washer width w, once $w>d$. The input coil then takes the form of a thin film spiral wound on top of the washer. Such an n-turn spiral input coil has a self inductance of about n^2L and a mutual inductance to L of about nL, with k^2 not far from unity. The leakage inductance which is the strip-line inductance of the spiral with respect to the washer is typically small compared to n^2L. The outside edge of the washer and the value of n can be adjusted to match L_i to some arbitrary pickup loop structure while the SQUID inductance and other optimized parameters remain constant.

Planarized All-Refractory Technology for Superconductors: As second high impact advance was in the area of fabrication of SQUIDs and other Josephson devices. Following the end of IBM's Josephson computer program in 1983, Bill Gallagher and his Exploratory Cryogenics Technology Group maintained a Nb/Pb alloy Josephson edge junction fabrication process for building SQUIDs and other scientific devices [52]. Meanwhile advances outside IBM had been made in fabricating tunnel junction with both electrodes being Nb. IBM had investigated all Nb tunnel junctions earlier, but had difficulties with relatively large subgap currents [94, 95] and high specific capacitances [94]. Kroger, Smith, and Jillie and colleagues at Sperry had shown that a deposited amorphous SiH barrier could give a lower specific capacitance [96] and had introduced the concept of first fabricating a huge Josephson junction, the size of an entire wafer, and then removing most of it to leave only isolated small

junctions where they can be incorporated into SQUIDs or other devices [97]. Gurvitch and colleagues at Bell labs had shown how a thin aluminum layer could be deposited and mostly oxidized to make a low specific capacitance and excellent low sub-gap leakage Josephson junctions with both electrodes being (mostly) Nb [98]. These also could be first made as a large junction and then patterned into isolated structures [99]. Figure 12(a) depicts such an isolated structure. A key problem with this approach is how to make electrical contact to the top of the junction pedestal. A contact hole through the inter-level dielectric would have to lie entirely on the pedestal which has serious implications on how far the junction dimensions can be scaled. It was long recognized that what is needed is some kind of self-aligned contact. An elegant solution to this problem emerged in the development of the Planarized All- Refractory Technology for Superconductors (PARTS) process at IBM in the late 1980s [73], a process that was developed and practiced in the Yorktown Silicon Technology line. At the heart of this was the use of chemical-mechanical polish (CMP) planarization techniques to solve the self-aligned contact problem as indicated in Figures 12 (b and c). In the late 1980s CMP was just being introduced into silicon technology and has since become the industry standard for planarization in multi-level interconnect fabrication. PARTS was developed at IBM as an activity under the DARPA funded Consortium for Superconducting Electronics (CSE), in which MIT, MIL LL, and AT&T Bell Labs were among IBM's partners [100]. The

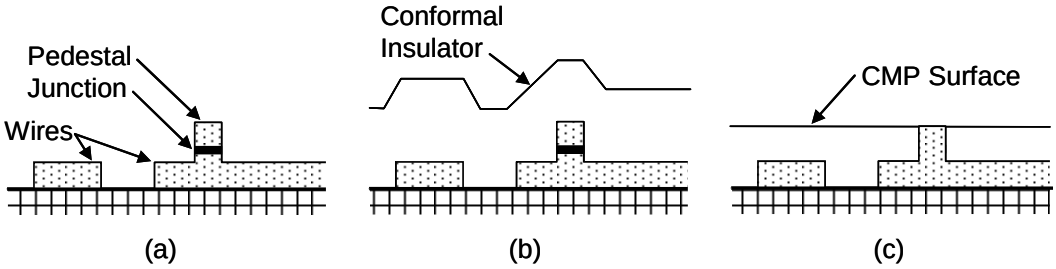

Fig. 12. (a) Trilayer etched to delineate wires and small junctions, (b) same structures buried in a conformal insulator, and (c) after CMP planarization.

all important Nb-AlO_x-Nb trilayers provided by MIT's Lincoln Laboratory were fabricated by Manjul Bhushan, a leading researcher in superconducting device fabrication at the time. Mark Ketchen worked with C.-K. Hu and Dale Pearson at IBM to develop the necessary etching, and CMP planarization processes as extensions of on-going work for silicon technology applications. It was of course not at all obvious that the delicate tunnel barrier would survive the mechanical stress associated with the vigorous CMP activity in close proximity, but such is the case and excellent quality Josephson junctions were produced. An additional challenge was to make the higher super current density junctions that would be needed to get better performance from scaled devices. Alan Kleinsassser took up this challenge under the auspices of the CSE, first working with Manjul Bhushan at Lincoln Lab to get 7.5 kA/cm^2 [101], and later with Ron Miller and Hank Mallison at AT&T Bell Labs to get up to 400 kA/cm^2 [102] with Nb/Al/AlO_x/Nb Josephson junctions, along the way understanding some of the physics controlling subgap current (multiple Andreev reflections [103]) and systematically cataloging some of the processing universality (critical current density as a function of oxygen exposure [104]) Junctions down to 0.1 μm diameter were subsequently demonstrated by Bhushan, after she had relocated to SUNY Stony Brook [105]. A full e-beam lithography variant of the PARTS process was later used there to make 750 GHz RSFQ circuits [106]. Variants of PARTS are still being used today at IBM and elsewhere for superconducting circuits and a similar approach is currently in use by IBM and partners for magnetic tunnel junction fabrication for MRAM [74].

Miniature SQUID Susceptometers and Magnetometers: A final advance, from the area of micromagnetometry, began with the device depicted in Figure 13(a). With this device a small sample to be investigated is placed in one of the pickup loops and a magnetic field applied with the field coil. The two SQUID pickup coils are counter-wound such that the net flux coupled to the SQUID should be zero in the absence of a sample. A small imbalance can be compensated for with the field coil center tap. In the original experiment [107] a 5 μm tin particle was placed in one of the pickup loops at room temperature by moving one of a number of such particles sprinkled on the surface of the chip into position using a micromanipulator. The chip was then carefully cooled to liquid helium temperature (4.2 K) in the horizontal orientation and a magnetic field of a few Gauss applied with the field coil. The helium bath was next pumped on, lowering the temperature through the superconducting transition of tin at about 3.7 K. The resultant flux change measured by the SQUID, which was six orders of magnitude above the noise floor, corresponded to the magnetic dipole moment induced in the tin particle through exclusion of the applied magnetic flux at the superconducting transition.

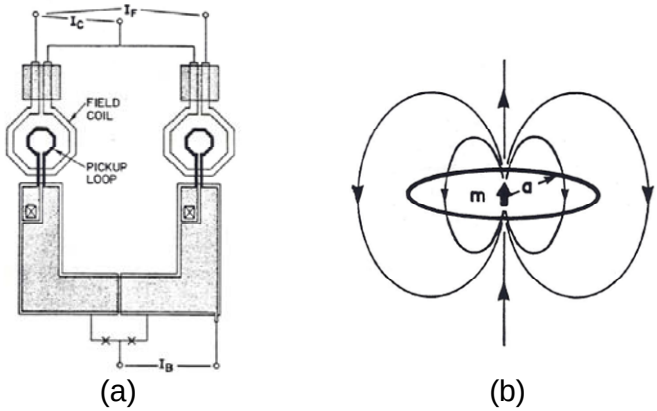

Fig. 13. (a) SQUID microsusceptometer with two series connected pickup loops [108], and (b) magnetic moment m coupling to a pickup loop of radius a.

This was the expected result and by itself not earthshaking. However, it ushered in a plethora of new devices and experiments with a number of high profile results at IBM and elsewhere. It soon became apparent that putting small particles into pickup loops, or microfabricating thin film samples in such loops was slow and painstaking. Far better to have a scanable device with a pickup loop that could be used to explore independently prepared surfaces – a scanning SQUID microscope. The precursor of such an instrument using a small wirewound pickup loop connected to a commercial rf SQUID had been developed by Stuart Bermon at IBM and another MIT co-op student, Pat Rogers, to investigate magnetic flux trapped in a ground plane [109] as part of the Josephson computer program. Thin film derivatives of the original miniature susceptometer design, configured as magnetometers, were fabricated with the PARTS process both at IBM and later by Manjul Bhushan, then at SUNY Stony Brook, and subsequently used by John Kirtley and collaborators to implement a sophisticated scanning SQUID microscope [86]. This microscope was used by Chang Tsuei, John Kirtley, and team to observe half integral flux quantization in specially prepared high-T_c rings, revealing the *d*-wave symmetry of superconductivity in YBCO [110].

Figure 13(b) shows a magnetic moment coupling to a small pickup loop or radius a. It can be shown that the spin sensitivity in Bohr magnetons per √Hz of a SQUID microscope incorporating such a loop is just $a\Phi_n/r_e$, where r_e is the classical electron radius and Φ_n is in units of $\Phi_0/\sqrt{\text{Hz}}$ [111]. For a sub-μm loop with a SQUID operating near the quantum limit ($\Phi_n^2/2L$ near h) it should be possible to resolve individual spins. While such resolution is yet to be demonstrated, experiments attempting to accomplish this feat are in progress today [112].

B. High-T_c SQUID magnetometer and gradiometer development

In contrast to IBM's early application assessment that high-T_c superconductivity would not favorably impact Josephson computing technology, IBM immediately recognized that nitrogen temperature SQUID-based instrumentation could be quite useful. In the euphoric period immediately following the high-T_c discovery, IBM researchers set about to demonstrate liquid nitrogen temperature dc SQUID operation, soon to be joined by research colleagues around the world. This was followed by a more serious multi-year high-T_c SQUID technology demonstration effort in Yorktown, done with partial support from the Office of Naval Research and in collaboration with IBM's Federal System's Division. The aim was to demonstrate a liquid nitrogen temperature SQUID system for magnetic anomaly detection for the U.S. Naval Coastal Systems Center in Panama City, Florida. In this section we review both IBM's development of high-temperature SQUIDs and its development of gradiometers for magnetic anomaly detection.

Compared to low-T_c pure metal and metallic alloy compounds, the high-T_c materials were rather exotic oxide compounds. Initially rather exotic means were employed to grow and pattern films for devices. Bob Laibowitz led IBM's first high-T_c films effort, growing YBaCuO e-beam co-deposition from three sources in a partial oxygen environment, followed by post annealing in oxygen [113]. It was a challenge at first to achieve the correct $YBa_2Cu_3O_{7-\delta}$ composition, with secondary phases turning out to be particularly sensitive to processing. To get around this, the initial YaBaCuO films, polycrystalline and grown on sapphire substrates, were patterned by first coating the film with a gold film layer, subtractively patterning that gold layer by ion milling and then using the patterned gold layer to mask an ion implantation that transformed the YBaCuO film into an insulator. Early dc SQUIDs made in this manner by Roger Koch and collaborators employed two 17 μm wide "weak links" in the polycrystalline YBaCuO film, but did operate up to 68 K. While a collection of grain boundaries in these structures provided the needed weak links [114], the weakly coupled grains throughout the superconducting film were also the source of much extraneous flux noise due to easily moved trapped vortices. Soon Praveen Chaudhari with Laibowitz, Koch, and other IBM collaborators first demonstrated that epitaxial YBaCuO films grown on $SrTiO_3$ substrates could carry high critical currents[115]. After that, it was not long before labs around the world demonstrated even better films grown *in situ* on heated substrates in oxygen atmospheres by methods such as laser ablation, first introduced by Dijkkamp, Venkatesan, Wu and collaborators at Bellcore [116], and by more conventional single-target sputtering, developed a bit later by a number of groups. High quality epitaxial films that were superconducting near 90 K or above became the norm for device development. A variety of means were developed for making more deliberately placed high-T_c Josephson junctions, including bicrystal grain boundary junctions from IBM [117], bi-epitaxial devices from the startup company Conductus [118], edge junctions from IBM and a number of other research labs, step-edge grain boundary junctions from TRW, Jülich, Siemens, and IBM, step-edge SNS devices from Biomagnetic Technologies (BTI) and NIST, and nanobridge devices. For a surprisingly long time, however, the lowest noise 77 K SQUIDs remained IBM random grain boundary devices, albeit ones made from large grain TlBaCaCuO films (transition temperature $T_c \sim 120$ K). Wen Lee at IBM's Almaden lab grew the films for these devices, which were patterned and tested at IBM Yorktown [119]. The energy resolutions demonstrated above about 100 Hz for the best TlBaCaCuO dc SQUIDs at 77 K were lower than the specification for the commercially available BTI 4.2 K rf SQUID.

While the energy sensitivity of the best high-T_c dc SQUID was good, their magnetic field sensitivity was poor. To achieve high field sensitivity it is necessary to focus the flux picked

up in a large superconducting loop into a sensitive, lower inductance SQUID. To efficiently focus the flux, a multi-turn superconducting flux transformer is required. The highly anisotropic nature of the high-T_c materials and the need to avoid high-angle grain boundaries in films, made fabricating superconducting cross-overs required for these to be quite a challenge. This challenge was tackled both by John Clarke and his students at U.C. Berkeley and by postdocs Byungdu Oh and Walter Eideloth at IBM in collaboration with Bill Gallagher and John Clarke's former student Roger Koch. Their friendly competition was the subject of an August 1990 Science news article, in which Robert Pool noted that leading up to the September Applied Superconductivity Conference that Clarke's team had a flux coil working but no 77 K SQUID while the IBM team had 77 K SQUIDs but not yet a superconducting cross-over technology [120]. By the time of the 1991 APS March meeting in Cincinnati, however, both groups had 77 K SQUID magnetometers containing multilevel flux transformers working [121, 122]. Because of the challenges involved in making a multilevel epitaxial film technology with insulated cross-overs, both groups took the approach of sandwiching one substrate with the high-T_c SQUID against a second substrate containing the pickup coil and flux transformer structure (Figure 14 (a)). Both groups used $SrTiO_3$ as the epitaxial insulator in their cross-over structures. The IBM group used a SQUID with the weak links made on the join in a bicrystal of $SrTiO_3$ as demonstrated earlier by Gross [117]. For their SQUID, the Berkeley group used an MgO substrate with a rotated $SrTiO_3$ buffer layer in seeding biepitaxial growth to form the SQUID weak links [123]. Patterning by this time was becoming more conventional, with the IBM group patterning all of their pick-up coil layers by ion milling while the Berkeley group patterned their YBaCuO layers with a dilute nitric acid wet etch and the insulator by ion milling. Nevertheless, obtaining multilayer epitaxial growth in the cross-over

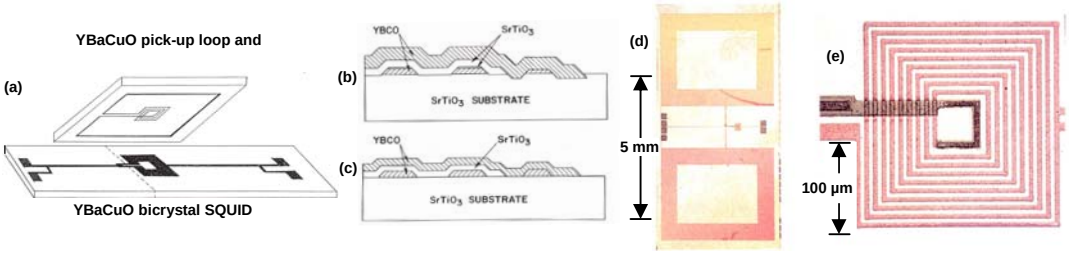

Fig. 14. High-T_c SQUID cross-over technology approach (a) with sandwich configuration, and (b) epitaxial superconducting cross-over structures patterned by ion-milling (b) and wet etching (c), and gradiometer pick up coil structure (d) with 10-turn coil (e) for focusing the differential flux signal patterned by wet etching.

structures and maintaining good superconducting interlayer contacts and high critical currents in cross-over structures were challenges.

IBM's Federal Systems Division in Manassas, Virginia, had by 1988 begun a program to develop magnetic anomaly detectors for U. S. Naval Coastal Systems Center in Panama City, Florida. Roger Koch from Research was involved in this work from its inception using low-T_c technology. For this application, sensitive gradiometers were required, and the development of high-T_c gradiometers became the next focus of the high-T_c SQUID activity in Yorktown, which had already been partially sponsored for some time by the U. S. Office of Naval Research. By July 1991, post doc Walter Eideloth (since deceased) had fabricated a 77 K high-T_c gradiometer with an 8 mm baseline and a 10-turn input coil [124] with the structures patterned entirely by wet etching (Figure 14 (c, d, e).).

Plans were underway to fabricate still larger base-line gradiometer using two-inch and three-inch $NdGaO_3$ and $LaAlO_3$ substrates that were becoming available within the Consortium for Superconducting Electronics. Larger base-line high-T_c gradiometers were not to be, however, as IBM's technical approach to the Naval challenge shifted to a new gradiometer

concept, the three-SQUID gradiometer (TSG), which was invented by Roger Koch in 1990 [125]. This gradiometer utilized a novel feedback circuit to accomplish the gradient sensing. In the three SQUID gradiometer, a central SQUID magnetometer is used as a null detector and the feedback flux to keep its null is also applied to the other two SQUID magnetometers. Those two SQUIDs are then read out differentially, producing a gradient signal. The feed back signals can all be applied with normal metal wires, so the baseline for the gradiometer can be arbitrarily long. By late 1992, Koch and his team had demonstrated both low-Tc and high-T_c three SQUID gradiometers [126], with the high-T_c gradiometer having a high frequency noise floor of 6 pT/(m-√Hz) at 77 K.

In the ensuing years, considerable effort went into understanding extraneous noise source which these gradiometers would experience in motion in the earth's field. A "flux-dam" was invented to help prevent excessive flux penetration into high-T_c pickup coil structures [127]. Some of these developments were done jointly with the company Quantum Magnetics, which partnered with IBM in 1994 with the intention of commercializing high temperature SQUID technology[1].

In the late 1990's, after Quantum Magnetics was practicing high-T_c SQUID technology, the remaining IBM Research effort led by Roger Koch focused on the gradiometer instrumentation aspects. (The thin film technology team under Bill Gallagher shifted focus to tunnel junctions with magnetic rather than superconducting electrodes, targeting magnetic random access memory. From this effort has come a proposal for a dense hybrid magnetic tunnel junction-Josephson junction memory [128].) By 2000, in a joint effort with the Naval Coastal Systems Station, a prototype three-SQUID gradiometer was developed and demonstrated to have a system gradient noise level of 0.8 and 0.3 pT/(m-√Hz) at 1 Hz and 10 Hz, respectively [129]. This system used 77 K dc SQUID magnetometers that were available commercially by then from Conductus.

As often happens, a novel concept invented to improve a new technology can also be applied to older technologies. The new gradiometer concept implemented with feedback could also be employed using fluxgate magnetometers. While Koch and his team continued development of the SQUID gradiometers in partnership with Quantum Magnetics, they also started work on a three-magnetometer gradiometer employing room-temperature fluxgate magnetometers [129]. Although not as sensitive as the high-T_c technology version, the three fluxgate magnetometer gradiometers became the focus of on-going U. S. Navy attention for autonomous underwater vehicles for mine detection.

C. Changing IBM Research and Researcher Interests

Beginning in the early 1990s several external factors began drawing IBM researchers away from superconductivity research and from high-T_c SQUID development. IBM's dominance within the computer industry was ending as CMOS microprocessor-based systems were becoming more powerful. IBM's business was significantly impacted. Budgets within IBM were cut, including that of the Research Division [130]. Within the Research Division, the portion of the research portfolio aimed at software and services was increasing relative to that aimed at hardware to match a similar change in IBM's business. These changes directly affected the size of the fundamental physics and materials research efforts, but less so the size of more applied efforts coupled to business opportunities. Other factors influenced those efforts.

[1] The high-T_c SQUID activities of Quantum Magnetics were later absorbed into an entirely high-T_c SQUID focused start-up, Magnesensors, Inc., to which rights to IBM SQUID technology were transferred. Magnesensors today focuses on magnetic assays for life science applications using its own high-T_c SQUID magnetometer technology.

In 1994, magnetic tunnel junctions, structurally very similar to Josephson tunnel junctions but with magnetic electrodes, were shown to have high magnetoresistance at room temperature, an effect predicted almost 20 years earlier by IBM theorist John Slonczewski based on spin polarized tunneling studies from superconducting electrodes into magnetic electrodes [131]. In collaboration with Stuart Parkin at IBM's Almaden lab, Bill Gallagher's superconducting device fabrication team was able to demonstrate the first microfabricated magnetic tunnel junctions [132] with large tunneling magnetoresistance at room temperature. That team provided the nucleus of skills for a growing program to develop magnetoresistive random access memory technology (MRAM). This is a large IBM program still today, with potential for providing a dense fast memory that may scale further than DRAM. The MRAM work in a lab which managed to retain superconductivity know-how and capability, has also spawned a small current IBM effort, led by Gerald Gibson, to demonstrate a hybrid superconducting-magnetic memory concept [128].

Also in 1994, IBM's profitable, but non-core Federal Systems Division was sold to Loral (two years later to be acquired by Lockheed Martin) to raise cash the company needed at that time. This took away the IBM system-level interest driver for magnetic anomaly detection. Roger Koch and his group continued magnetic detection work for a few years after this, but also joined the move towards magnetic memory research particularly the fundamental device aspects. However, beginning in the early 2000's he began shifting work towards a Josephson junction implementation of quantum bits (qubits) for quantum computation, the subject of our next section.

Both the hybrid memory exploration and the Josephson junction qubit experimental efforts had a low barrier to entry due to the PARTS process being so compatible with CMOS back-end-of-the-line processing. IBM Research in Yorktown maintains a 200 mm CMOS process line capable of handling non-standard CMOS materials, in which the PARTS process can continue to be run.

V. SUPERCONDUCTING DEVICES FOR QUANTUM COMPUTING AT IBM

Mark B. Ketchen

A. Quantum Computing

In 2012, just over 100 years after the discovery of superconductivity, superconducting devices are again under intense investigation at IBM for potential information technology applications. This time the target application area is quantum computing in which devices configured with superconducting electrodes and Josephson junctions form superconducting bits, or qubits, which are seen as essential building blocks in a future quantum computer. In this section we will briefly discuss quantum computing and mention some of the exciting recent developments in this latest superconducting device endeavor at IBM.

Quantum computing is an exciting emerging field in information technology with potential to solve certain mathematical problems that are intractable with today's computers. It is in its very early stages, where basic discoveries in the physics laboratory and new theoretical constructs continue to occur on a regular basis. Original insights on energy dissipation and reversibility in logic operations by IBM's Rolf Landauer [133] and Charles Bennett [134] established a context for thinking about quantum mechanical systems as computers. In 1994 Peter Shor [135] at Bell Labs developed a quantum algorithm that could express a number as its prime factors and required only polynomial resources of time and quantum bits, offering an exponential speedup over known classical approaches. As modern encryption is based on fac-

toring of large numbers, interest in quantum computing increased dramatically with Shor's insight.

The fundamental logical entity in quantum computing is the qubit, an elementary quantum mechanical system having a ground state and a single excited state. Classically such a system would, at any given time, be either in the ground state or the excited state, but quantum mechanics allows the system to be in a superposition of both states at the same time. For a collection of N distinct such classical systems there are 2^N possible combinations, but the entire collection can be in only one of these at a given time. In quantum mechanics, however, this collection of qubits can at any time be in an extended superposition or entangled state involving components of some or even all of the possible combinations, requiring $\sim 2^N$ coefficients to specify. The execution of an algorithm involves a sequential set of simultaneous gate operations on all of the qubits in the system that, over time, establishes a particular quantum state, the coefficients of which embody the solution to the problem at hand. A final readout of some fraction of the qubits as classical 1's and 0's (the readout operation forcing each target qubit into one state or the other) gives the answer to the problem. The successful execution of the algorithm requires that the "coherence" of the entire collection of qubits be maintained, that is that there are no qubit transitions that are inadvertently induced by mechanisms such as internal dissipation, thermal noise or externally introduced noise.

It is instructive to consider some specifics relevant to the factoring problem to illustrate the potential of quantum computing. In 2010 a 231 decimal digit number was factored on a large highly parallel machine [136]. It was estimated that a conventional single core 2.2 GHz microprocessor would take about 1500 years to accomplish this feat. Increasing the number of decimal digits to 600 leads to an estimated single 2.2 GHz core microprocessor execution time of 10^{14} years [137], a direct consequence of the exponential growth in the difficulty of the problem with the size of the number to be factored. With a quantum computer, however, the situation could be very different. It can be shown that in the case of perfect qubits (no decoherence) an appropriately configured and controlled assembly of N = 10n perfect qubits could in principle be used to factor an n-decimal-digit number. The 200 decimal digit number would then require only about 2000 perfect qubits, while the 600 decimal digit number would only require of order 6000 perfect qubits. Furthermore with an operating frequency of about 1 MHz, it has been estimated that the 200 digit number could be factored in about five minutes while the larger number would take approximately two hours [137]. The hardware resources grow linearly with the size of the number to be factored while the execution time grows in polynomial fashion, much slower than exponential.

This all sounds extremely favorable for the quantum computing approach, but there is one very big problem: qubits are not perfect. Over time they decohere which leads to erroneous gate operations. If the coherence time is T_2 and the time for a gate operation is Tg then at best the error rate ε will be of order $T\mathrm{g}/T_2$ leading to a likelihood of successful gate operation, or fidelity, of $f = (1 - \varepsilon)$. It was originally thought that such errors would rapidly render the execution of an algorithm meaningless, but then in the mid-1990s concepts were conceived for error correction that would enable correct execution of algorithms in the presence of errors at the physical gate level that would be detected and fixed [138, 139]. However, such error correction would only work for error rates below some threshold which was originally thought to be of order 10^{-4}. In addition, the total number of qubits required for an error corrected system is a factor of η greater than required for the case of error free qubits, and right at the threshold, $\eta = \infty$. As ε is further reduced the value of η rapidly decreases. It is likely that ε will have to be reduced by a factor of 100 or so beyond threshold to get η into a reasonable range of 100-1000.

At present, two factors are combining to make the picture for quantum computing more realistic. First, on the theory side, architectures employing so-called surface codes have been

devised that enable carrying out a general algorithm at considerably higher error thresholds than originally thought possible [140]. For example if qubits are configured in a square lattice with each qubit directly coupled to only its nearest neighbors, the error threshold can be at about 1%. Secondly, on the experimental side, there has been great progress developing qubits with improved coherence. At present there are a number of physical systems that are being investigated as candidates for qubits [141, 142,143], with superconducting qubits being a strong contender among them. IBM's present program in experimental quantum computing is based entirely on superconducting qubits [144].

B. Experimental Quantum Computing Effort at IBM

The original work on experimental quantum computing at IBM was headed by Ike Chung at IBM's Almaden Research Laboratory in the late 1990s using nuclear spins as qubits in a liquid state NMR approach. He with students from Stanford carried out a number of impressive experiments, including factoring the number 15 into its prime factors (3 x 5) [145]. The liquid state NMR approach soon proved to be very difficult to scale up beyond about eight to ten qubits. This realization along with others led David DiVincenzo at IBM to develop a set of criteria that must be met for a qubit technology to be considered scalable [146]:

1) A scalable system of well-characterized qubits, each being a well defined two-level quantum system
2) A universal set of quantum gates composed of interacting qubits to serve as the building blocks for a quantum computer
3) An efficient procedure to initialize the quantum system to a known state
4) The ability to perform qubit-specific measurements, i.e., high fidelity readout of individual qubits
5) Long coherence times compared with the average time for logic gate function

These "DiVincenzo criteria" have served as the guiding light for experimental quantum computing ever since. There is clearly "more to it" than just good coherence (criterion number 5), but good coherence is a fundamental necessary requirement and has motivated much of the experimental quantum computing work to date at IBM and elsewhere. As coherence has improved the focus is changing more to multi-qubit experiments and the hard engineering aspects that must ultimately be managed in order to scale up to useful systems.

At IBM in the early 2000s Roger Koch and David DiVincenzo under the strong encouragement of Nabil Amer launched an effort to develop superconducting qubits. Other groups were also working seriously on superconducting qubits, including, for example, those at NEC, Yale, NIST (Boulder), U. C. Santa Barbara, Delft, and Saclay. The first demonstration of a superconducting qubit was at NEC in 1999 where a qubit with T_2 = 1 ns coherence time was developed [147]. IBM's effort in superconducting qubits was, from its inception, motivated by the DiVincenzo criteria and in particular the necessity for scalability. This basically came down to working on improving the coherence time of qubits that were deemed to be scalable. The IBM team, including extremely talented engineering support, was expanded to include Matthias Steffen in 2006 and then Mark Ketchen following Roger's untimely death in 2007. This team, with considerable encouragement and support from the government, subsequently worked on a number of different superconducting qubit designs motivated by both internally generated ideas and advances reported by other groups working in the field. The enterprise has continued to grow with the addition of a number of other strong players. After being stuck at T_2 = 10 ns for a very long time, IBM is today a world leader with T_2 in the range of 10 – 100 μs [148, 149,150], which is at the threshold of what is needed for error correction with surface-code-based systems.

IBM's present vision of a future quantum computer [144] involves a 2D surface code implementation with only direct nearest neighbor connections. A skew square lattice has evolved, as shown in Figure 15. Each qubit capacitively couples to two resonators and a group of four qubits plays a role equivalent to that of a single qubit in the original square lattice scheme where each qubit would have had to couple to four resonators. The qubit itself consists of a single capacitively shunted Josephson junction that is weakly coupled to the resonators. The ground state of the qubit corresponds to the fundamental LC self-resonance of the capacitively shunted junction. Higher energy levels would be equally spaced (quantum mechanical harmonic oscillator) except for the non-linear inductance of the Josephson junction which leads to smaller spacing as the energy increases. As a result the ground to first excited state has a unique transition energy as required by DiVincenzo criterion number 1. The resonators serve to physically connect qubits together and to provide a medium through which they interact. Resonators can also be used to "read out" qubits. In a very basic experiment a single qubit is coupled to a single resonator where, for example, the fundamental frequency of the resonator is at 10 GHz and the 0 to 1 transition of the qubit occurs at 6 GHz. The qubit initially in the ground state can be placed in the 1 state by applying the appropriate microwave pulse at 6 GHz. The cavity is then measured in reflection by applying a short microwave pulse in the vicinity of 10 GHz. The amplitude and phase of the reflected signal will be modulated differently depending on whether the qubit is in ground ("0") or first excited ("1") state. Repeated measurements can thus be made to determine the coherence times of the qubit.

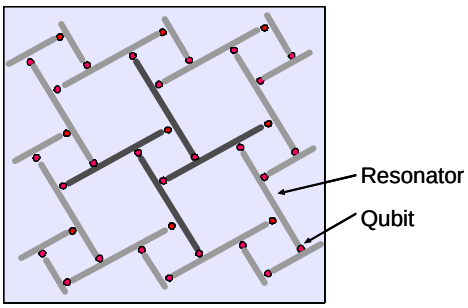

Fig. 15: Qubit – resonator fabric for surface code implementation.

IBM is at present working on two different flavors of the basic qubit-cavity approach. An example of the first is shown in Figure 16 (a) which is a system abstracted from the fabric of Figure 15 consisting of three qubits and two coplanar waveguide cavities, all integrated on a silicon substrate. The cavities and coplanar waveguide inputs to the qubits are patterned in a Nb ground plane with wirebond jumpers used as crossovers. Wirebonds at the periphery of the chip connect the chip ground plane to a copper ground plane in the PC board package and also connect the chip I/O pads to the I/O lines in the package. The qubits are fabricated of aluminum using a double angle evaporation technique in combination with electron beam lithography to form Josephson junctions with linear dimensions of order 0.1 μm. The chip is operated at a temperature of about 15 mK and great care is taken to shield the system from radiation at all frequencies. The qubits are driven with externally generated microwave signals and read out with low noise amplifiers located nearby. Coherence times on the order of 10 μs are now routinely achieved and a universal gate set with $\varepsilon < 5\%$ for all gate operations has been demonstrated using an all microwave technique [149,151]. The residual losses limiting the coherence time are believed to originate in defects in the dielectric penetrated by the electromagnetic fields of the qubits and particularly at the interface between the superconducting thin films and the underlying substrate.

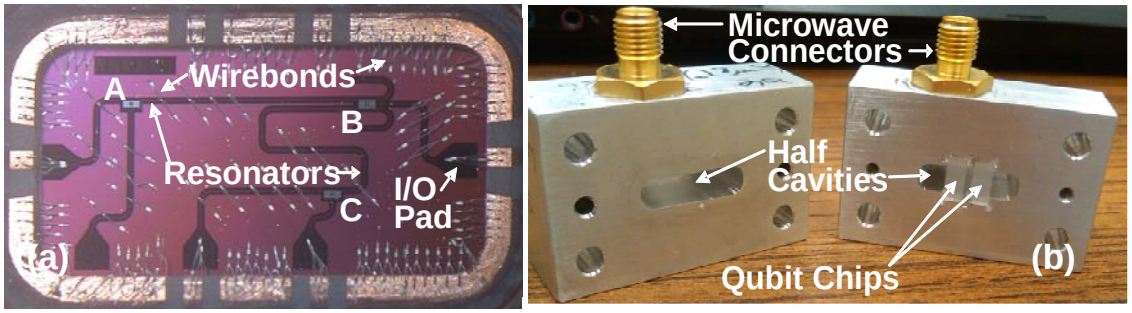

Fig. 16. (a) System with three qubits (A, B, and C) and two resonators currently under study at IBM. Measurements are made at 20 mK at frequencies in the 5 to 10 GHz range. (b) Two qubits on sapphire chips in a superconducting microwave cavity. The two halves of the cavity are bolted together, sandwiching the qubits at approximately the center. The assembly is then mounted inside a dilution refrigerator for test.

The second qubit-cavity flavor builds on an innovation at Yale University reported in 2011, where the cavity takes the form of a rectangular three-dimensional waveguide cavity with the single junction Josephson junction qubit on a sapphire chip positioned inside [152]. In this case most of the electromagnetic field energy is in free space where there are no losses. The I/O take the form of coax microwave connectors with center-pins extending into small holes in the side of the cavity. Using a carefully shielded Cu cavity assembly, IBM has recently achieved T_2 as long as 95 μs [150].

Two different approaches are being investigated to scale up such a system. The first involves placing multiple qubits in a single cavity. Figure 16 (b) shows a breakout of two halves of an aluminum cavity housing two qubits. The second approach involves multiple cavities that are coupled to each other through, for example, small holes in common walls. It is not difficult to envision a system utilizing a combination of these approaches to implement a surface code architecture having 100's or even 1000's or more qubits.

C. Status and plans

At present, systems with qubits coupled to both 3D and 2D cavities are being investigated at IBM, with an eye to scaling up to the few 100 physical qubit level. There is clearly a long way to go to get to a useful quantum computer, but IBM has a vision of what it will look like and at least the outline of a plan to get there, and superconducting devices are at the heart of that vision and plan!

VI. CONCLUDING REMARKS

As the preceding sections describe, IBM has had substantial applied superconductivity research activities for the past 57 years and these continue today. In parallel, there were very significant fundamental research activities, which are described in Part II of this article. IBM's researchers could and often did move between fundamental and applied work in superconductivity as well as in and out of superconductivity. This mobility is a factor that has helped insure IBM's considerable institutional superconductivity background is brought to bear on new areas of investigation.

Another important key to the health and stability of superconductivity research at IBM throughout this time was that research itself has remained highly valued in the business model of the IBM Corporation. One of the three core values [153] driving IBMers is "Innovation that matters – for our company and for the world." Not just symbolically, IBM's last two CEO's each made a visit to the Watson Research lab their first IBM site visit after assuming the CEO position. While there is this steadfast belief in innovation, in the value of research, and in the value of the Research Division, it is also the case that IBM's model for research has evolved. From the 1950s to the 1980s, the majority of IBM's research was done with central corporate funding and directed at technologies IBM envisioned transferring itself to its product divisions. In the latter 1980s and early 1990s, Research made a point to organize projects so as to engage substantially with IBM's product divisions, often in so-called "joint programs." This was done to insure the Research Division was connecting with usable technologies and to facilitate faster adaptation of Research technologies. The IBM Josephson program itself, while not a formal joint program, had involvement from IBM's East Fishkill semiconductor manufacturing site, where the Josephson pilot line was set up. Also as covered above, Research later engaged with IBM's Federal Systems Division for work on SQUID detection systems for their naval applications. As described above, when project learning or other factors made it clear that commercial success was unlikely, IBM management itself, generally Research managers, made the difficult decisions to scale-back or end programs. Beginning around 1990, IBM Research's partnerships became broader and began to extend to external parties as well. This move was important for the long term viability of hardware research in IBM. A large world-wide digital electronics infrastructure was emerging and commodity components were improving. IBM by this time was on a longer term trend where it would manufacture a smaller percentage of its hardware system components, meaning there was less internal drive and outlet for Research technology. External partnerships became an important part of applied superconductivity research agenda as well, both to broaden the technical skills to bring to bear on developments and to lower the cost. In 1989 IBM Research led the formation of the Consortium for Superconducting Electronics with AT&T Bell Labs, MIT, MIT Lincoln Labs, and later also Conductus. In the mid 1990s, IBM Research partnered with Quantum Magnetics on high-T_c SQUID systems. While often there was government funding of IBM's applied superconductivity research including in these partnerships, corporate funds were involved as well. The partnership commitments and corporate funds particularly serve to stabilize programs as they go through inevitable fluctuations in funding. Throughout, intellectual property generation has remained an important component of the IBM business model, particularly for Research. Patents as well as the "know how" of IBM and its researchers are highly valued. These are brought into partnership arrangements in beneficial ways.

With a corporate business model that values research and relies on innovation, and with a robust Research Division business model that supports a critical mass of skills, IBM is as well positioned as any enterprise to explore promising new technologies in the most appropriate manner, whatever the scale. In line with this model, IBM's current program aimed at quantum computing with superconducting qubits is vibrant and healthy. It appears poised to become IBM's third major thrust at developing superconducting technology for new computational frontiers. And, as everyone knows, the third time is the charm.

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The next page presents the short biographies of co-authors.

About the Authors:

William J. (Bill) Gallagher, 2008

Dr. William J. Gallagher joined IBM Research in 1978 after receiving his B.S. in Physics *summa cum laude* from Creighton University and his Ph.D. in Physics from MIT. He worked for five years at IBM on scientific and engineering aspects of Josephson computer technology and then managed IBM's Exploratory Cryogenics Research Group for six years. In 1989 Dr. Gallagher participated in the formation of the IBM-AT&T-MIT-founded Consortium for Superconducting Electronics (CSE). He served as a Director of the CSE until 1995. Since then, he has been leading efforts at IBM and with industrial partners to explore the use of magnetic tunnel junctions for nonvolatile magnetoresistive random access memory, MRAM. Currently he is senior manager of Exploratory Magnetic Memory and Quantum Computing at IBM's Thomas J. Watson Research Center.

Dr. Gallagher is a Fellow of the IEEE and of the American Physical Society (APS). He has served as Assistant to the Chairman of the APS Panel on Public Affairs, on the Executive Committee of the APS Forum on Physics and Society, on the Board of Directors of the Applied Superconductivity Corporation, and on numerous university and government lab review panels. He has over 190 technical publications and 20 U.S. patents.

Erik P. Harris, 2005

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Mark B. Ketchen, 2010

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