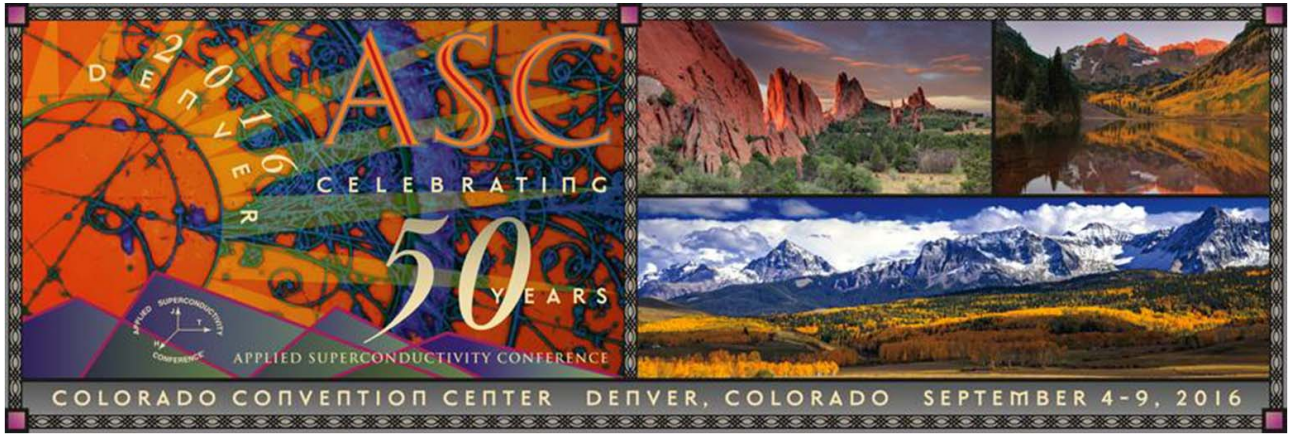
IEEE/CSC & ESAS EUROPEAN SUPERCONDUCTIVITY NEWS FORUM (global edition), October 2016.
Plenary presentation 3PL-01 given at ASC 2016; Denver,Colorado,USA, September 4 – 9, 2016.



Low-energy High-performance Computing based on Superconducting Technology

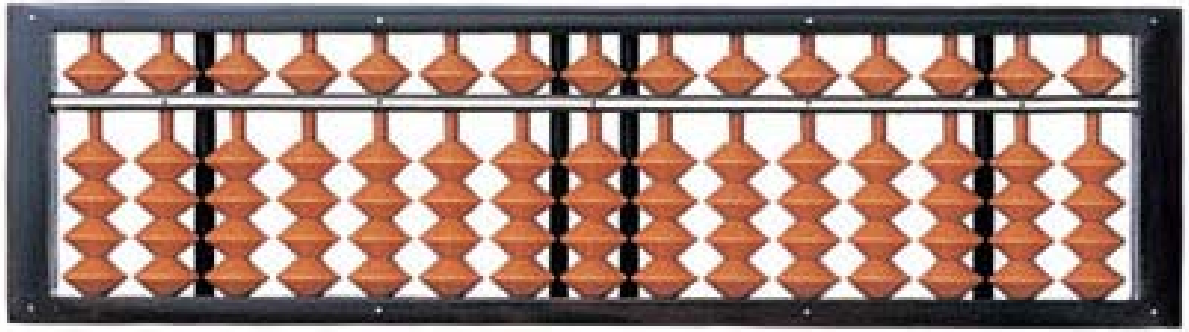
Nobuyuki Yoshikawa
Graduate School of Engineering,
Yokohama National University, Japan

The circuit was fabricated using ISTEC standard process (STP2). National Institute of Advanced Industrial Science and Technology partially contributed to the circuit fabrication.

YNU Initiative for Global Arts & Sciences YOKOHAMA National University

Question

What is this?



Outline

- Background and motivation
- Present status of superconducting computing
  - Japanese and US projects
- The minimum energy in computation?
  - Landauer's principle
  - Adiabatic computing and reversible computing
- Adiabatic quantum flux parametron (AQFP)
- Reversible QFP (RQFP)
- Summary

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Background

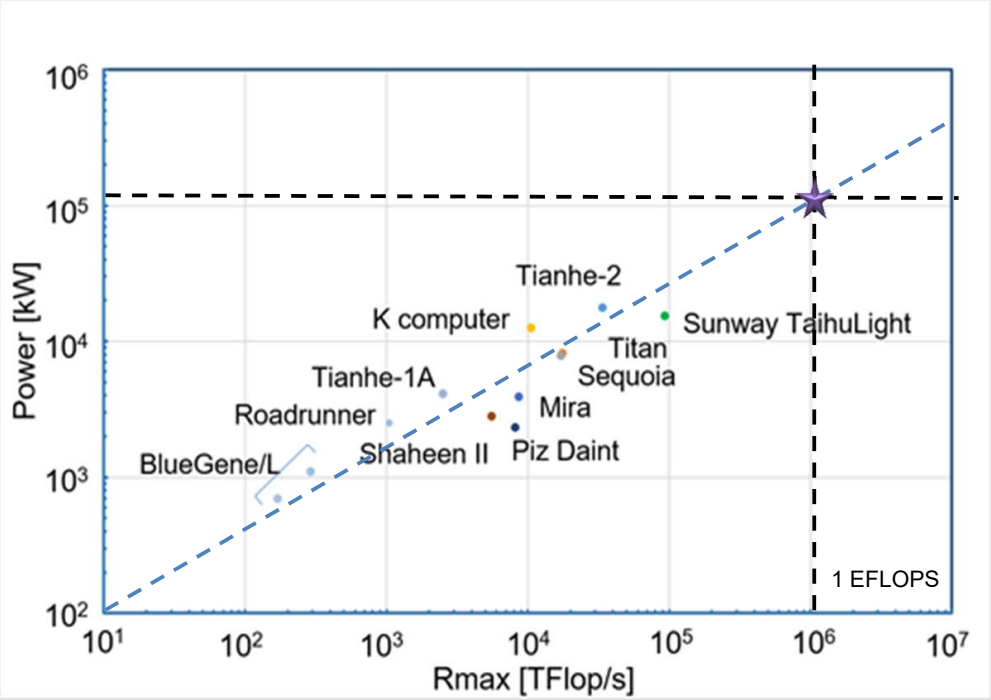
Estimated power consumption to realize an exa-scale computer

> 100 MW
~ $million/100 MW per year

K computer (Japan)

Peak performance: 10.5 PFLOPS
Power consumption: 12.6 MW

1st-ranked computers in recent TOP500



http://www.top500.org/

Low-Power Logic Devices is highly demanded.

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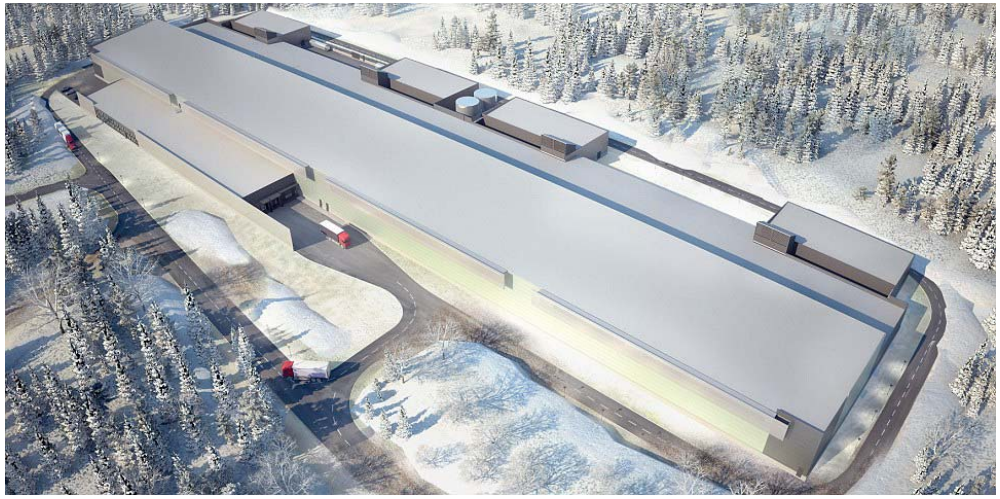
Energy Consumption in Data Centers

Explosive increase in electric power of data centers

↓

Approaching 10% of total electric power in nations

Facebook Data Center, Lulea, Sweden



Performance: 27-51 PFLOP/s
Power 84 MW average (120 MW max)

D.S. Holmes, ISS 2013, Tokyo, Japan.

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Energy Consumption in Data Centers

Electric power consumed in 100 searches in the internet

=

Electric power consumed in ironing a shirt

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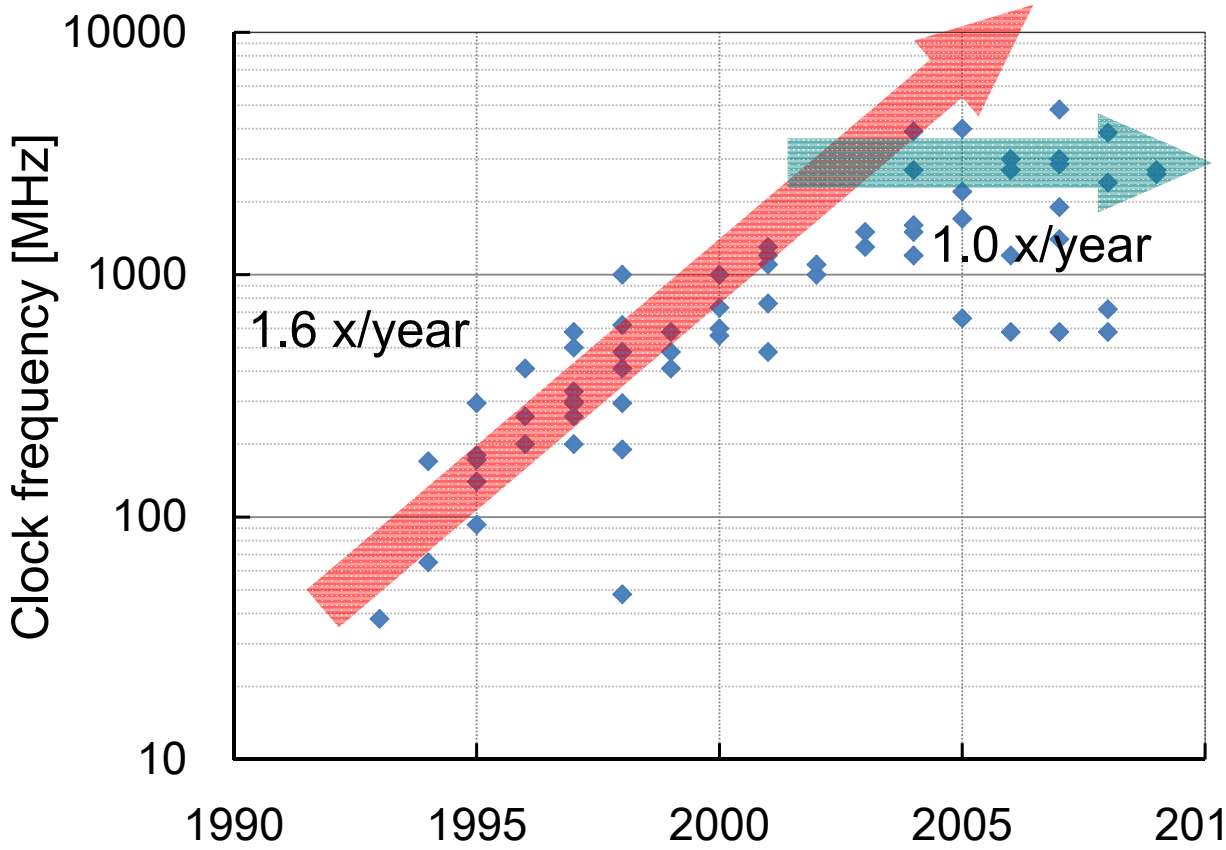
End of the Moor's Law

Trend of the clock frequency of high-performance processors



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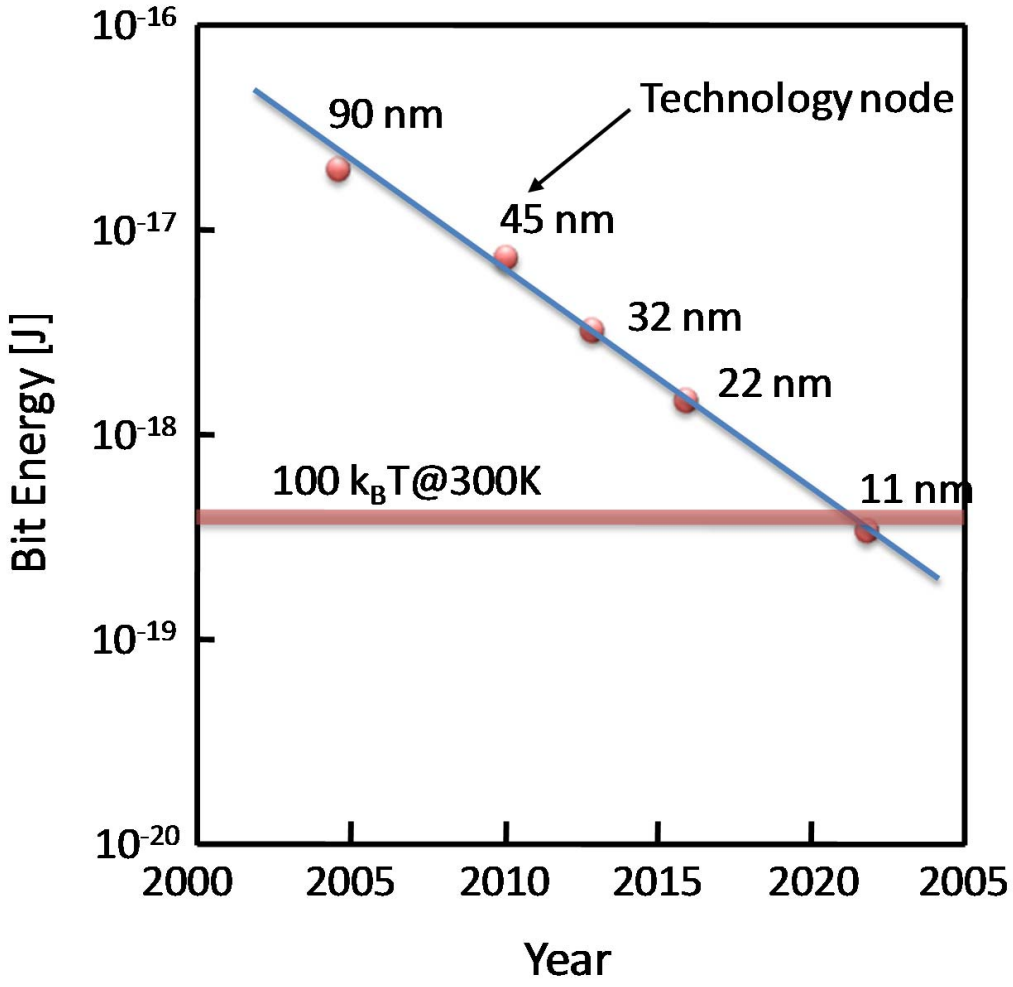
Intrinsic Bit Energy of CMOS Logic



* Actual switching energy is about three orders of magnitude larger for charging interconnects.

After International Technology Roadmap for Semiconductors, 2009 Edition.

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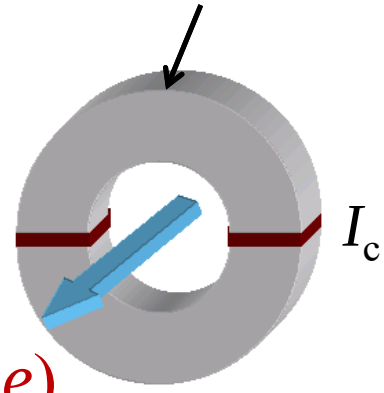
Single-Flux-Quantum (SFQ) Circuits

SFQ circuits

Superconducting loop
with Josephson junctions

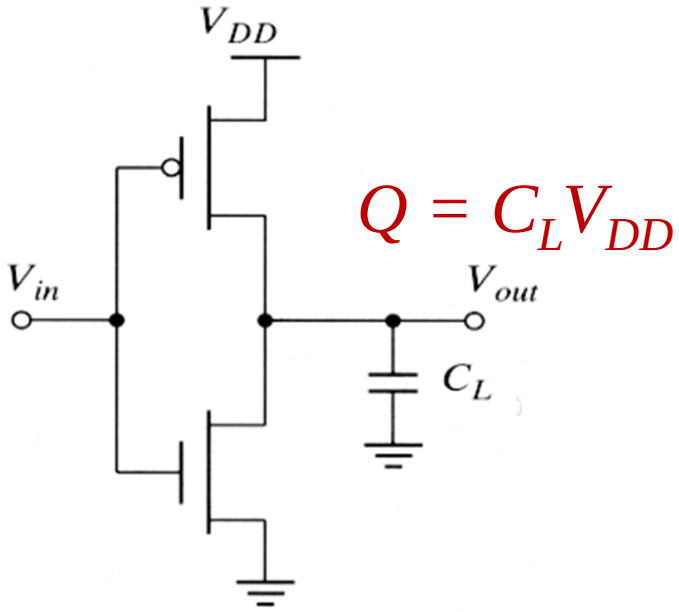


$\Phi_0 = h/(2e)$

Switching energy

$$E = \Phi_0 I_c \sim 10^{-19}\ \mathrm{J}$$

CMOS circuits



$Q = C_L V_{DD}$

Switching energy

$$E = QV_{DD} \sim 10^{-16}\ \mathrm{J}$$

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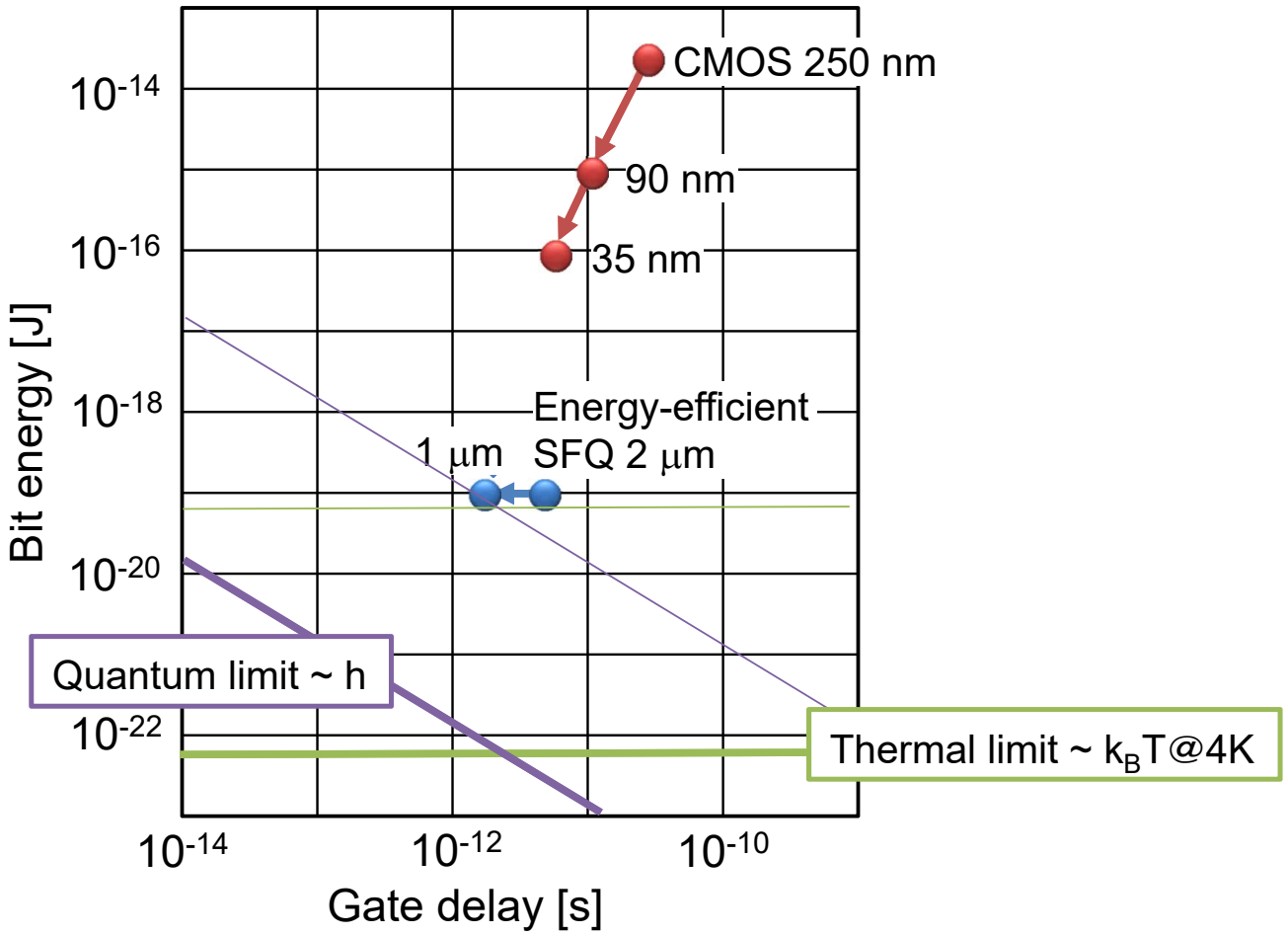
Energy-Delay Product of SFQ and CMOS



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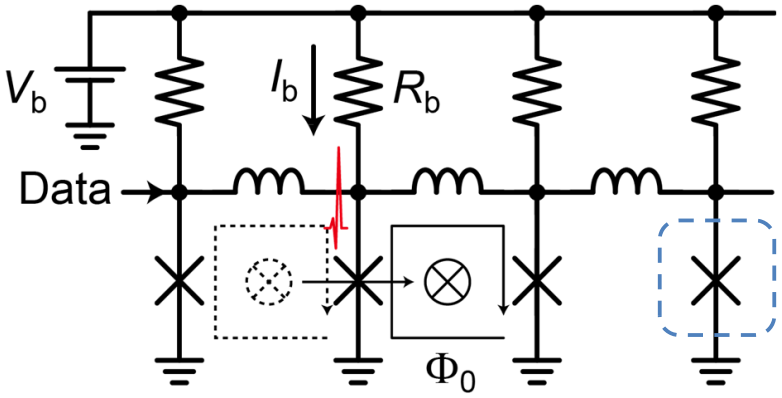
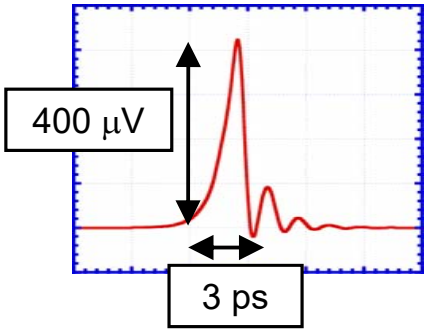
Rapid Single-Flux-Quantum (RSFQ) Circuits

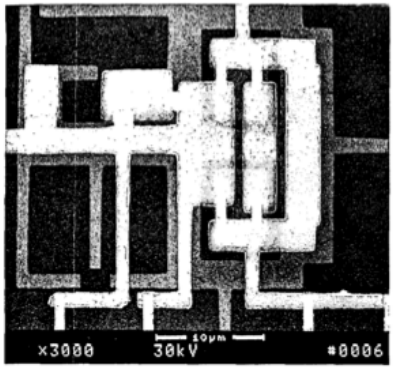


Josephson junction



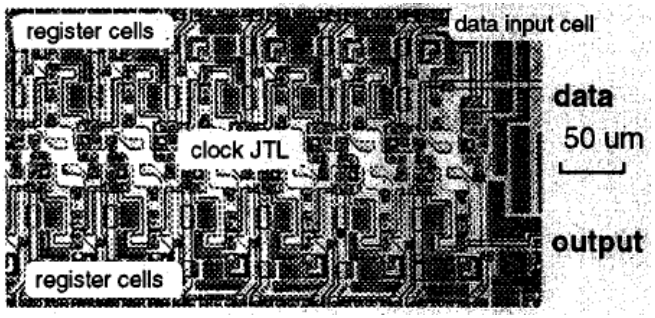
- Pulse height ~ 400 μV
- Pulse width ~ 3 ps
- Power ~ nW/gate

K. K. Likharev, V. K. Semenov, *IEEE Trans. Appl. Supercond.* 1, 3–28 (1991).



T Flip-flop operating at up to 770 GHz.

W. Chen *et al.*, *IEEE Trans. Appl. Supercond.* 9, 3212–3215 (1999).



256-b shift register operating at 12 GHz

O. Mukhanov *et al.*, *IEEE Trans. Appl. Supercond 3,* 2578-2581 (1993).

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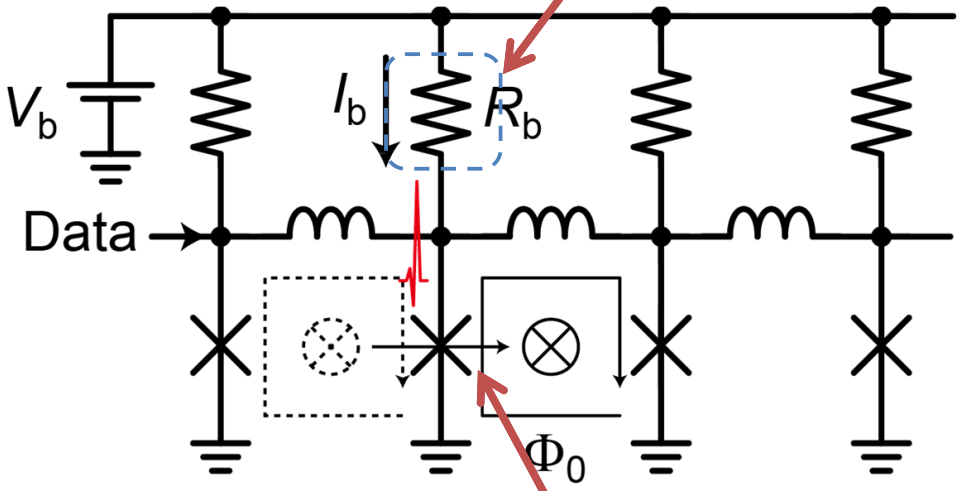
Power Consumption in RSFQ Logic

Static power dissipation:

$$P_S = R_b I_c^2$$



$$P_D \sim P_S/20$$

Dynamic power dissipation:

$$P_D = \Phi_0 I_c f$$

Reduction of static power is required.

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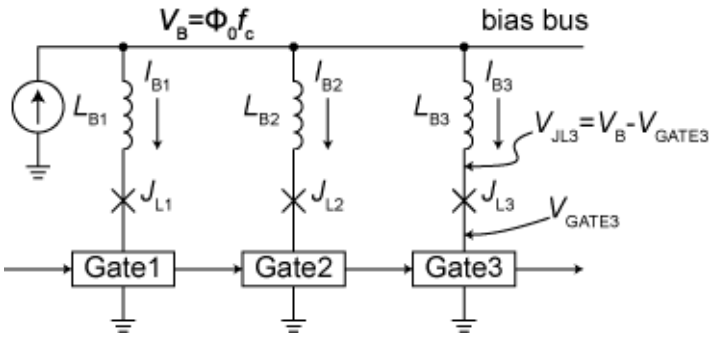
Energy-Efficient SFQ Circuits

DC Powered

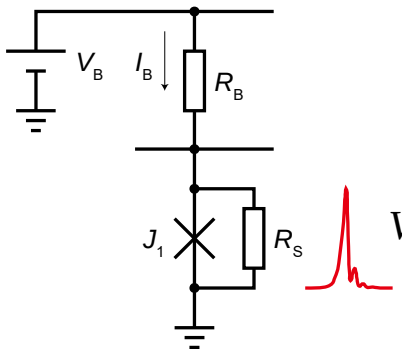
ERSFQ (Hypres)



$P_S \sim P_D \sim I_c \Phi_0 f$

O. A. Mukhanov, *IEEE Trans. Appl. Supercond.* **21**, 760 (2011).

LV-SFQ (Nagoya Univ.)



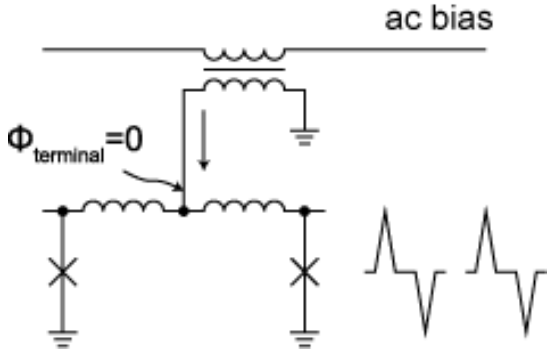
$P_S \sim 5P_D, \; P_D \sim I_c \Phi_0 f$

$$V=\frac{\Phi_0}{2\pi}\frac{d\varphi}{dt}$$

M. Tanaka *et al. JJAP* **5** 1053102 (2012)

AC Powered

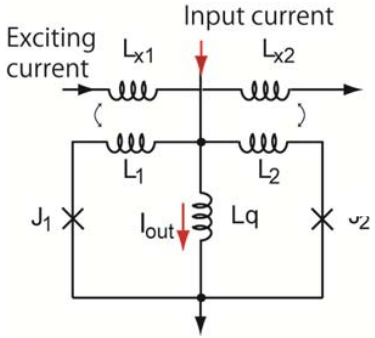
RQL (Northrop Grumman)



$P_S \sim 0, \; P_D \sim I_c \Phi_0 f$

Q. P. Herr *et al., J. Appl. Phys.* **109**, 103903 (2011).

AQFP (Yokohama National Univ.)



$P_S \sim 0, \; P_D < I_c \Phi_0 f$

N. Takeuchi, *et. al.*, *SUST*, 26, 035010 (2013).

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Japanese SFQ Computer Projects

- JST-CREST Project (FY2006 - FY2012)
  - Leader: Prof. Takagi (Kyoko Univ.)
  - "Reconfigurable low-power high-performance processor based on single-flux-quantum circuitry"
- JST-ALCA SFQ Project (FY2011 – FY2016)
  - Leader: Prof. Fujimaki (Nagoya Univ.)
  - "Superconductor electronic system combined with optics and spintronics“
- MEXT-JSPS Project (FY2014 – FY2018)
  - Leader: Prof. Yoshikawa (Yokohama National Univ.)
  - Study on Adiabatic Single-Flux-Quantum Circuits Operating in the Thermodynamic Energy Limit

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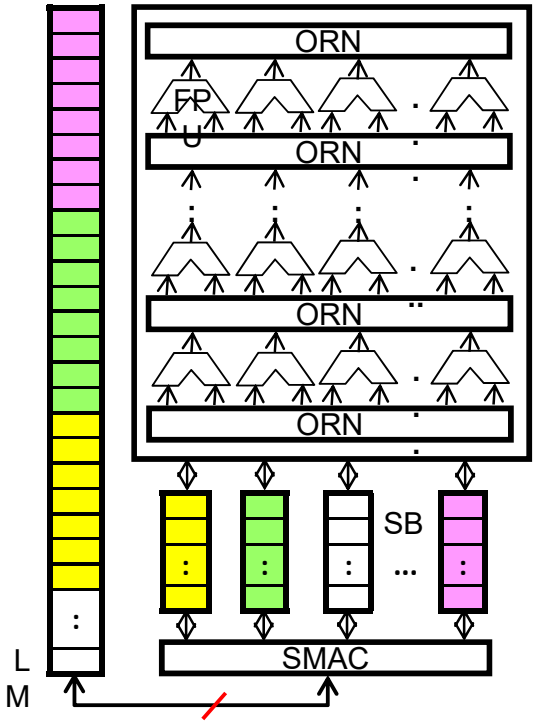
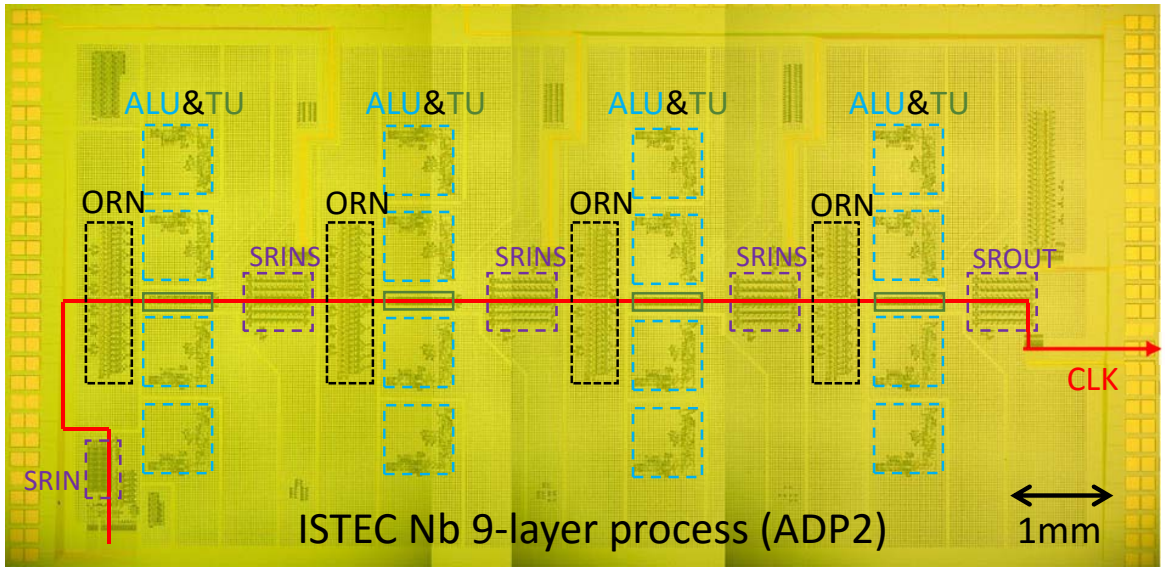
Large-Scale Reconfigurable Data-Path (RDP) Architecture for Accelerator



SB: stream buffer
SMAC: streaming memory access controller
LM: linear memory
ORN: operand routing network

4×4 SFQ-RDP



- ✓ Operating Freq. (Design): 40 GHz
- ✓ Number of Pipeline Stages: 64
- ✓ Number of JJ: 28528
- ✓ Area of Die: 14 mm x 5 mm

A. Fujimaki *et al* ASC 2012, Portland.

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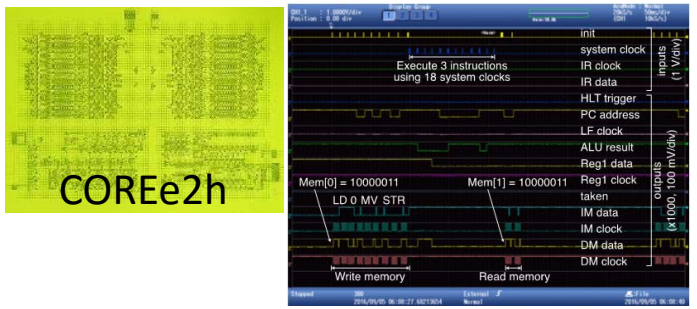
Achievements in JST-ALCA Project

Institute: Nagoya Univ., Yokohama Nat'l Univ., Kyoto Univ., NICT, AIST

The ALCA Project showed

- ✓ Low-power **microprocessors with embedded memories**,
- ✓ Static timing analyzer and **automatic routing tool**,
- ✓ Increased flexibility in logic circuits by **introducing magnetic materials**,
- ✓ Several kinds of cryogenic memories,
- ✓ **Low-power optical-to-SFQ converter** based on the SNSPD technology,
- ✓ Reliable Nb 9-layer fabrication process with **minimum junction size of 0.7 μm-sq.**
- ✓ **Cryocooled system with low-heat inflow, broadband communications** between 4 K and RT.

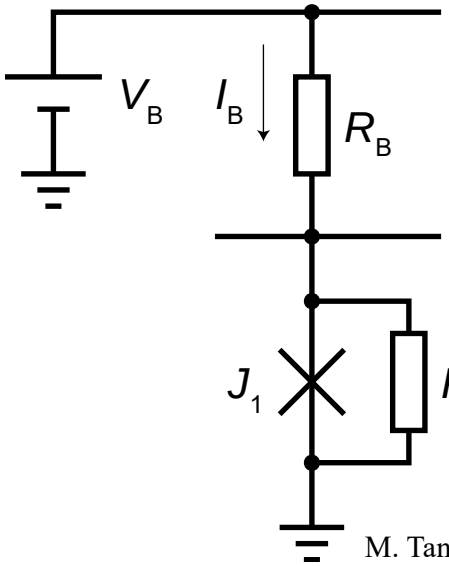


Execute all the instructions stored in the memory around 50 GHz.

Optical fiber installation

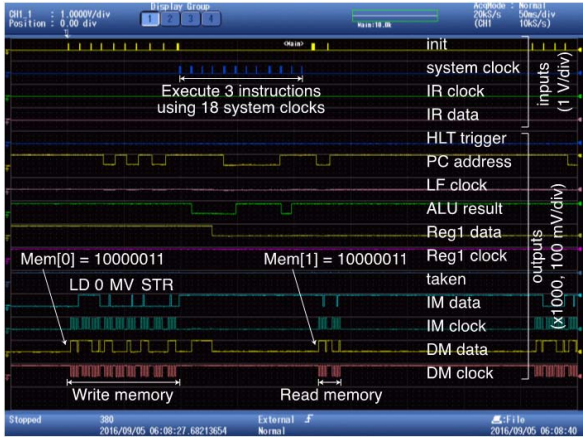
HTS waveguides on YSZ subst.

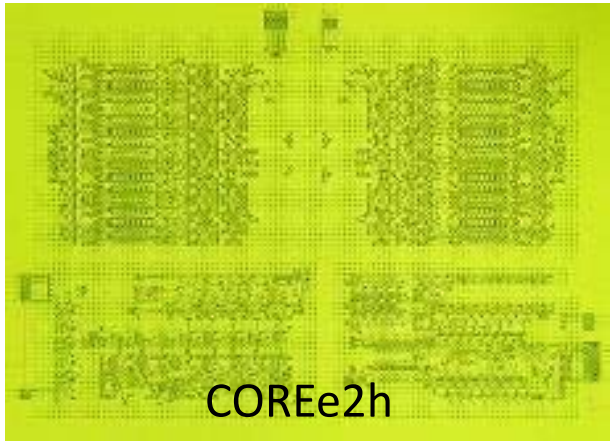
LV-RSFQ Microprocessors



Constant, lower voltage source
(1.0–0.1 I_cR_s)

M. Tanaka et al. *JJAP* **51** (2012) 053102





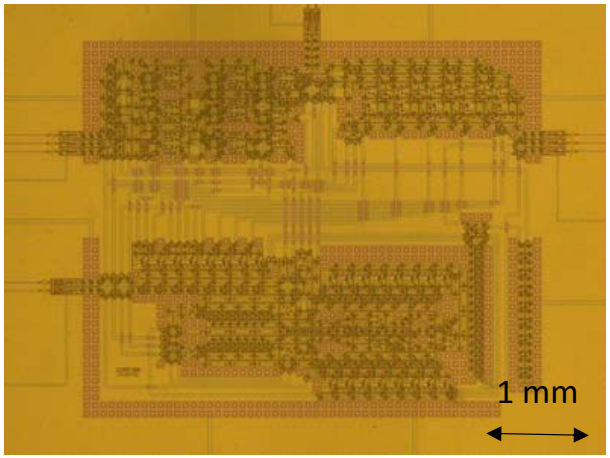
Execute all the instructions stored in the memory around 50 GHz.

- ✓ **Reduced static & dynamic energy consumption**
- ✓ **Simplified layout design**
- ✓ **Interoperability with conventional RSFQ**

See 4EOr2B-01

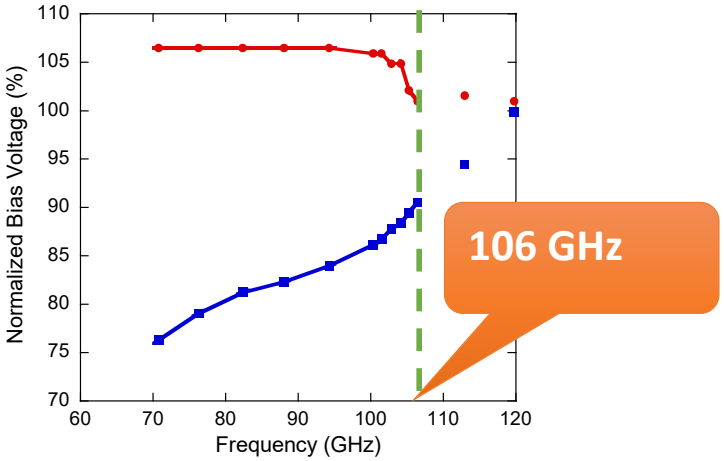
NAGOYA UNIVERSITY

100-GHz bit-serial microprocessor

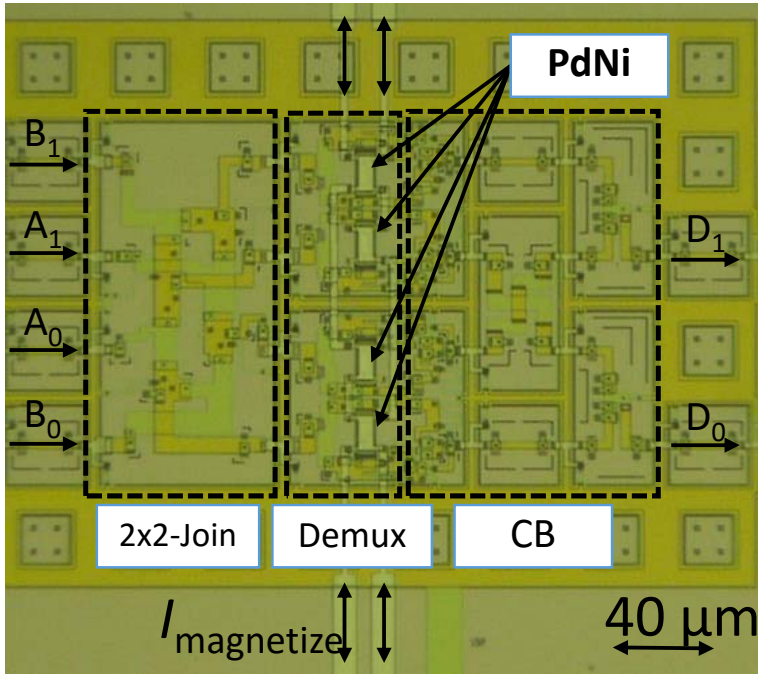


CRAVITY AIST

- ✓ AIST 20-kA/cm^2 Fab.
- ✓ Mixed-voltage RSFQ



Programmable device using magnetic material



Look-up table based on dual-rail SFQ and ferromagnet

See EPo1B-05

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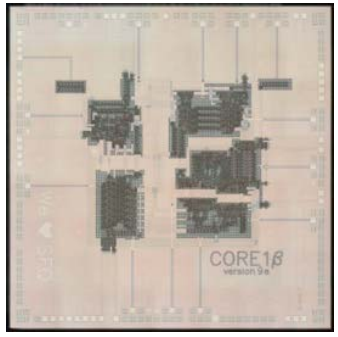
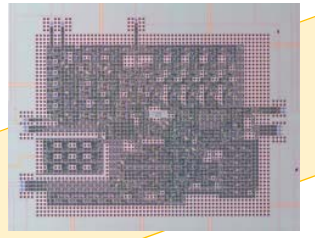
RSFQ Microprocessor Development in Japan

Bit-Serial Architecture (Complexity-Reduced)

Bit-Slice/Parallel Architecture

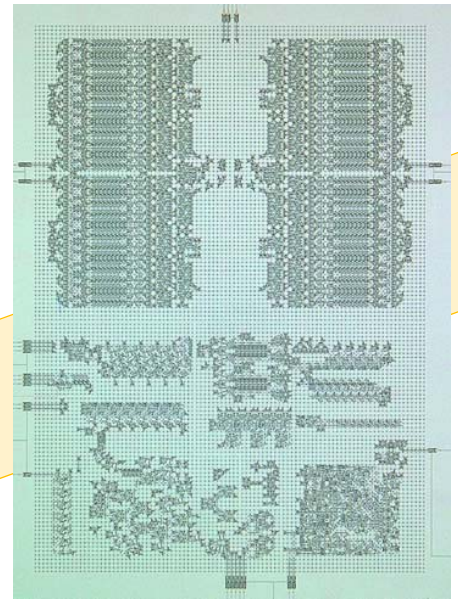


CORE1β MPU (2006)
25 GHz, 10955 JJs

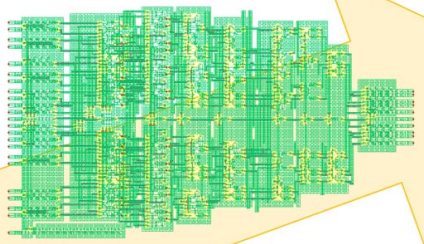


CORE1α MPU (2003)
15 GHz, 4999 JJs

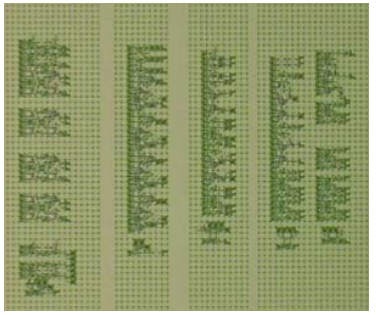
(*see* **4EOr2B-01**)



CORE e4 MPU (2015)
50 GHz, 20532 JJs



8b bit-parallel ALU (2016)
50 GHz, 4271 JJs

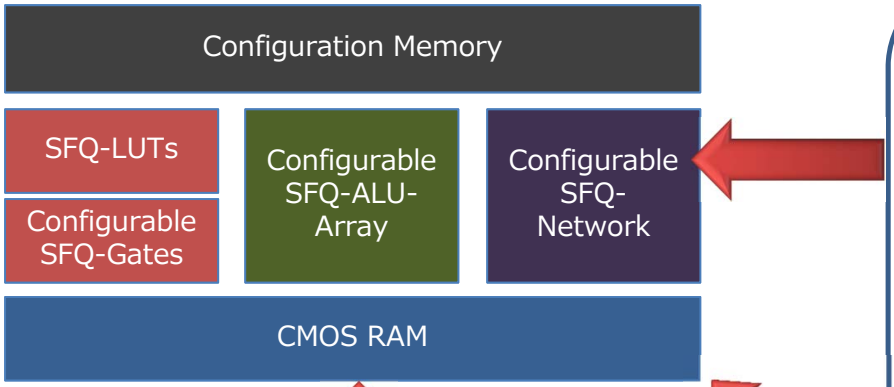


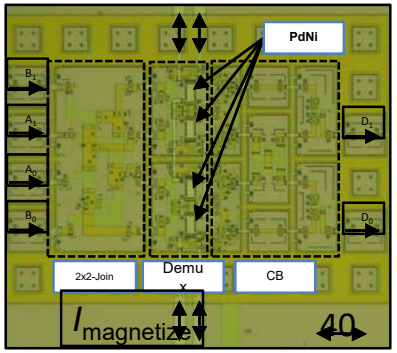
bit-slice ALU (2015)
50 GHz, 3481 JJs

YOKOHAMA National University　NAGOYA UNIVERSITY　京都大学 KYOTO UNIVERSITY　KYUSHU UNIVERSITY　CRAVITY AIST

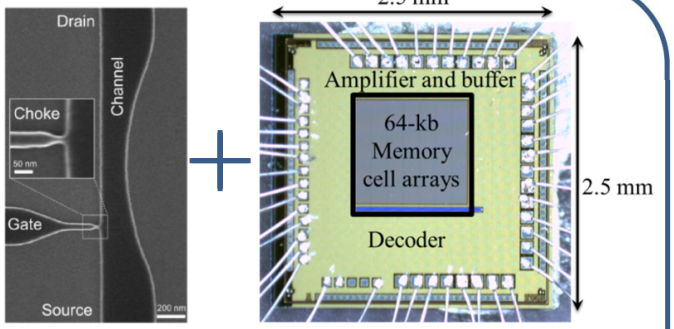
Energy-efficient SFQ Processor/FPGA for Data Center

Superconducting programmable gate array

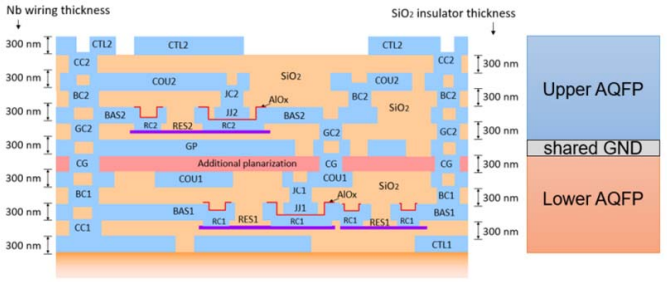




Programmable SFQ circuits using magnetic materials



SFQ-CMOS hybrid memories with nTRON



3D Josephson LSI

A. McCaughan *et al*. *Nano Lett*., **14**, 5748 (2014)

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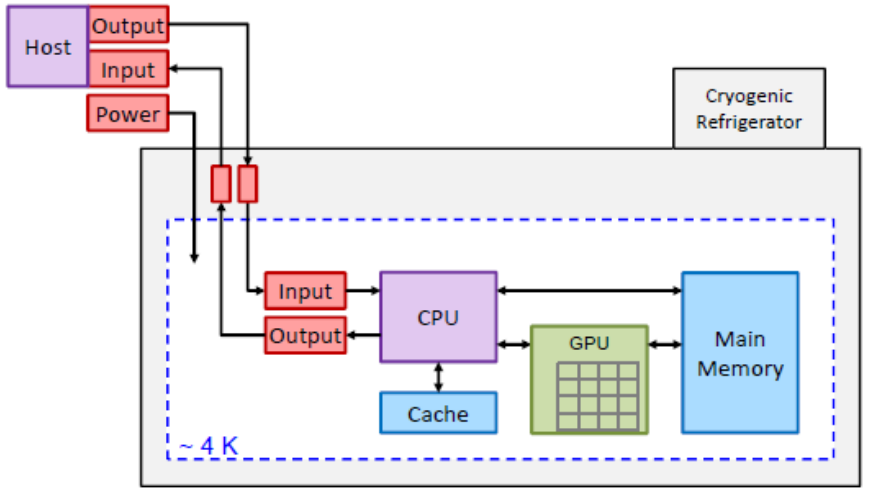
US Computer Projects

- Cryogenic Computing Complexity Program (C3)
- Sponsored by IARPA
- To demonstrate fully functional cryogenic computer
  - 64-bit processors
  - cryogenic RAM
  - > 2 GHz
  - < 1 nJ / FLOP
- 5 years



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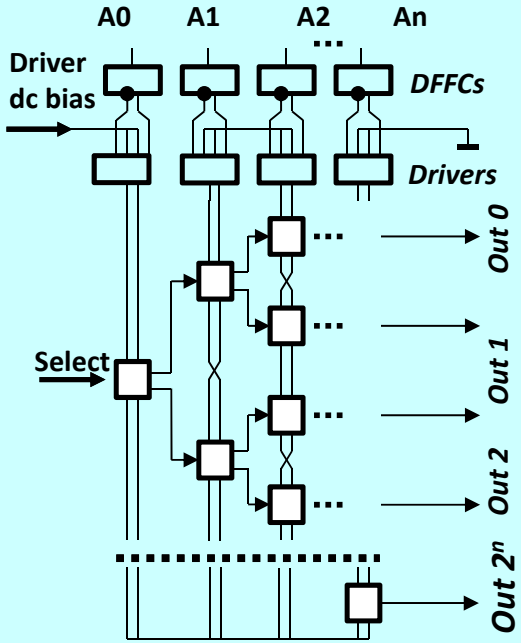
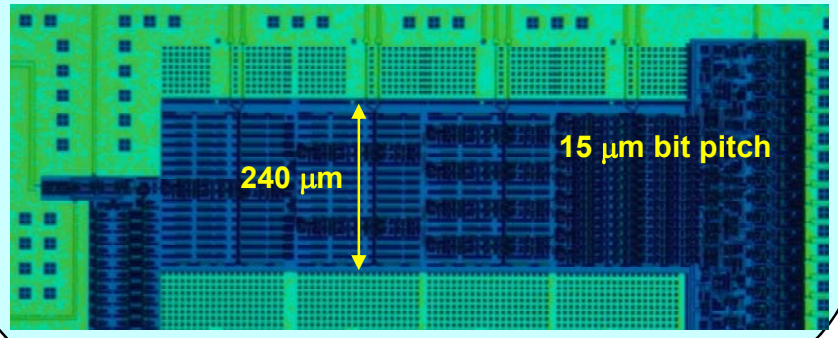
Energy-Efficient Circuits for C3 Computing

HSC & FAB

ERSFQ Compact Decoder

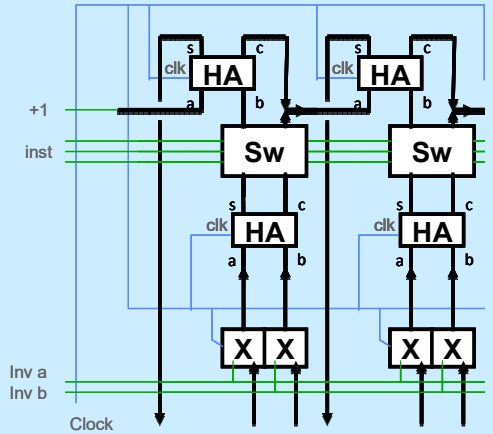


- Scalable binary-tree architecture
- Implemented with 10 kA/cm^2 HYPRES and MIT-LL fab process
- 40 ps latency, 100 aJ/clock



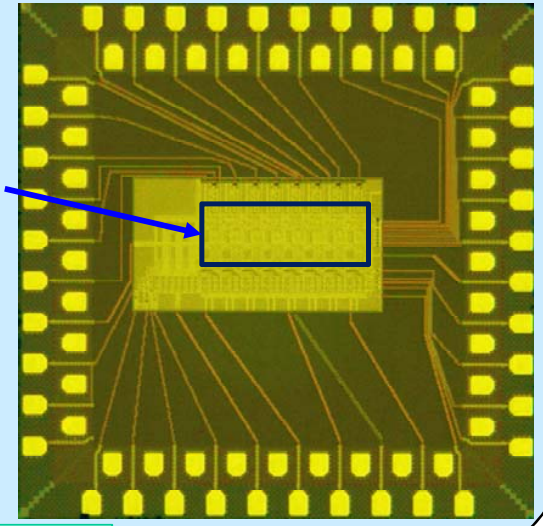
In collaboration with BBN

ERSFQ Arithmetic Logic Unit



- Wave pipeline modular design
- MIT-LL 10 kA/cm^2
- 20 GHz clock
- 34 ps / bit slice
- 12 μW for 8-bit implementation

- **8-bit ALU**
- **0.54 x 2.4 mm^2**
- **17 instructions**



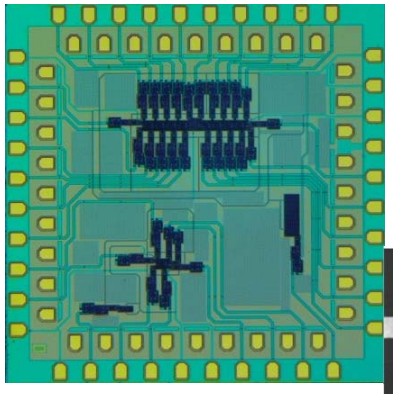
In collaboration with IBM

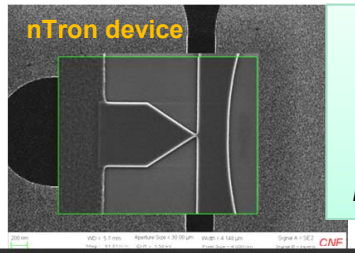
A. Kirichenko, et.al 4EOr3A-04 and 1EOr1B-06

HYPRES Integrated Memory Process (IMP)
(for C3 project and beyond)

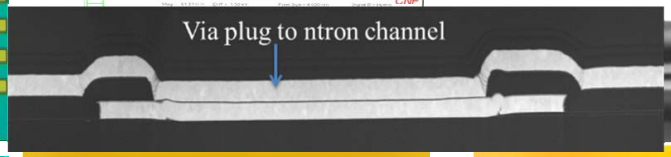
HSC & FAB

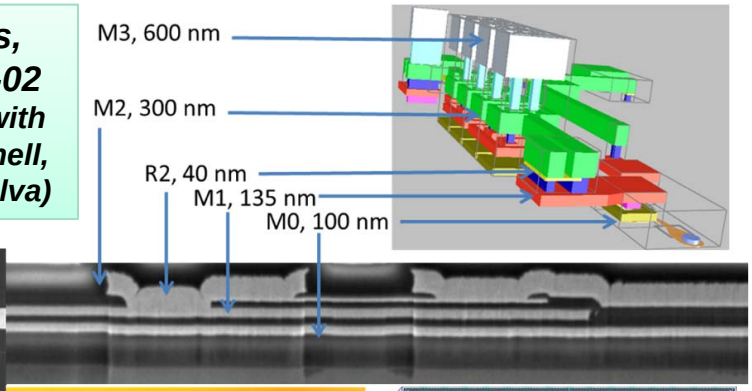
First of its kind "Digital+" fabrication process
150 mm wafer process integrating SFQ circuits, nTrons and MRAM devices

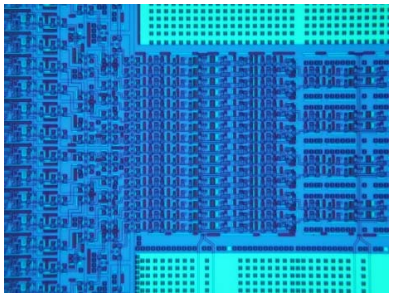


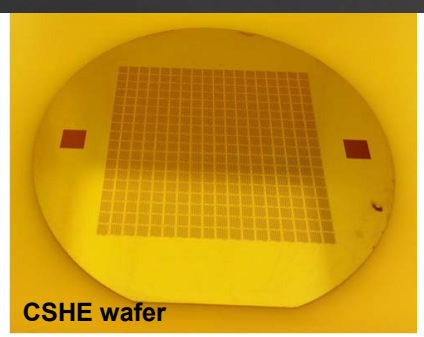


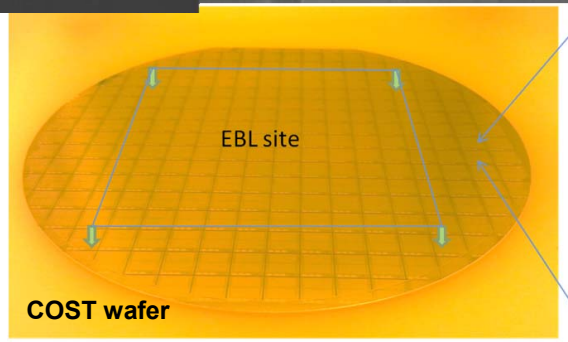
D. Yohannes, et.al 2EOr3B-02 (collaboration with BBN, NYU, Cornell, MIT, Canon-Anelva)

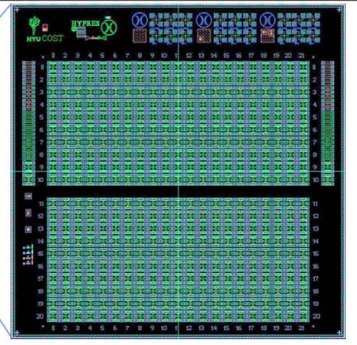












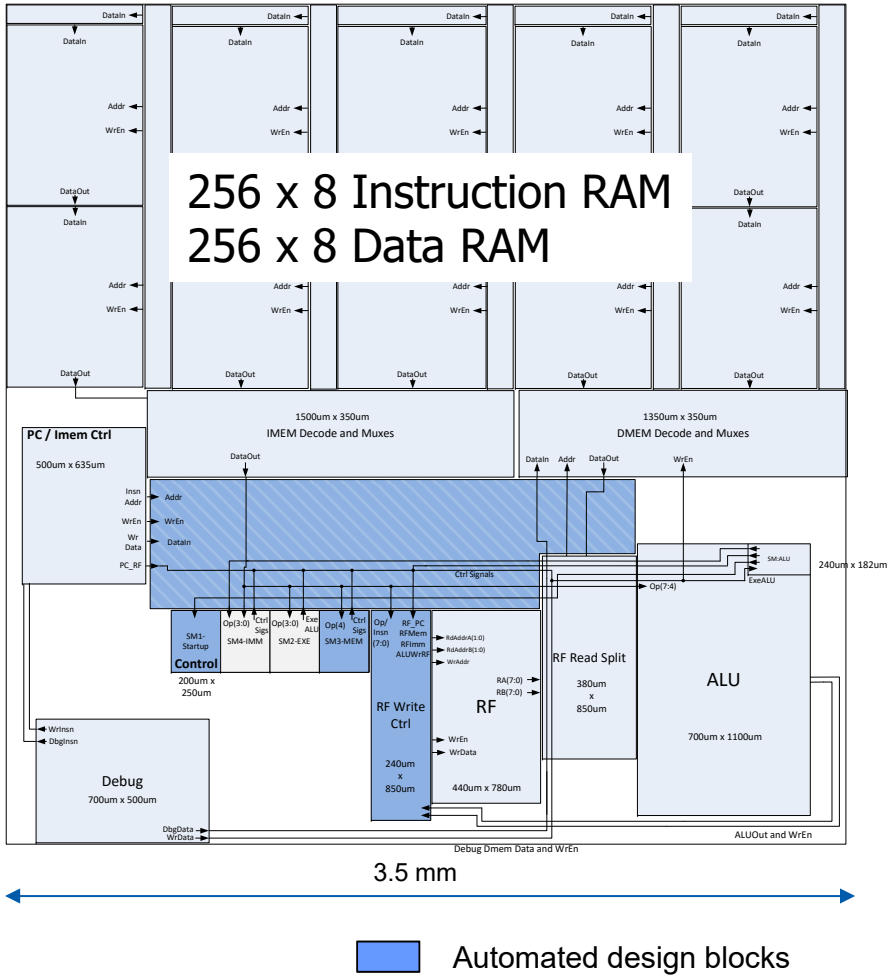
ERSFQ features
- 10 kA/cm^2
- 3 Ohms/sq
- 7 superconducting layers
- Min size 500 nm

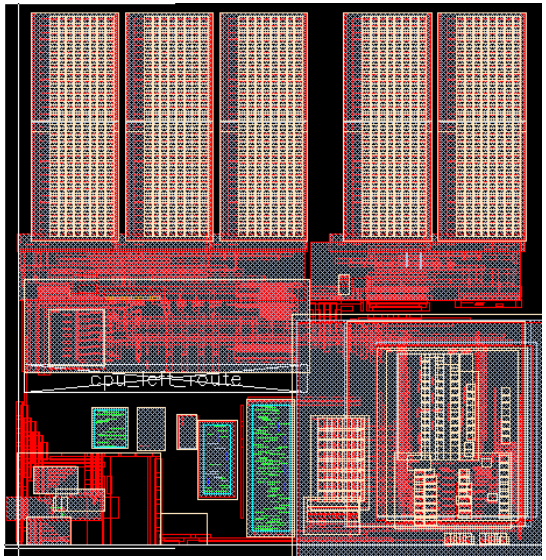
nTron features
- 15 nm thick NbN_x
- T_C = 12 K
- 10 – 30 nm gate size
- Rsq = 150 Ohm/sq

MRAM features
- Orthogonal Spin Transfer (COST)
- Spin Hall Effect (CSHE)
- EBL defined nano-pillars
- Optimized for < 0.1 mA

The first superconducting parallel 8 bit RISC CPU

NORTHROP GRUMMAN





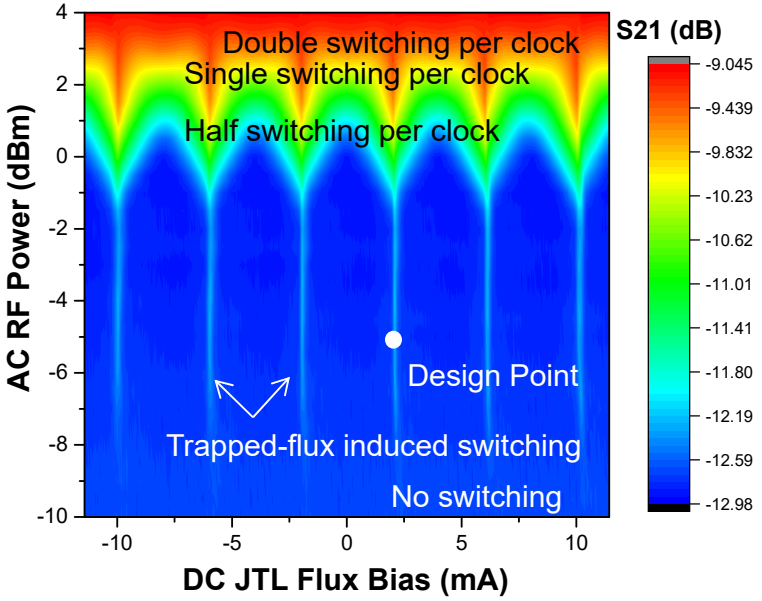
- Realizable in Lincoln 5ee processes
- Clock is 3.5 GHz
- 10 RQL clocks per instruction
- Can run benchmark algorithms
  - ✓ Fletcher Checksum
  - ✓ Greatest Common Divisor
  - ✓ Integer Divide
  - ✓ Bit Matrix Transpose
  - ✓ Least Common Multiple
  - ✓ Reverse Add

This RQL design is a practical step towards 32-bit SIMD

Resonator Clock Network Powered RQL is Successful in the Test Lab

NORTHROP GRUMMAN

Measured Resonator S21 at **10.1 GHz**

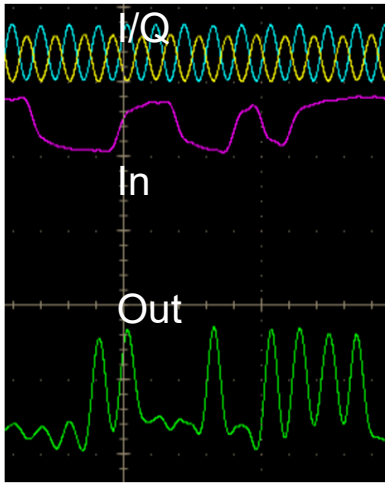


Analog Test

Digital Test

- Good signal integrity on the I/O
- No flux trapping
- Resonator is sized to power much larger circuits
- Same design applies to the 8-bit CPU

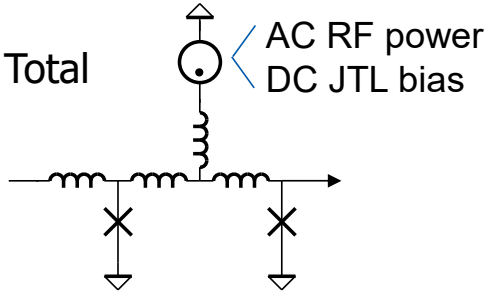
Measured Resonator at **4.5 GHz**



2,800 Junction Shift Register

49,000 Junctions Total

One stage



First Demonstration of a Scalable Technology Substrate for Superconducting Digital

Measurement translates to about 50% efficiency at the design point.

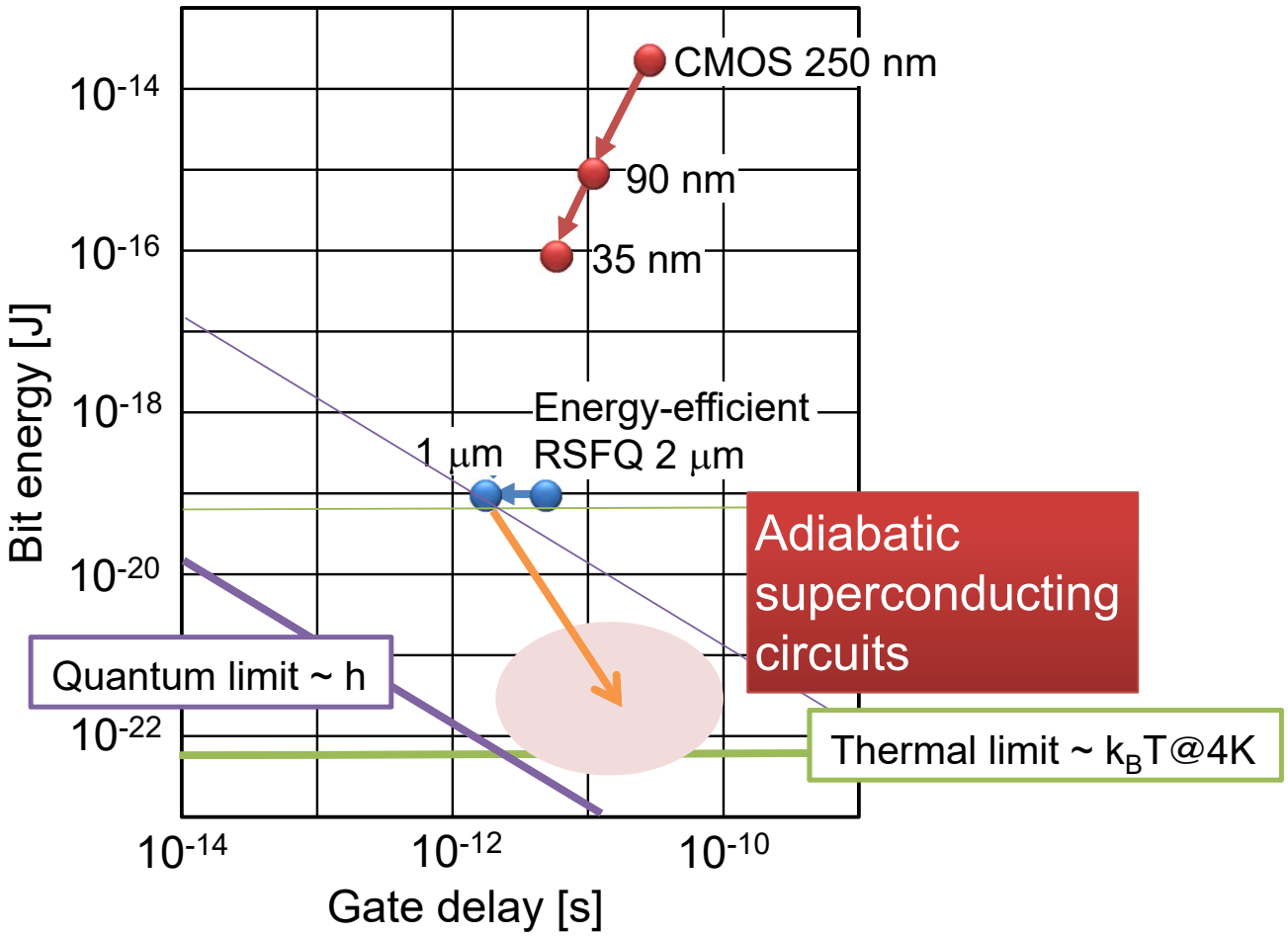
25

Outline

NORTHROP GRUMMAN

- Background and motivation
- Present status of superconducting computing
  - Japanese and US projects
- The minimum energy in computation?
  - Landauer's principle
  - Adiabatic computing and reversible computing
- Adiabatic quantum flux parametron (AQFP)
- Reversible QFP (RQFP)
- Summary

Comparison of Energy-Delay Product



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Minimum Energy in Computation?

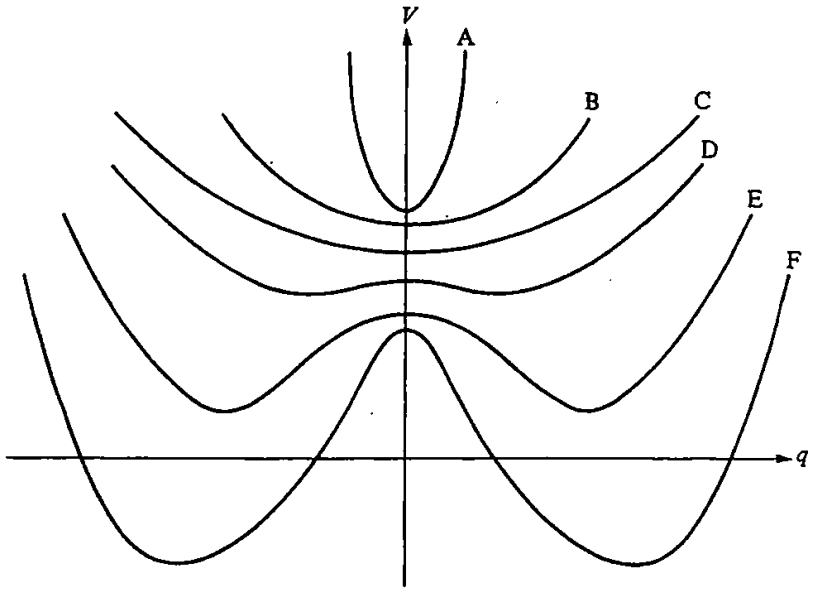

Figure 2 Time sequence of potentials starting at A (for a particle known to be near $q = 0$) and changing continuously to the deep bistable wells at F.

Adiabatic change of the energy potential of logic:
Single well → Double well

Minimum energy dissipation when the "entropy" of information decreases:
~ $k_B T \log 2$

R. W. Keyes, R. Landauer, *IBM Journal of Research and Development*, 14, 152 (1970).

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Landauer's Principle

- Equivalence between thermodynamic entropy and information entropy
- For computation reducing the information entropy, the minimum bit energy, $E_{bit} = k_B T \ln 2$, is consumed.
- For computation conserving the information entropy, there is no minimum limit of bit energy in computation.
- In erasure of results in computation, the bit energy is consumed.

R. Landauer, *IBM Journal of Research and Development* 5, 183 (1961).
C. H. Bennett, *IBM Journal of Research and Development* 17, 525 (1973).

Entropy in Information Theory

The decrease of the information entropy when the logical bit information is lost:

$$S = k_{\mathrm{B}} \ln 2$$

Helmholtz free energy

$$F = U - TS$$

The change of the thermodynamic energy

$$k_{\mathrm{B}} T \ln 2$$

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Parametric Quantron

The minimum energy in computation was discussed based on Parametric Quantron.

The minimum energy in computation

$$E_{bit} = \frac{k_B T}{\omega_c \tau \ln[\omega_A \tau p]} \propto f_{clock}$$

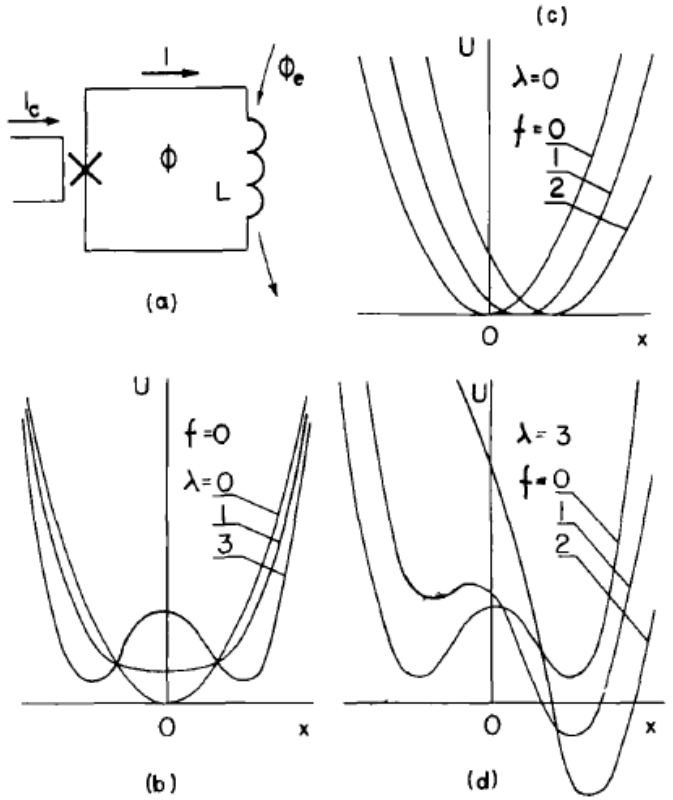

Fig. 1. Parametric quantron (a) and its potential energy U as a function of coordinate x (normalized magnetic flux Φ) at various values of parameters $\lambda=(2\pi/\Phi_0)I_M L$ and $f=(2\pi/\Phi_0)\Phi_e-\pi$ (b)–(d). Cross denotes a Josephson junction with the critical current I_M controlled by current I_c.

K. K. Likharev, *IEEE Tran. Magn.* MAG-13, 242 (1977).
K. K. Likharev, *Int. J. Theoretical Phys.*, 21, 311 (1982).

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Verification of the Landauer's Principle using Small Beads

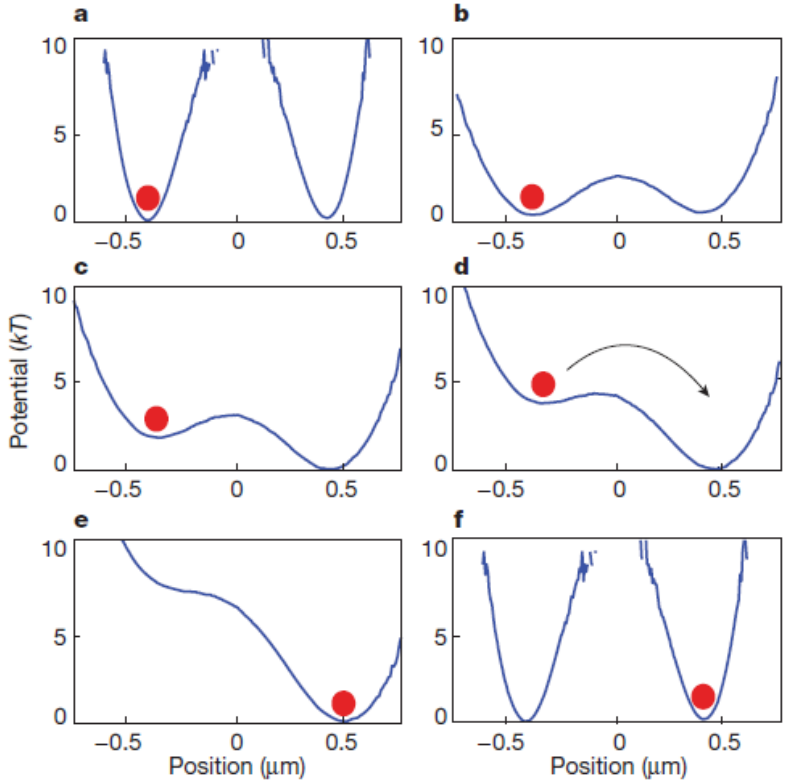

Figure 1 | The erasure protocol used in the experiment. One bit of information stored in a bistable potential is erased by first lowering the central barrier and then applying a tilting force. In the figures, we represent the transition from the initial state, 0 (left-hand well), to the final state, 1 (right-hand well). We do not show the obvious 1 → 1 transition. Indeed the procedure is such that irrespective of the initial state, the final state of the particle is always 1. The potential curves shown are those measured in our experiment (Methods).

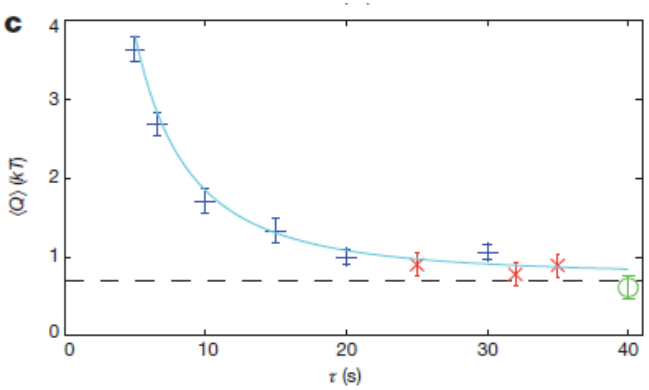

Figure 3 | Erasure rate and approach to the Landauer limit. **a**, Success rate of the erasure cycle as a function of the maximum tilt amplitude, F_{max}, for constant $F_{max}\tau$. **b**, Heat distribution P(Q) for transition 0 → 1 with $\tau = 25$ s and $F_{max} = 1.89 \times 10^{-14}$ N. The solid vertical line indicates the mean dissipated heat, $\langle Q \rangle$, and the dashed vertical line marks the Landauer limit, $\langle Q \rangle_{Landauer}$. **c**, Mean dissipated heat for an erasure cycle as a function of protocol duration, τ, measured for three different success rates, r: plus signs, $r \geq 0.90$; crosses, $r \geq 0.85$; circles, $r \geq 0.75$. The horizontal dashed line is the Landauer limit. The continuous line is the fit with the function $[A\exp(-t/\tau_K) + 1]B/\tau$, where τ_K is the Kramers time for the low barrier (Methods). Error bars, 1 s.d.

A. Berut *et al.*, *Nature*, 483, (2012) 187.

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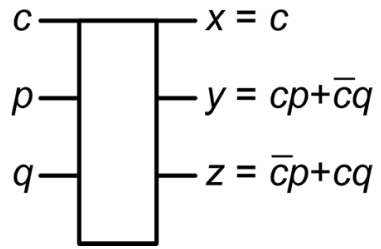
Reversible Computing

- The entropy is conserved during computation.
- No minimum energy dissipation
- Logically reversible

Dose logically reversible computing consume no energy?

Fredkin gate



Input			Output		
c	p	q	x	y	z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

E. Fredkin and T. Toffoli, *Int. J. Theor. Phys.* **21**, 219-253 (1982).

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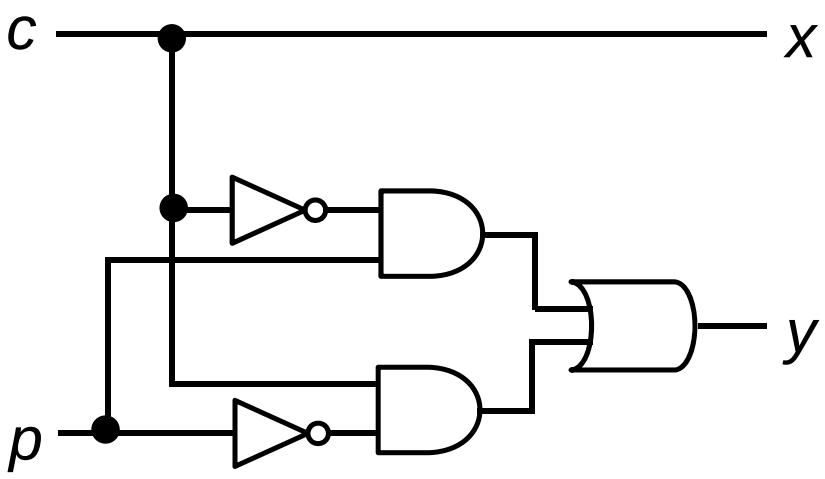
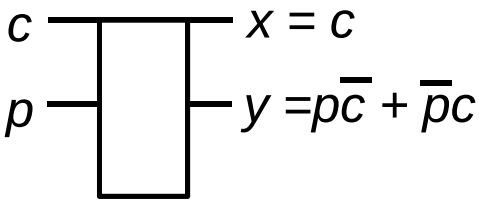
Example of a CNOT Gate



CNOT gate



Input		Output	
c	p	x	y
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Logically reversible circuits can be made by using conventional logic.

Physical reversibility is required for reversible computing.

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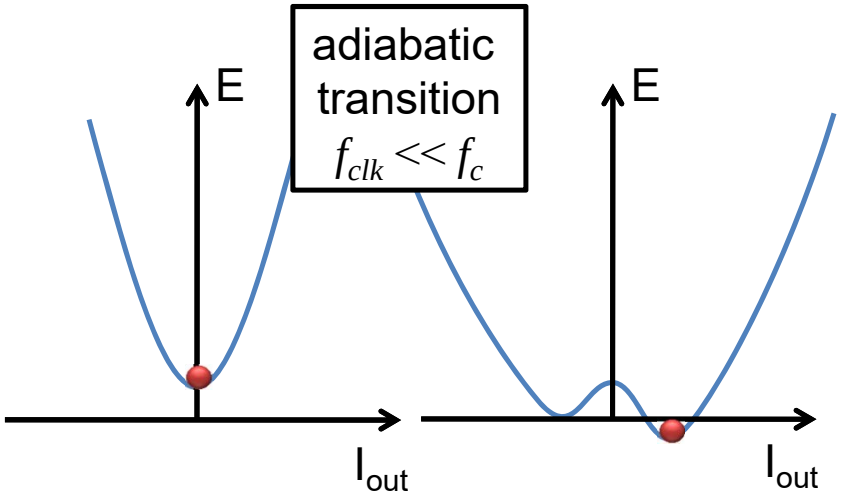
Adiabatic and Reversible Computing

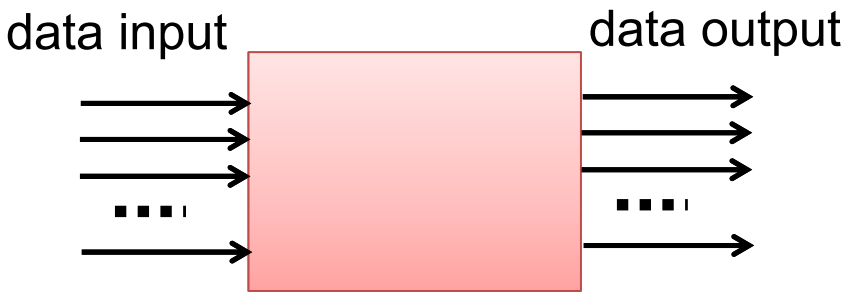
Adiabatic computing



- Potential of the system is changed adiabatically
- No nonadiabatic energy dissipation

$$E_{bit} \propto f_{clock}$$

Reversible computing



- Input data can be calculated from output data.
- Number of input = Number of output
- No change in information entropy

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Outline

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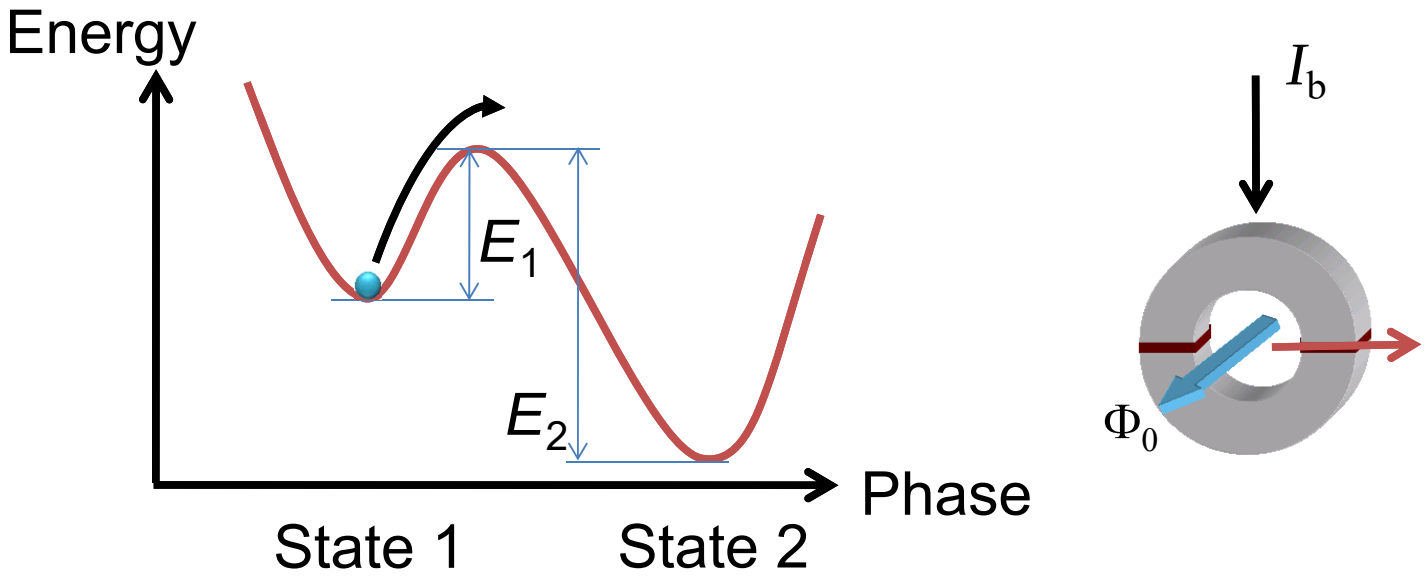
Energy Potential of RSFQ Circuits



Input energy: E_1
Output energy: E_2

Energy dissipation: E_2

Requirement for the reduction of switching errors

$E_1 > 100\ k_B T$

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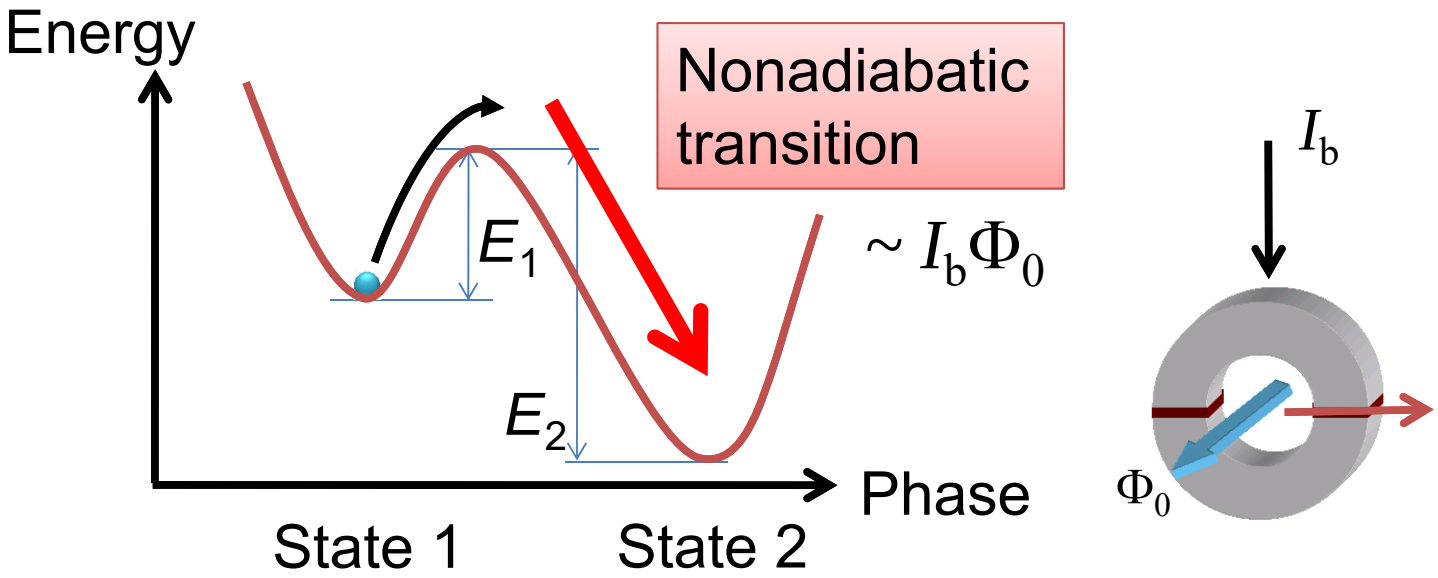
Energy Potential of RSFQ Circuits



Adiabatic operation of the system is required for energy-efficient computing.

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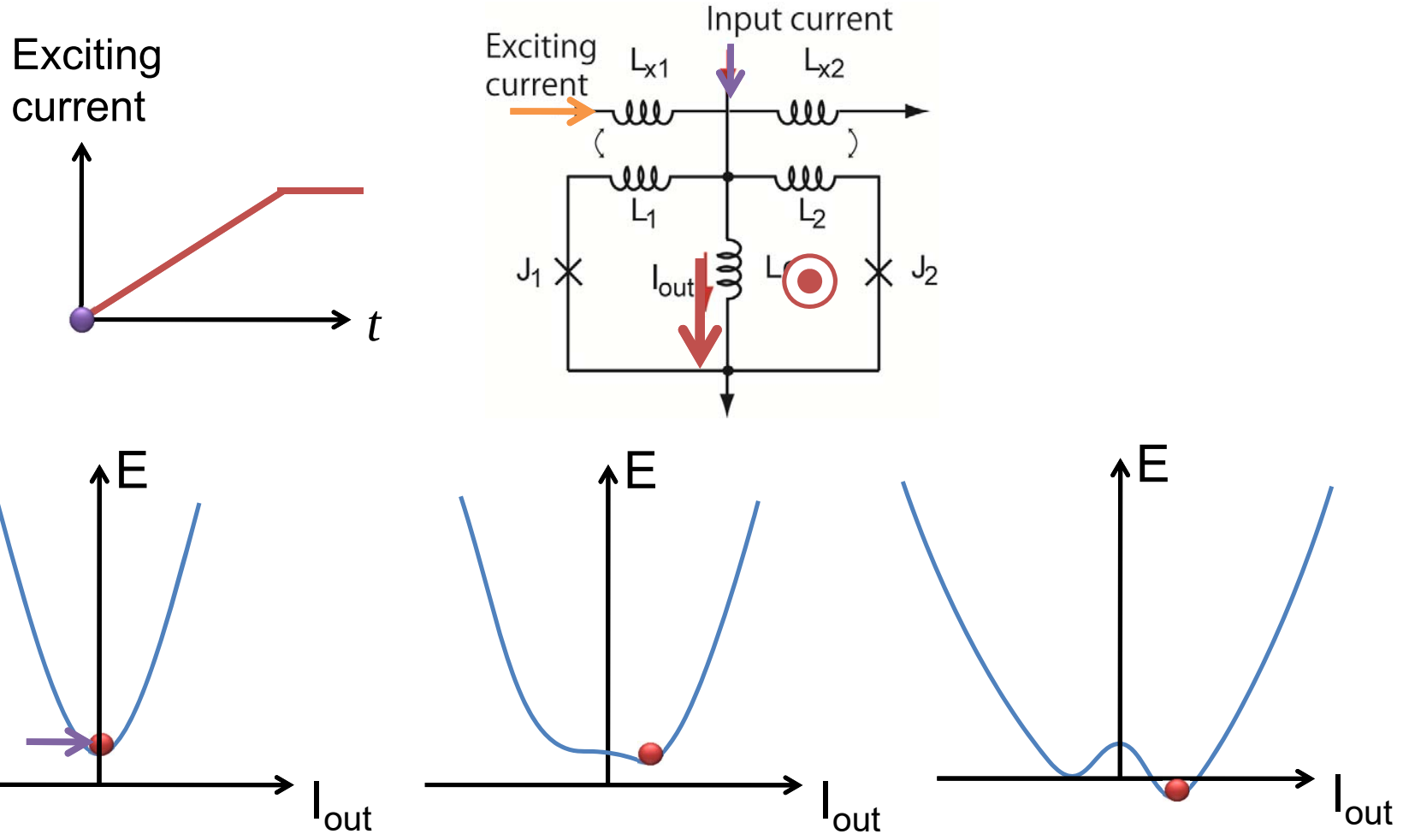
Operation Principle of Quantum Flux Parametron (QFP)



E. Goto, *Pros. 1st RIKEN Symp. Josephson Electronics, 1984.*

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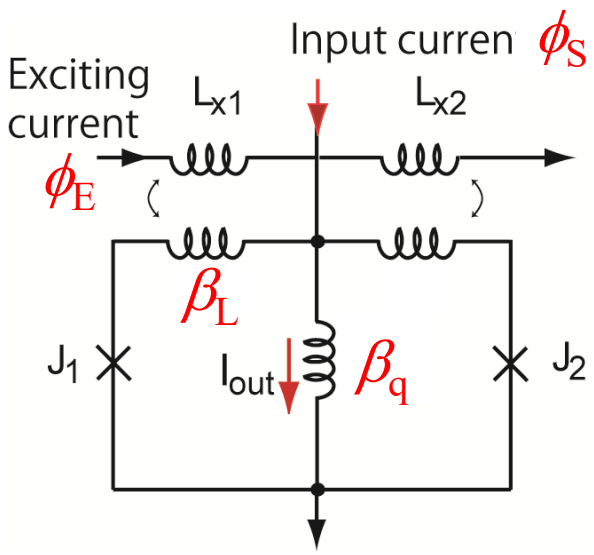
Potential Energy of QFP



$$U_{qfp} = E_j \left[\frac{(\phi_E - \phi_-)^2}{\beta_L} + \frac{(\phi_S - \phi_+)^2}{\beta_L + 2\beta_q} - 2\cos\phi_- \cos\phi_+ \right]$$

Normalized exciting current $\phi_E = 2\pi \frac{M_1 I_E}{\Phi_0}$,

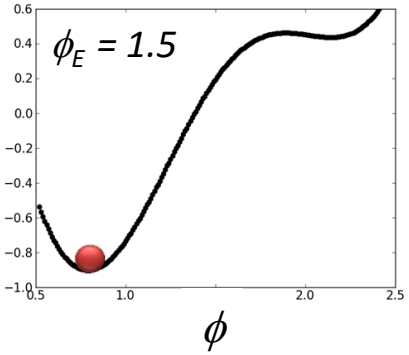
Normalized input current $\phi_S = 2\pi \frac{L_q I_S}{\Phi_0}$

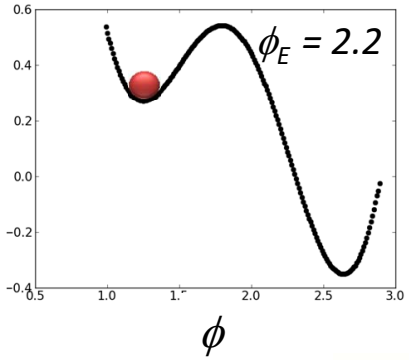
Normalized loop inductance $\beta_L = 2\pi \frac{L_1 I_0}{\Phi_0}$,

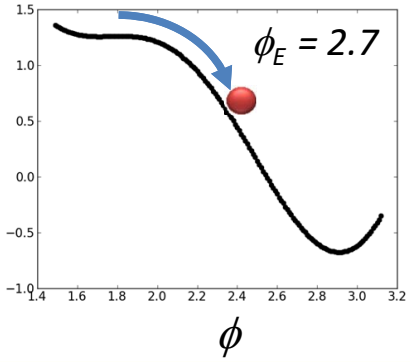
Normalized output inductance $\beta_q = 2\pi \frac{L_q I_0}{\Phi_0}$

$$E_j = \frac{E_J}{2\pi} = \frac{I_0 \Phi_0}{2\pi}, \quad \phi_+ = \frac{\phi_1 + \phi_2}{2}, \quad \phi_- = \frac{\phi_1 - \phi_2}{2}$$

◆ $(\beta_L, \beta_q) = (1.0, 3.0)$







M. Hosoya et al, *IEEE Trans. Appl. Supercond.* vol. 1, 1991, pp. 77 – 89.

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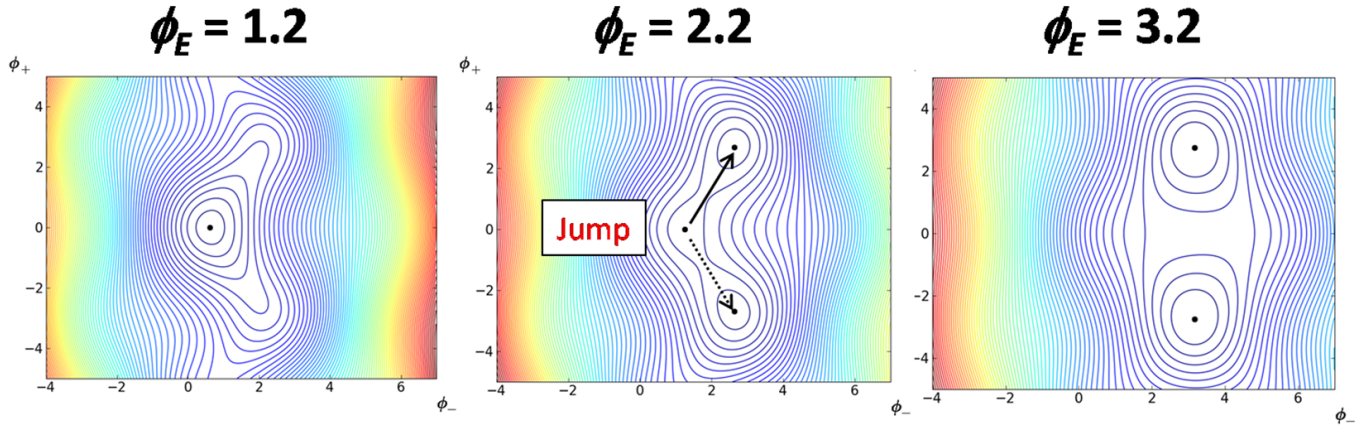
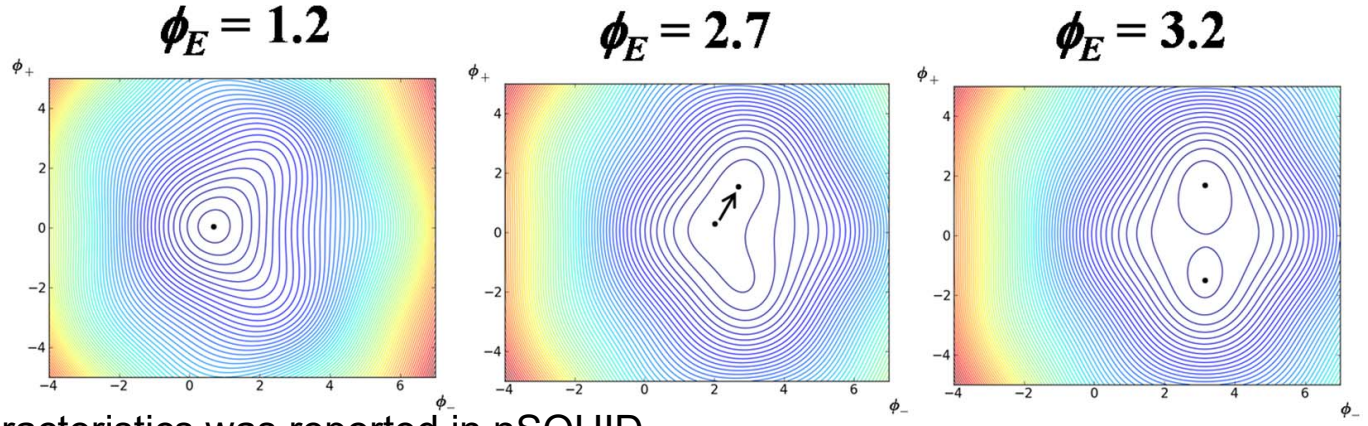
Non-adiabatic and Adiabatic QFP

Non-adiabatic QFP ◆ $(\beta_L , \beta_q) = (1.0, 3.0)$



Adiabatic QFP ◆ $(\beta_L , \beta_q) = (0.8, 0.4)$



Similar characteristics was reported in nSQUID.
V. Semenov *et al*. *IEEE TAS* 13, 938 (2003).

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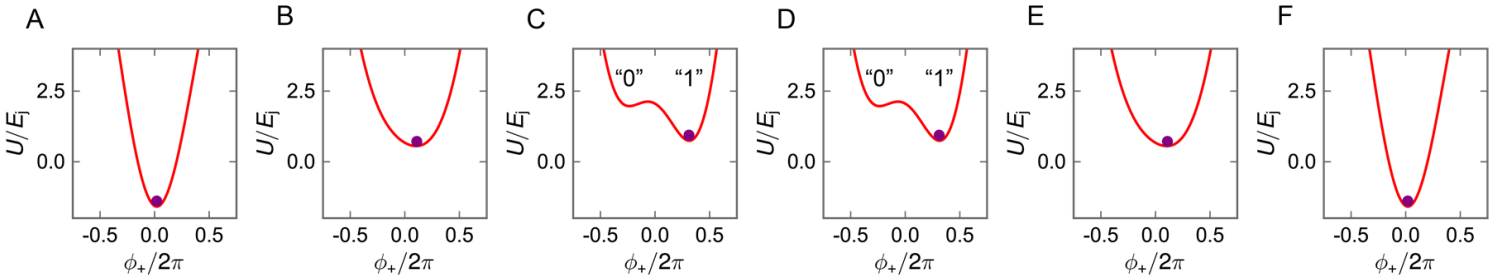
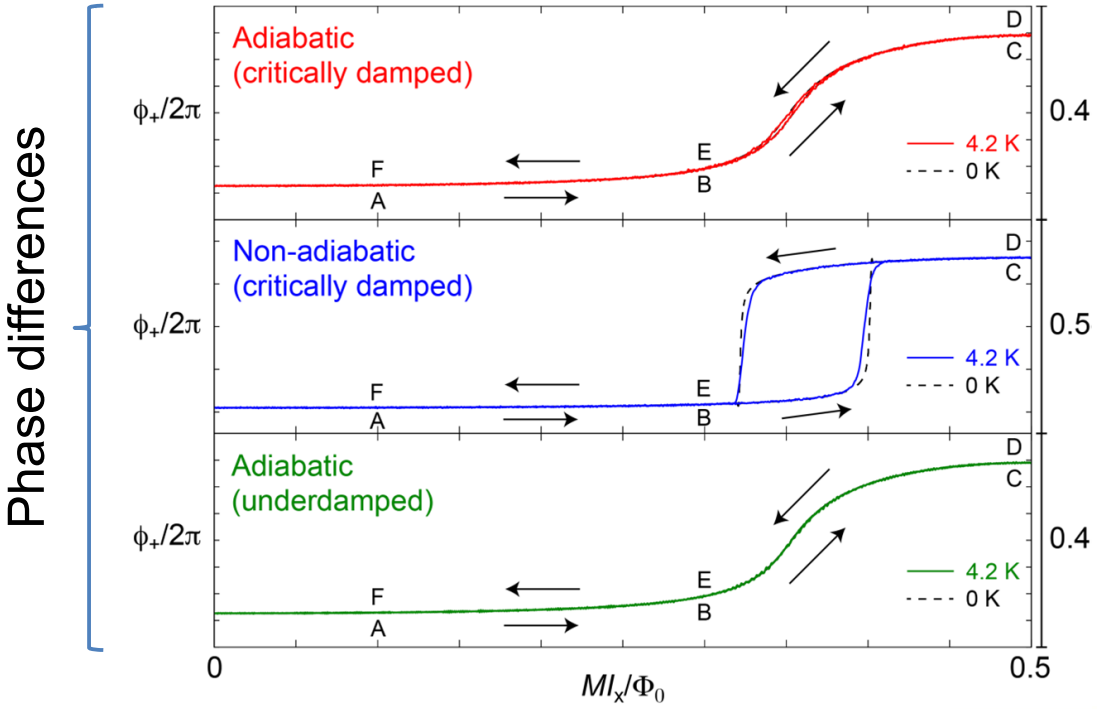
Evolution of Phase Differences at 4.2 K





The phase differences of junctions in AQFP gates change adiabatically even at a finite temperature.

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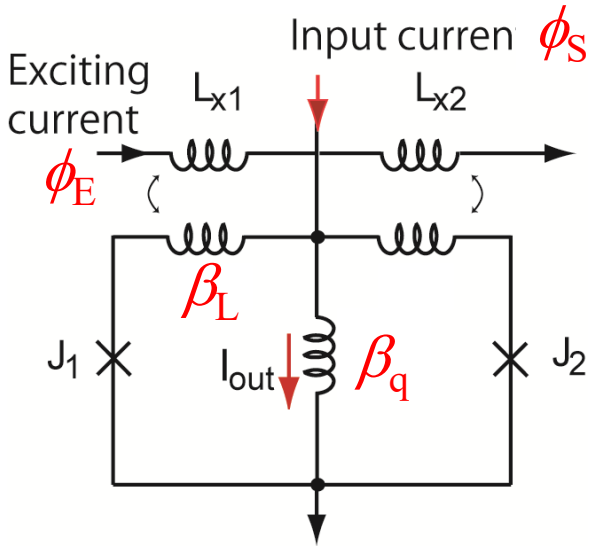
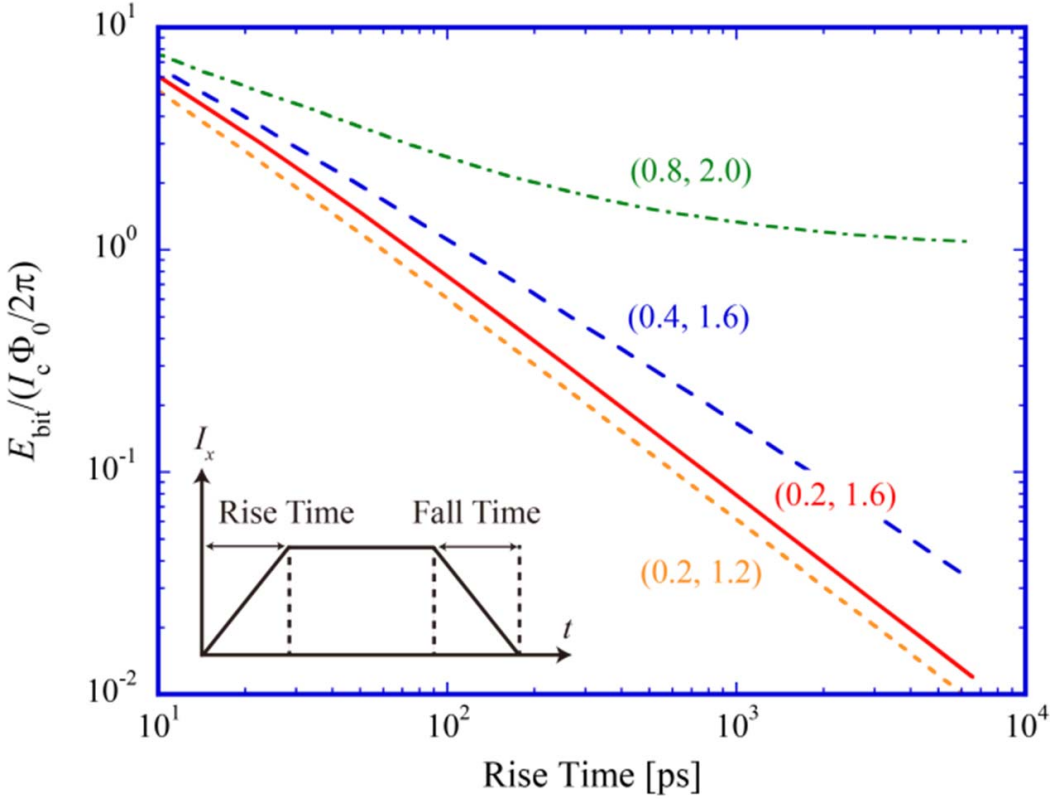
Bit Energy vs. Clock Period of AQFP



Energy dissipation $\propto f$



When rise time is 1000 ps, $E_{bit} = 0.023\ I_c\Phi_0$ ($\sim 20k_BT$).

→ 1/1000 of RSFQ

N. Takeuchi, *et. al.*, *SUST*, 26, 035010 (2013).

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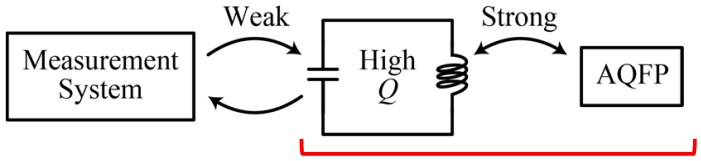
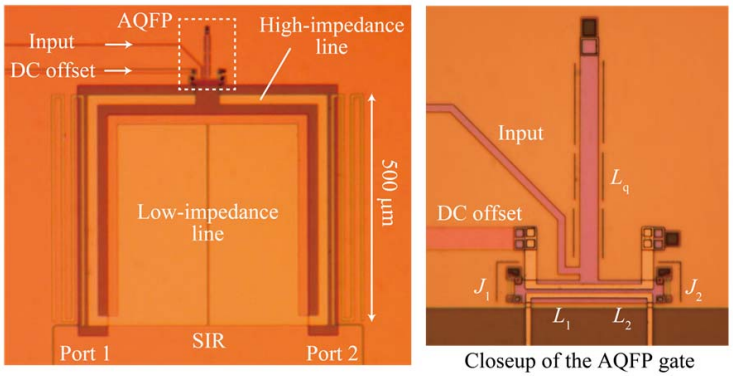
Bit Energy Measurement of AQFP using a Superconducting Resonator





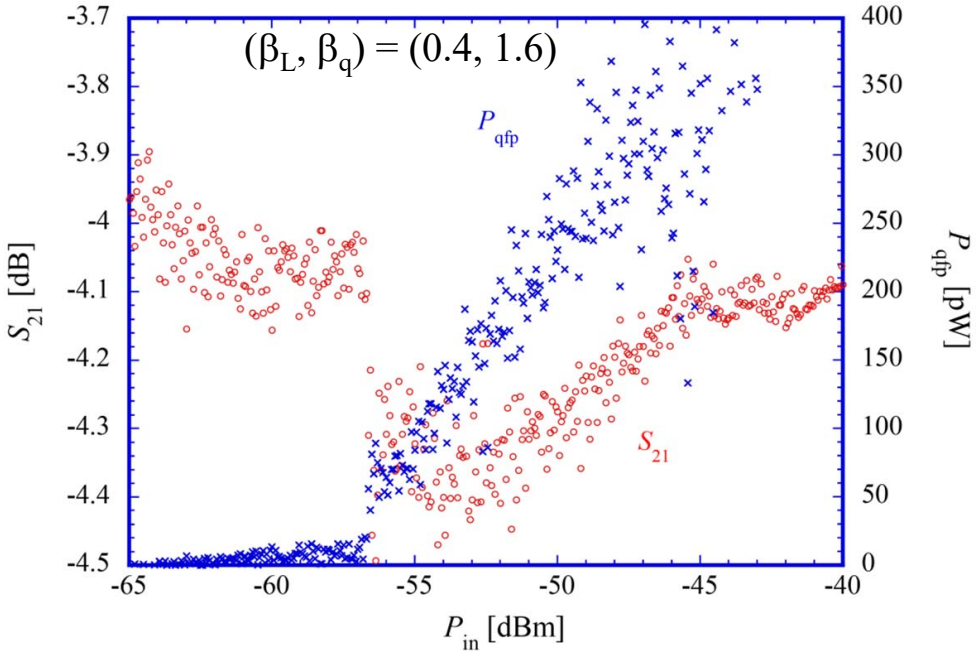
Closeup of the AQFP gate

Clock frequency: 4.998 GHz
Q of resonator : 357

AIST Nb Josephson standard process (STP2) was used.

N. Takeuchi, *et. al.*, *Appl. Phys. Lett.*, 102, 052602 (2013)

Measured power consumption of AQFP



P_{qfp} ~ 50 pW

E_{bit} ~ 10 zJ ~ 170k_BT

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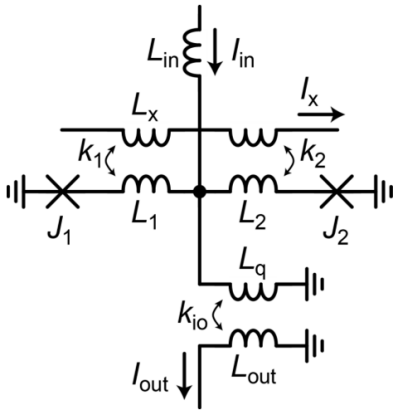
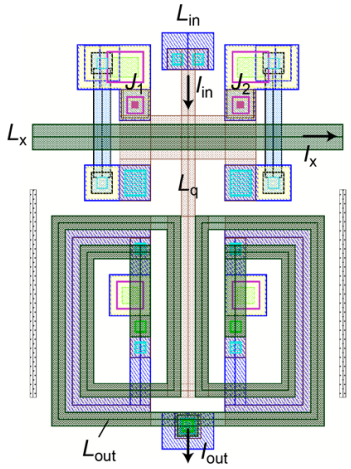
AQFP Logic Family

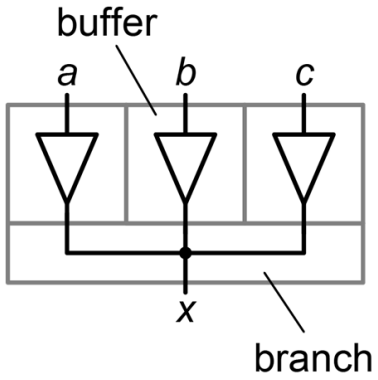
AQFP buffer



Layout of AQFP buffer

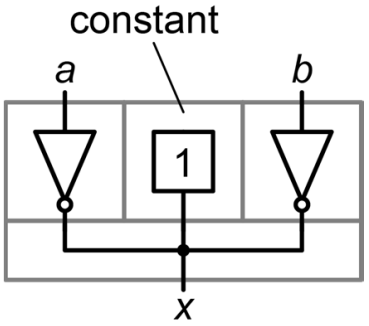


Majority gate



$x = \mathrm{MAJ}(a, b, c)$
$= ab+bc+ca$

NAND gate



$x = \mathrm{MAJ}(\bar{a}, 1, \bar{b})$
$= \overline{ab}$

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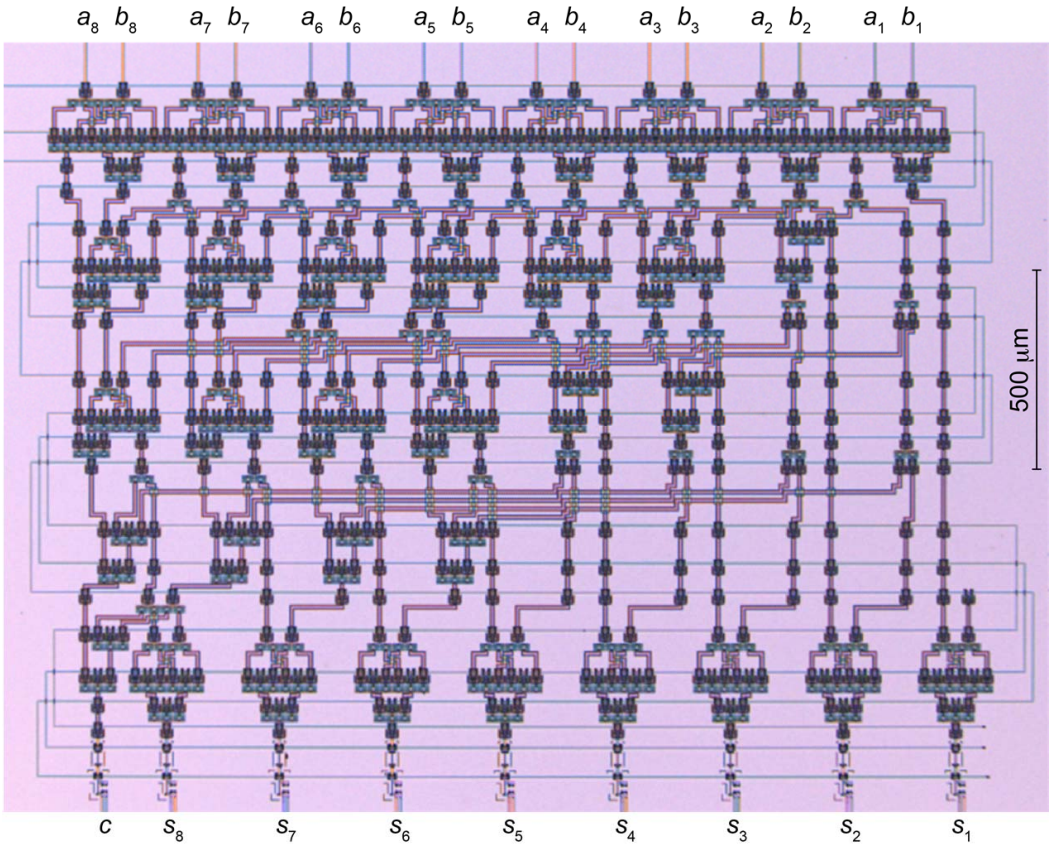
Demonstration of AQFP 8-bit Carry-Look-Ahead Adder

- Energy per operation
  ~ 12 aJ @5GHz
  (cf. Bit energy of a single RSFQ gate: ~10 aJ)
- Designed clock frequency:
  5 GHz
- Junction number:
  1152 ($\beta_c = 5.0$)
- Circuit area: 2.7 x 1.7 mm^2

Microphotograph of 8-bit CLA



The circuits were fabricated using AIST standard process (STP2).

N. Takeuchi *et al.*, *J. Appl. Phys.* **117**, 173912 (2015).

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Comparison of Energy Consumption of CMOS and AQFP

	CMOS	AQFP
Device parameters	Technology: 45 nm Supply voltage: V_{DD} = 1.0 V Frequency: f = 2.85 GHz	Technology: 2 μm (J_c = 2.5 kA/cm^2) Critical current: I_c = 50 μA, Frequency: f = 5 GHz Inductance: $(\beta_L , \beta_q) = (0.4, 1.6)$
Energy/bit	~1 fJ (~10^{-15} J)	10 zJ (~10^{-20} J)

- Energy consumption of AQFP is five orders of magnitude lower than state-of-the-art CMOS devices.
- Further energy reduction is possible by using unshunted junctions.
- Further energy reduction is possible by using high-J_c process.

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Outline

- Background and motivation
- Present status of superconducting computing
  - Japanese and US projects
- The minimum energy in computation?
  - Landauer's principle
  - Adiabatic computing and reversible computing
- Adiabatic quantum flux parametron (AQFP)
- Reversible QFP (RQFP)
- Summary

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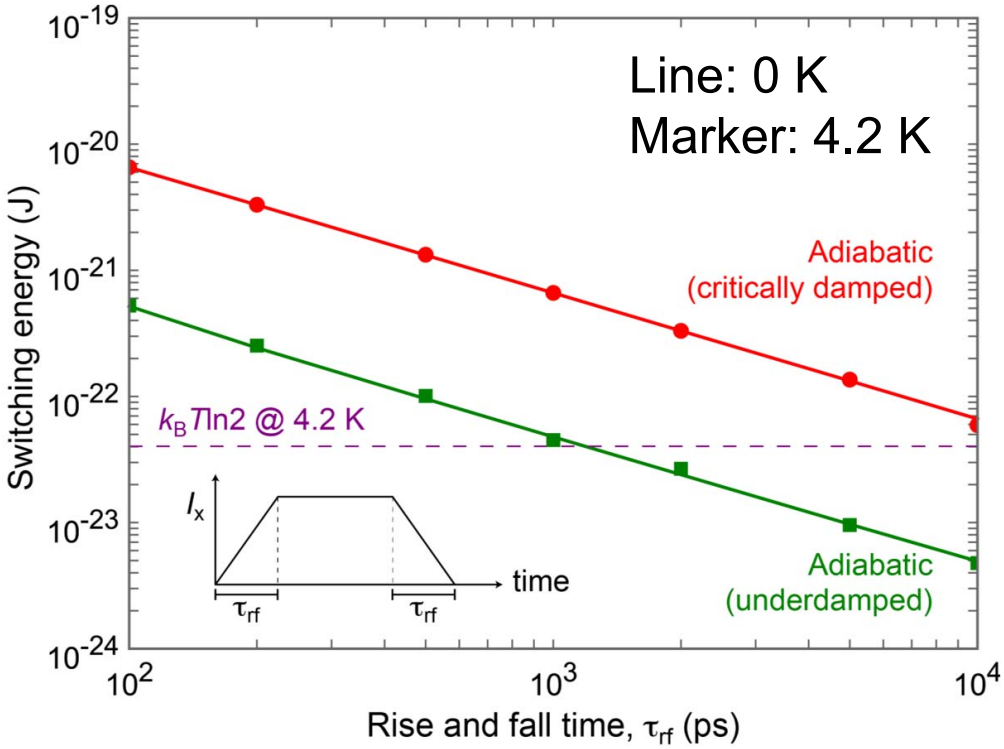
Switching energy of AQFP

Energy dissipation $\propto \frac{f}{Q} \times E_b$

Error rate $\propto \left(-\frac{E_b}{k_B T} \right)$

f, operation frequency
Q, quality factor of junctions
E_b, energy barrier

Switching energy (numerical calc.)



Switching energy can fall below $k_B T$
by lowering frequencies or increasing *Q*.

N. Takeuchi *et al.*, *Phys. Rev. Appl.* 4, 034007 (2015).

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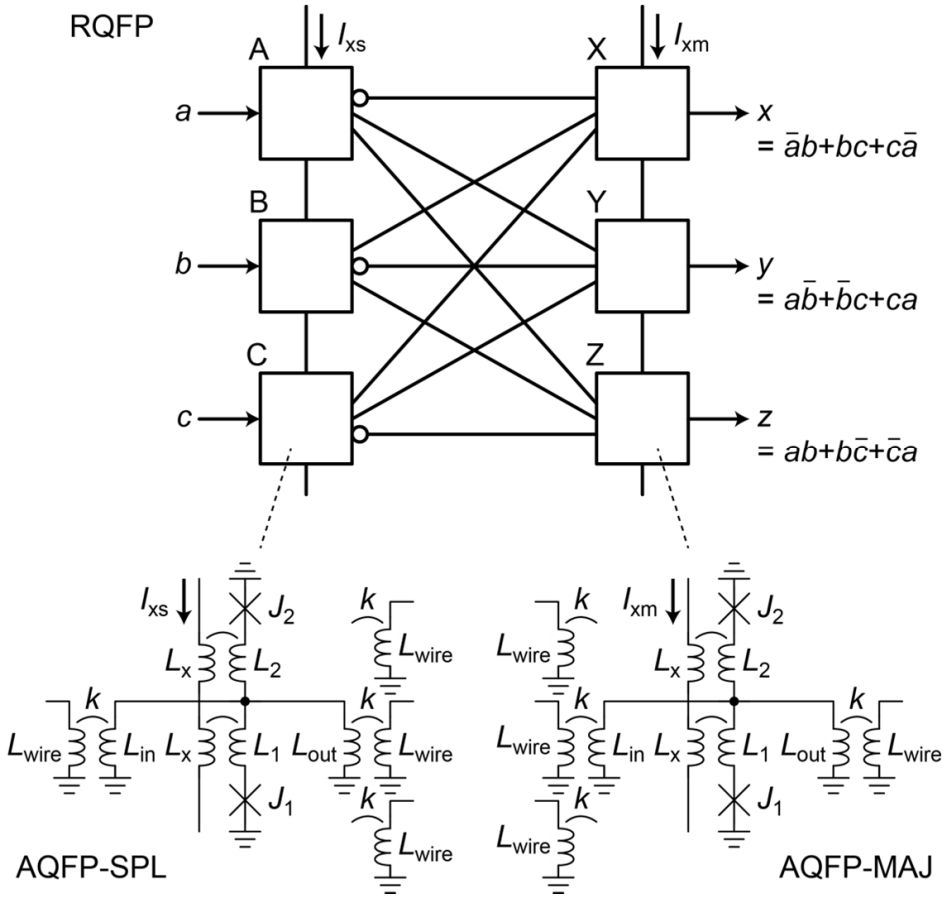
Reversible AQFP (RQFP)

Reversible majority QFP gate



A logically and physically reversible gate can be achieved by using MAJ and SPL gates.

N. Takeuchi, *et. al.*, *Scientific Reports* 4, 6354 (2014).

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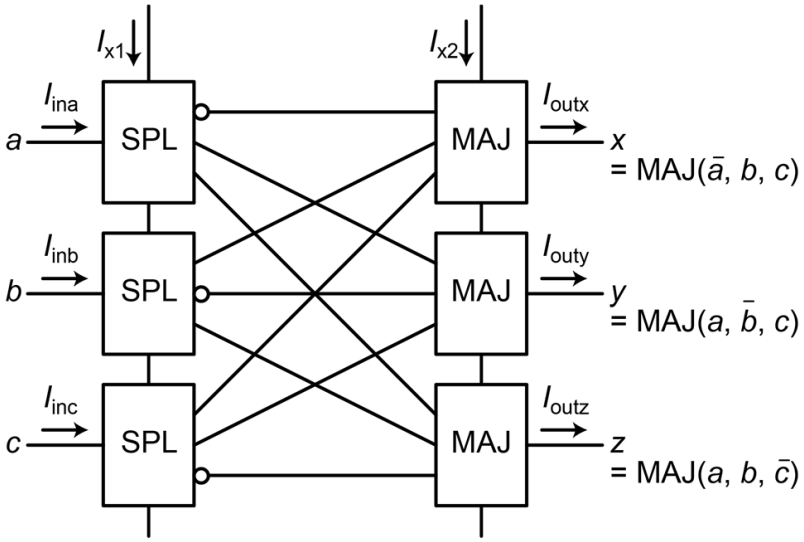
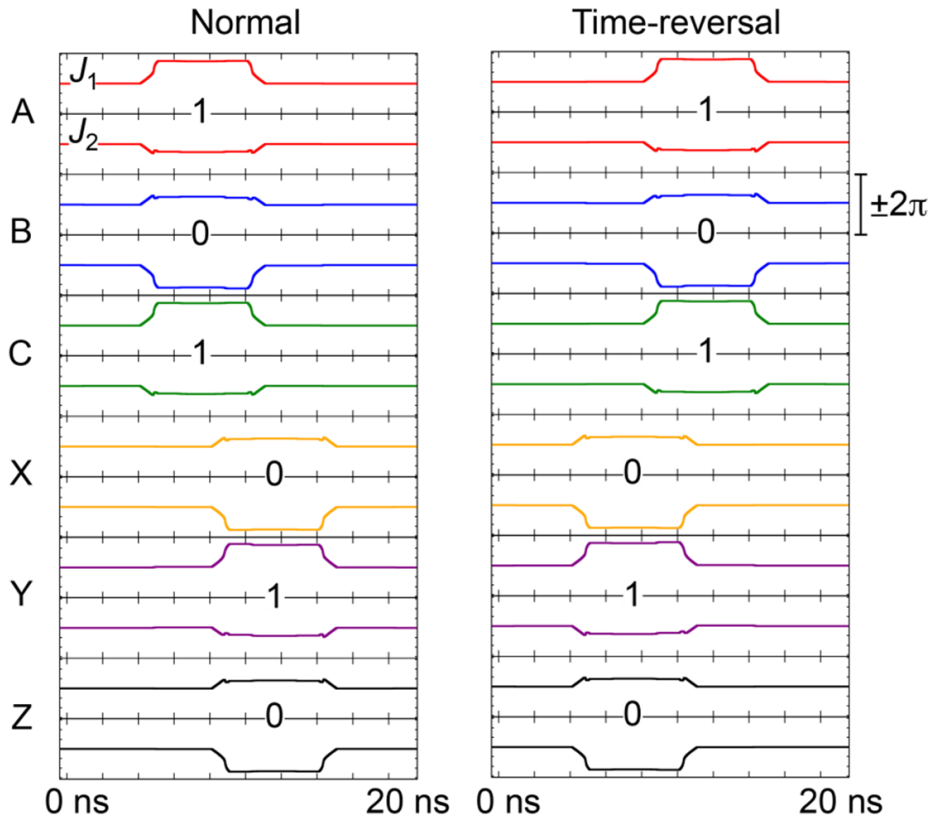
Physical Reversibility of RQFP

Reversible majority QFP gate





Complete time reversibility is satisfied in input/output waveforms.

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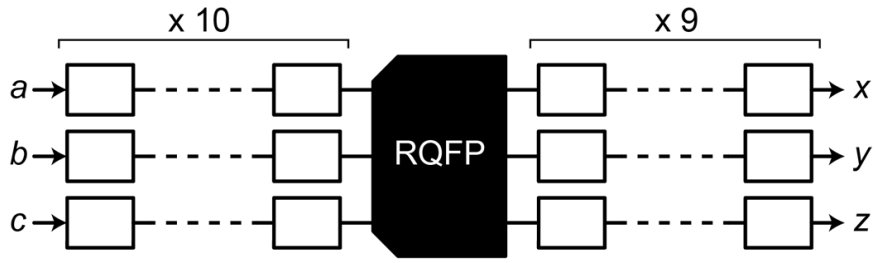
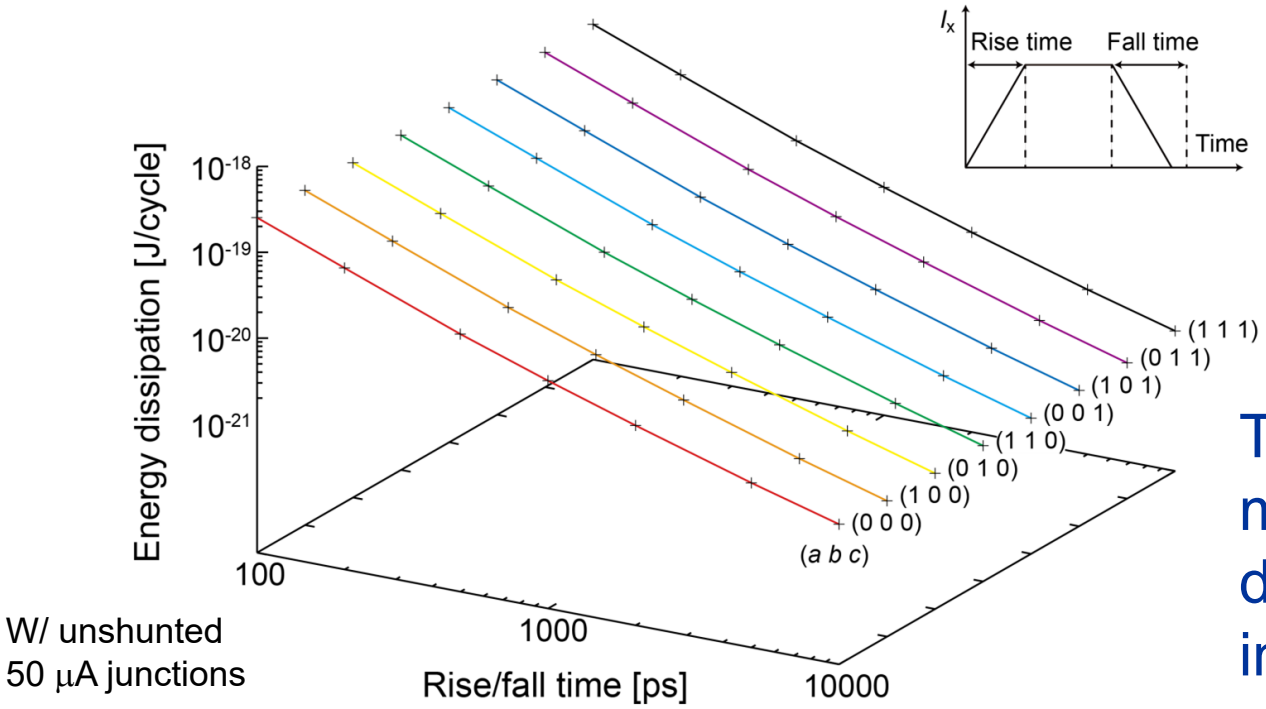
Energy Dissipation of RQFP Gate





W/ unshunted
50 μA junctions

There is no minimum energy dissipation in RQFP.

N. Takeuchi, *et. al.*, *Scientific Reports* 4, 6354 (2014).

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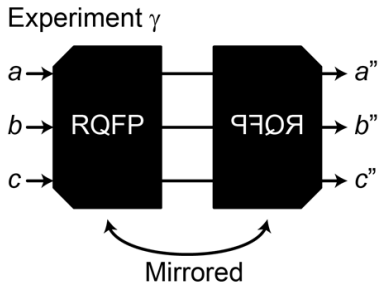
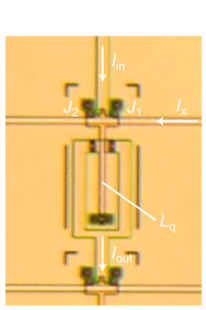
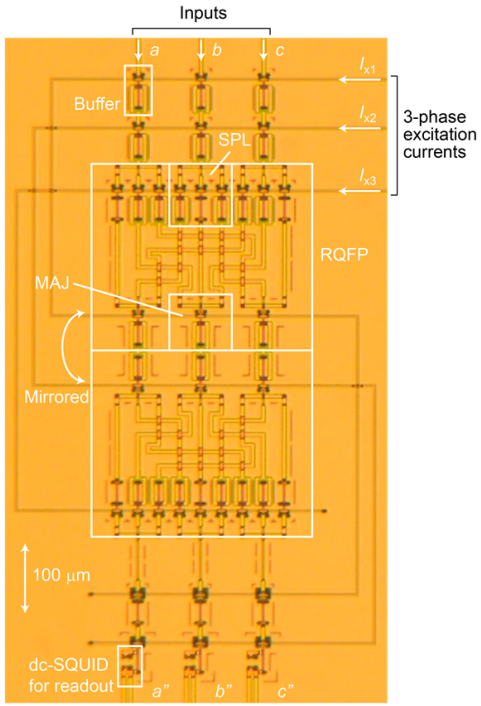
Demonstration of Physical Reversibility

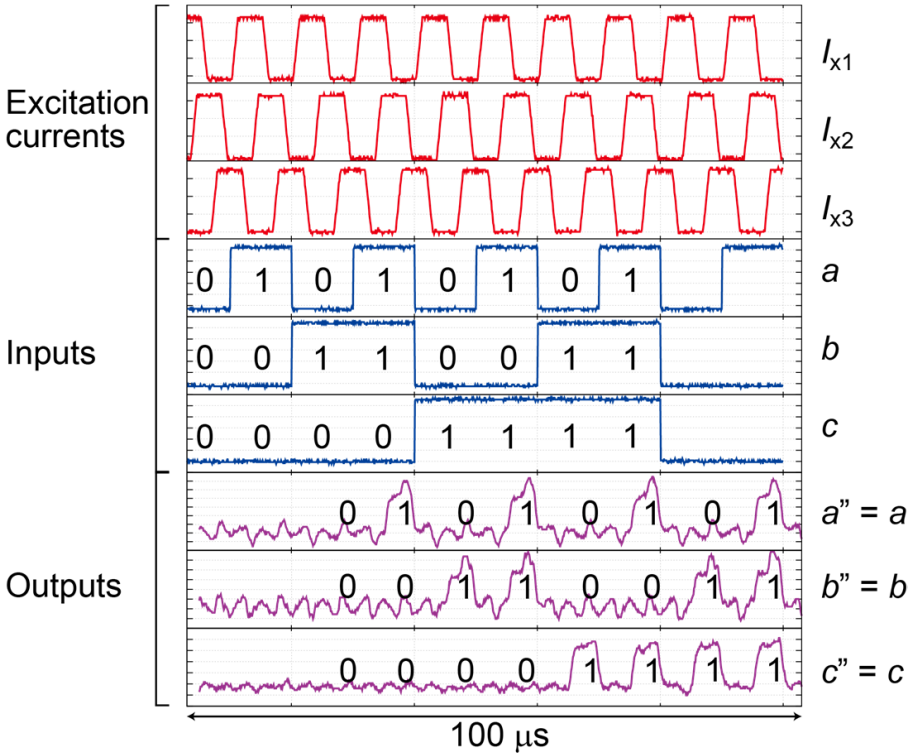
2 RQFP gates are serially connected, one of which is physically mirrored.







Measurement results @ 100 kHz



Physical reversibility is successfully demonstrated.

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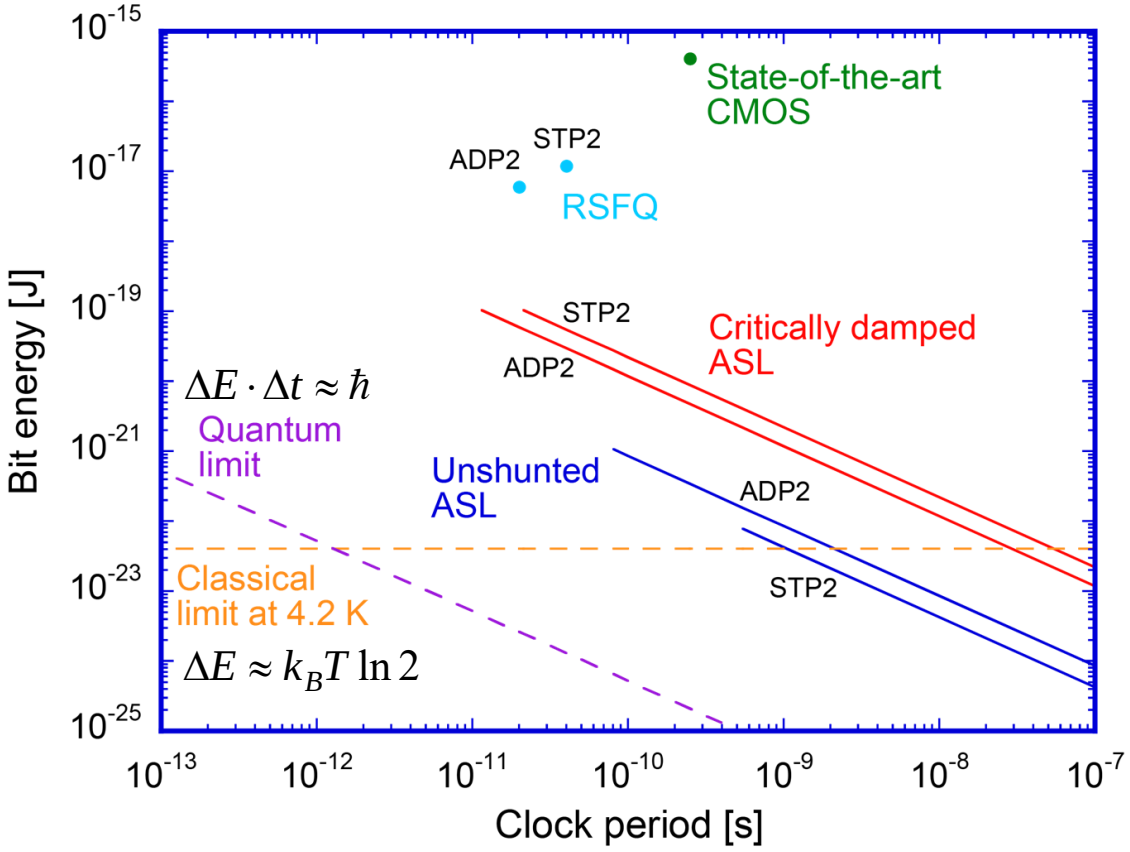
Energy-Delay Products of Superconducting Logic



Energy-delay products of AQFP

$$EDP = \frac{32\pi}{1.76}\frac{E_j}{k_B T_c}\frac{\hbar}{2}$$

Cross over temperature at which the quantum noise equals to the thermal nose

$$T_{cross} = \frac{1.76}{32\pi \ln 2}\frac{R_{sg}}{R_n}T_c$$
$$= 0.3T_c$$

for Nb junctions

N. Takeuchi *et al.*, *SUST*, 28, 2015, 015003.

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Summary

- Current research activities in Japan and US were reviewed.
- Adiabatic quantum flux parametron (AQFP) is extremely energy efficient logic.
  - ~10 zJ/bit @5 GHz
  - Three orders of magnitude smaller than energy-efficient SFQ logic
  - Six orders of magnitude smaller than CMOS logic
- Sub-$k_B T$ bit-energy operation is possible using AQFP gate with high-Q junctions.
  - ~10 yJ/bit (~ 0.2 $k_B T$) @100 MHz
- Reversible logic can be realized based on AQFP.

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Conclusions

- The superconducting logic is only the technology that breaks through the thermal limit in computation.
- We still have a lot of possibilities for improving the energy efficiency in computation using superconducting circuits.

My Special Thanks to

- Dr. O. Mukhanov, Dr. Q Herr, Prof. A Fujimaki, Prof. M. Tanaka

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