IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), September 2019.
Distinguished presentation 3-DI-D-1 given at ISEC, 28 July-1 August 2019, Riverside, USA.

Single Flux Quantum Logic for Digital Applications

Oleg A. Mukhanov

SeeQC, Inc. *(spinout from Hypres)*
Elmsford NY 10523, USA

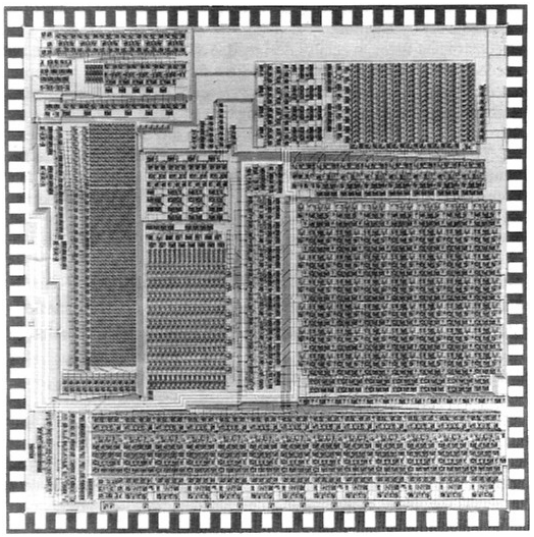
seeqc

Acknowledgments

Thank you for valuable discussions.

- D. Bedard, A. Braginsky, P. Bunyk, J. Clarke, L. DiCarlo, V. Dotsenko, O.Chernyashevskiy, S.Hasuo, T. Filippov, A. Fujimaki, C. Hamilton, A. Herr, S.Holmes, M. Hutchings, A. Jafari Salim, M.Johnson, A. Kirichenko, D.Kirichenko, A. Kadin, N. Katam, M.Ketchen, J.Levy, K. Likharev, M.Manheimer, R.McDermott, A. Miano, I.Nevirkovets, G. Pepe, B.Plourde, S.Polonsky, Yu.Polyakov, J. Przybysz, T.Ortlepp, M. Renzullo, H.Rogalla, V.Ryazanov, S.Rylov, A. Rylyakov, V.Semenov, A. Silver, F. Tafuri, S.Tolpygo, E. Track, P.Truitt, T.Van Duzer, M.Vavilov, I. Vernik, J. Vivalda, M.Volkmann, J.Walter, N.Welker, S. Whiteley, F. Wilhelm-Mauch, D. Yohannes, N.Yoshikawa

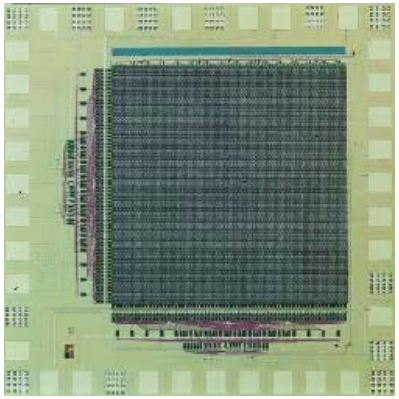
Nb-based Digital and Memory Integrated Circuits



Fujitsu 8-bit Digital Signal Processor (DSP), 5x5 mm^2

Under national project "Scientific Computing System" Fujitsu, Hitachi, NEC, ETL (now AIST) worked on Josephson computing technologies (1981-1990)

The world's first Josephson microprocessor was installed in a cryostat, which was connected to a refrigerator and operated in a closed cycle.



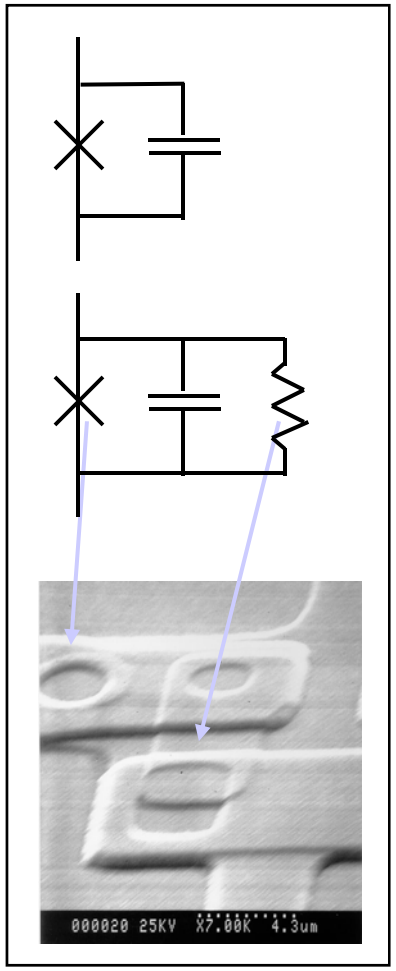
NEC 4-kb RAM, 4.5x4.5 mm^2

- **ac-powered, voltage-state latching logic**
- Nb trilayer process
- **A 770 MHz 4-bit microprocessor (compare to silicon-based AMD's AM2901 with 30 MHz clock)**
- Work (especially on RAM) continued in 90s

S. Hasuo, "Digital Electronics in Japan," in 100 Years of Superconductivity, chapter 7.3, eds. H. Rogalla, P. Kes, Taylor & Francis, 2011.

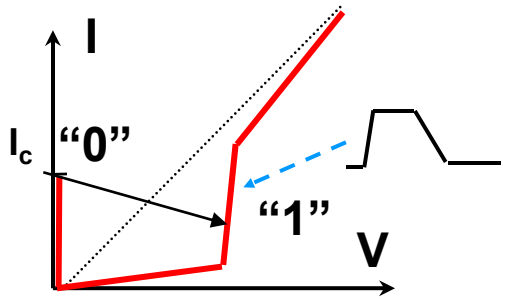
Active Device: Josephson Junction (JJ)

Picosecond waveforms and time responses



70-90's

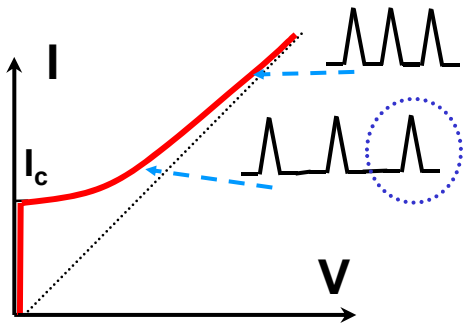
Latching logic



Voltage pulses
(picosecond front, nanosecond tail)

Since mid-80s

RSFQ Logic



SFQ pulses with quantized areas
(picosecond front and tail)

$$\int V dt = \Phi_0$$

Adding a shunt resistor allows the generation of separate SFQ pulses

RSFQ Technology

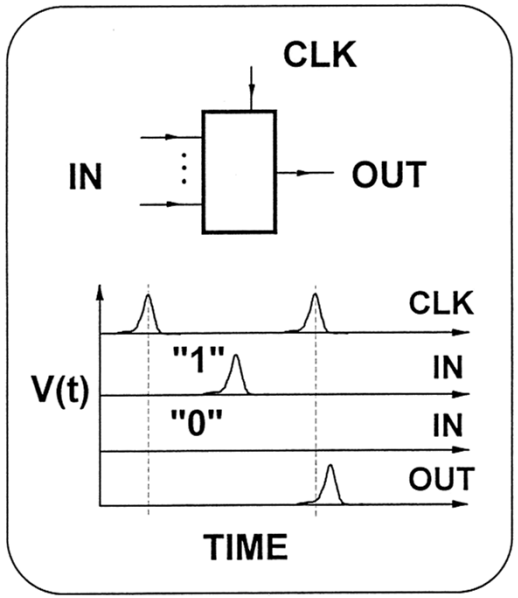
RSFQ - Rapid Single Flux Quantum

Timeline:

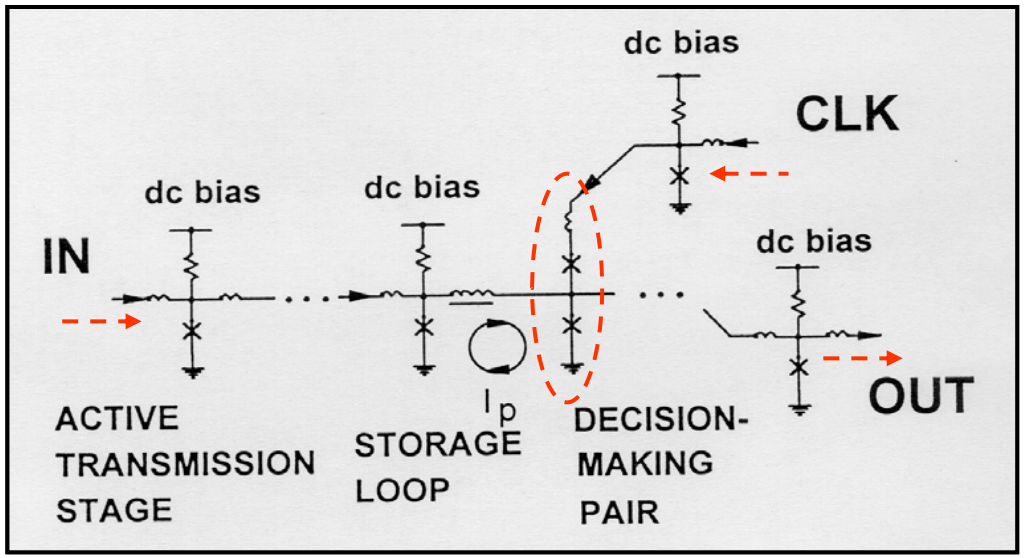
invented in 85-86, generally accepted in 90, adopted in the US in 91, became the main digital superconducting electronics by mid-end of 90s, first product by mid-00s

$$\int V dt = \Phi_0 = h/2e = 2.07\ mV \cdot ps$$

$E_{SFQ} = 10^{-19} J$



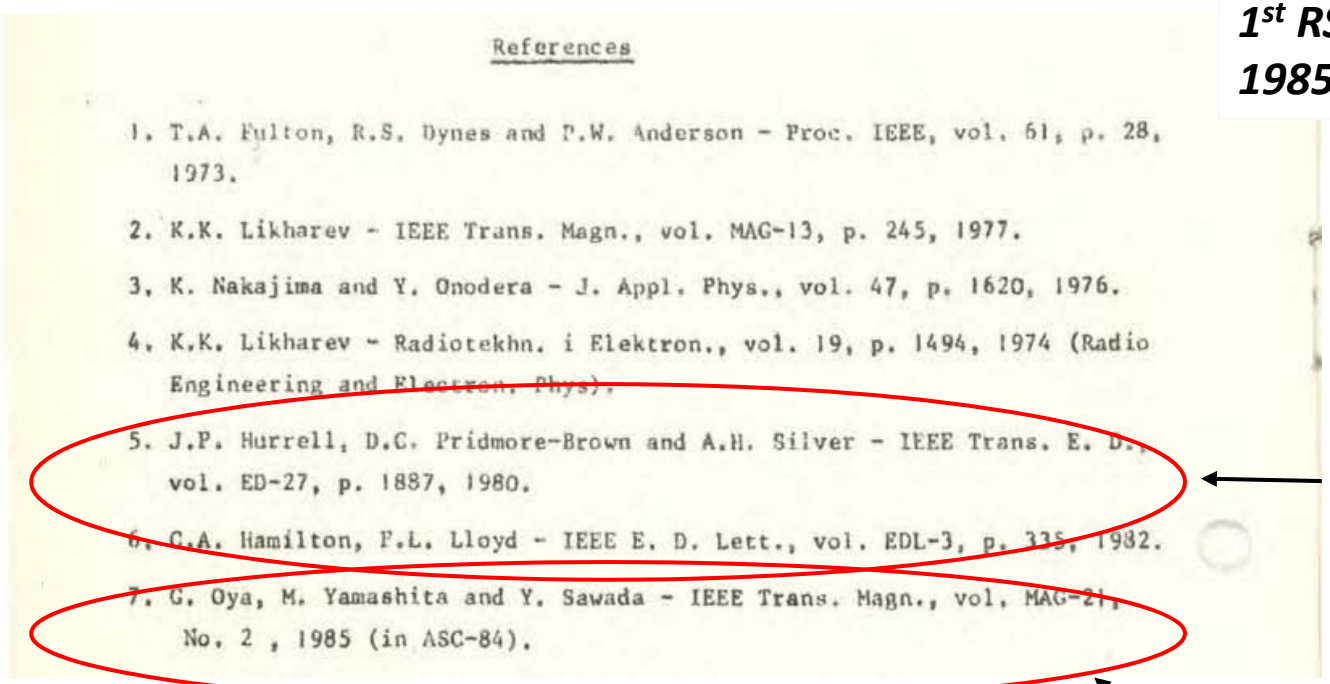
Both Data and Clock are SFQ voltage pulses V(t) with quantized areas



- 750 GHz digital frequency divider demonstrated
- internal memory
- gate-level pipelining
- high-throughput
- low switching power
- dc bias only
- local timing
- amendable for synchronous and asynchronous schemes

Inspiration

References from the 1st RSFQ disclosure: 1985 MSU preprint



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1. T.A. Fulton, R.S. Dynes and P.W. Anderson - Proc. IEEE, vol. 61, p. 28, 1973.

2. K.K. Likharev - IEEE Trans. Magn., vol. MAG-13, p. 245, 1977.

3. K. Nakajima and Y. Onodera - J. Appl. Phys., vol. 47, p. 1620, 1976.

4. K.K. Likharev - Radiotekhn. i Elektron., vol. 19, p. 1494, 1974 (Radio Engineering and Electron. Phys).

5. J.P. Hurrell, D.C. Pridmore-Brown and A.H. Silver - IEEE Trans. E. D., vol. ED-27, p. 1887, 1980.

6. C.A. Hamilton, F.L. Lloyd - IEEE E. D. Lett., vol. EDL-3, p. 335, 1982.

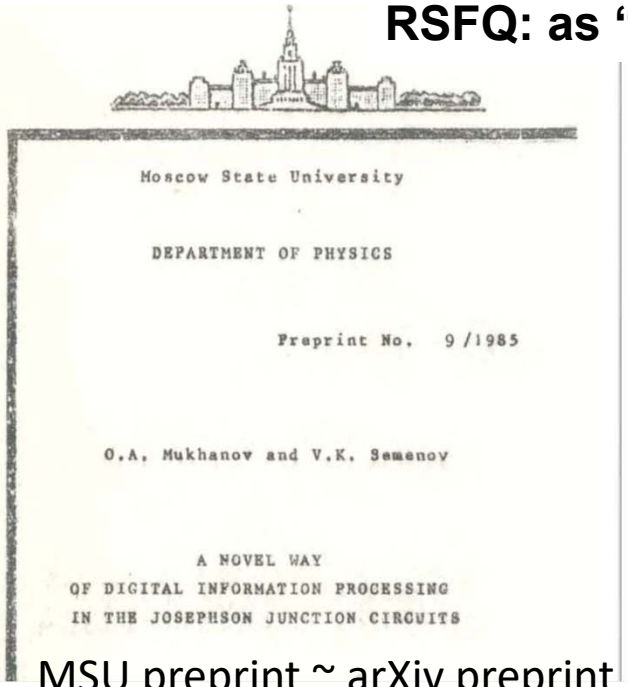
7. G. Oya, M. Yamashita and Y. Sawada - IEEE Trans. Magn., vol. MAG-21, No. 2 , 1985 (in ASC-84).

Asynchronous SFQ binary counters for analog-to-digital converters

Fluxoid-based logic on long JJs based on collisions/annihilation of fluxoids with antifluxoids

RSFQ: first papers

RSFQ: as "ResistiveSFQ"



Moscow State University

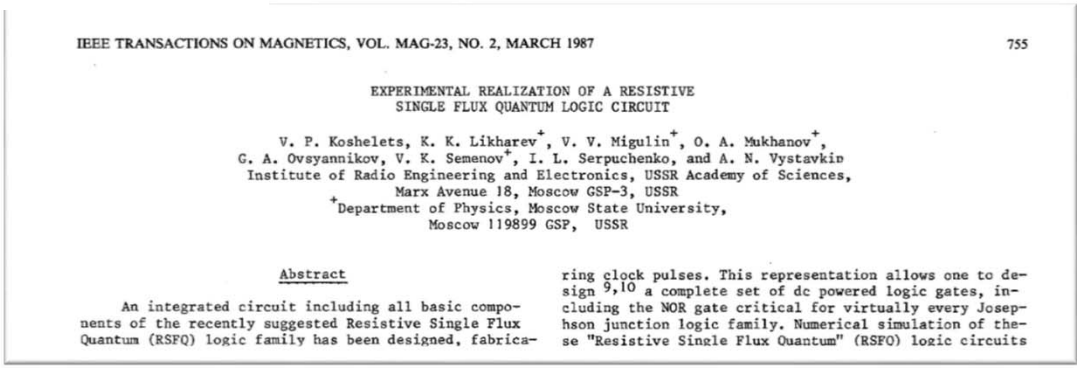
DEPARTMENT OF PHYSICS

Preprint No. 9 /1985

O.A. Mukhanov and V.K. Semenov

A NOVEL WAY
OF DIGITAL INFORMATION PROCESSING
IN THE JOSEPHSON JUNCTION CIRCUITS

MSU preprint ~ arXiv preprint



IEEE TRANSACTIONS ON MAGNETICS, VOL. MAG-23, NO. 2, MARCH 1987 755

EXPERIMENTAL REALIZATION OF A RESISTIVE
SINGLE FLUX QUANTUM LOGIC CIRCUIT

V. P. Koshelets, K. K. Likharev+, V. V. Migulin+, O. A. Mukhanov+,
G. A. Ovsyannikov, V. K. Semenov+, I. L. Serpuchenko, and A. N. Vystavkin
Institute of Radio Engineering and Electronics, USSR Academy of Sciences,
Marx Avenue 18, Moscow GSP-3, USSR
+Department of Physics, Moscow State University,
Moscow 119899 GSP, USSR

Abstract

An integrated circuit including all basic components of the recently suggested Resistive Single Flux Quantum (RSFQ) logic family has been designed, fabricating clock pulses. This representation allows one to design [9,10] a complete set of dc powered logic gates, including the NOR gate critical for virtually every Josephson junction logic family. Numerical simulation of these "Resistive Single Flux Quantum" (RSFQ) logic circuits

1st experimental RSFQ IC:30 GHz clock

Universal set of RSFQ gates: ~25 Jan. 1985, |Rm.1.61a>+|dorm rm> v2

Reprint from
SQUID '85 - Superconducting Quantum Interference Devices and their Applications
Editors: H. D. Hahlbohm, H. Lübbig
© 1985 Walter de Gruyter & Co, Berlin · New York - Printed in Germany.

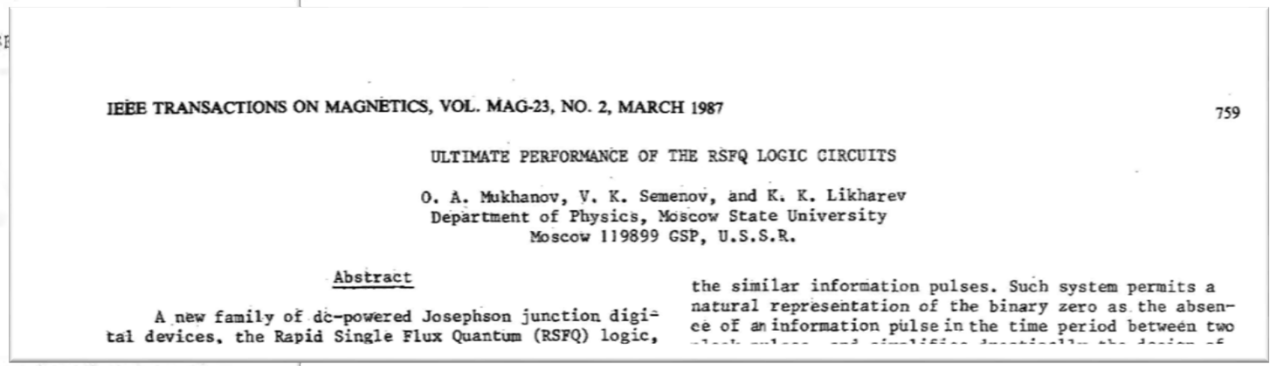
RESISTIVE SINGLE FLUX QUANTUM LOGIC FOR THE JOSE
DIGITAL TECHNOLOGY

K.K. Likharev, O.A. Mukhanov and V.K. Semenov
Department of Physics, Moscow State University
Moscow 119899 GSP, U.S.S.R.

Introduction

The Josephson logic systems reported earlier were based on one of

RSFQ: "RapidSFQ"



IEEE TRANSACTIONS ON MAGNETICS, VOL. MAG-23, NO. 2, MARCH 1987 759

ULTIMATE PERFORMANCE OF THE RSFQ LOGIC CIRCUITS

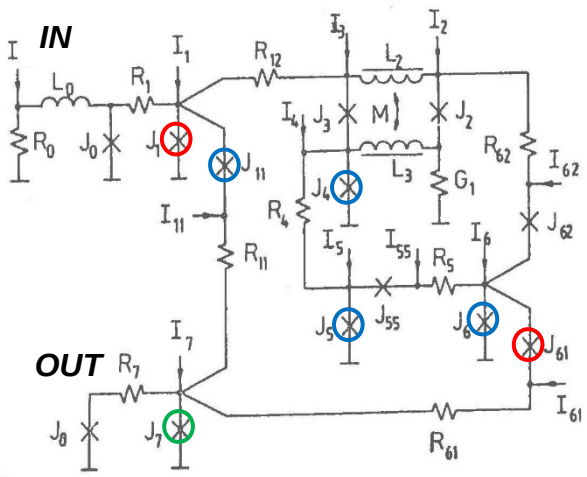
O. A. Mukhanov, V. K. Semenov, and K. K. Likharev
Department of Physics, Moscow State University
Moscow 119899 GSP, U.S.S.R.

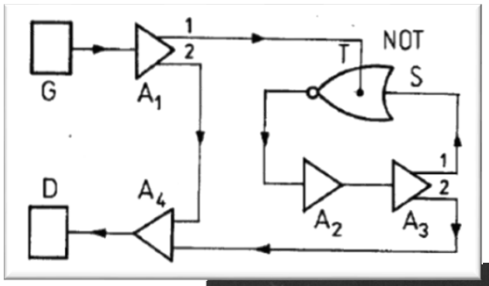
Abstract

A new family of dc-powered Josephson junction digital devices, the Rapid Single Flux Quantum (RSFQ) logic,

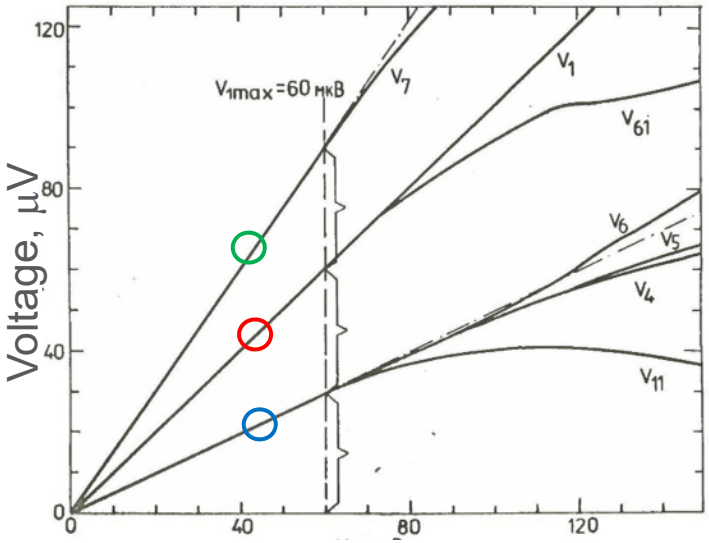
the similar information pulses. Such system permits a natural representation of the binary zero as the absence of an information pulse in the time period between two

RSFQ Logic: First Demonstration (1986)

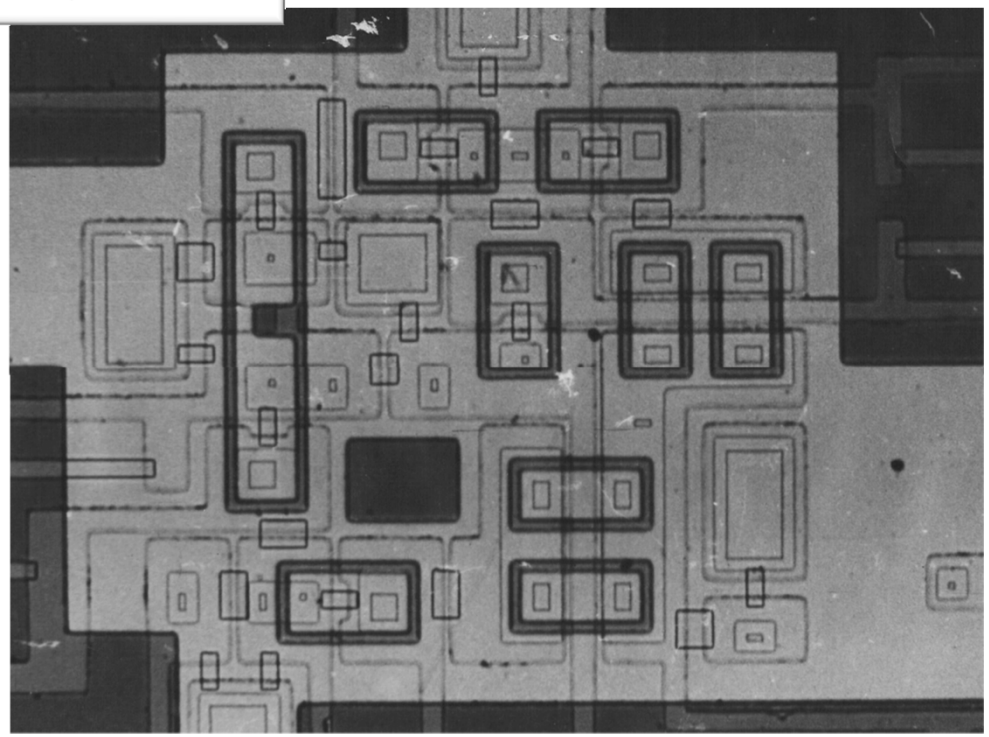




NOT is the principle gate in any universal logic set

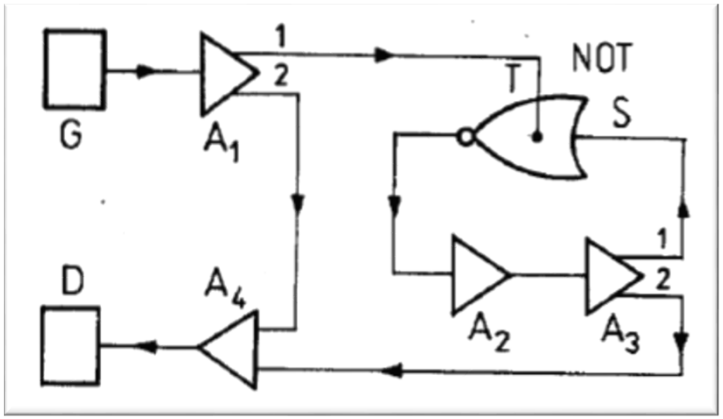


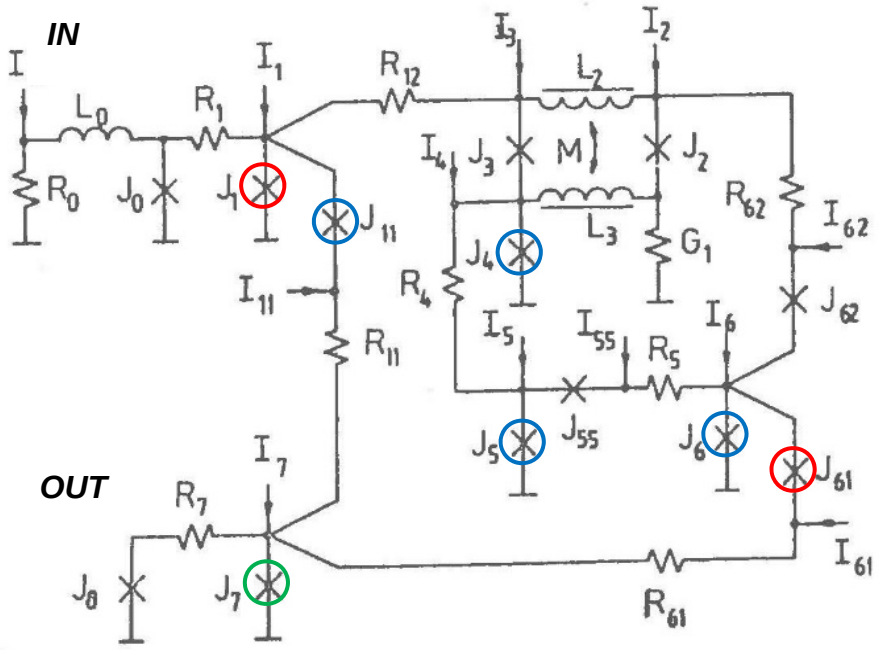
Continuous operation **from 0 to 30 GHz**



10 μm Inst.RadioEng.&Ele. (IRE) fabrication process, 500 A/cm^2 (Nb-AlOx-Nb JJs: 100, 150, 200 μm^2)

RSFQ Logic: First Design Tools



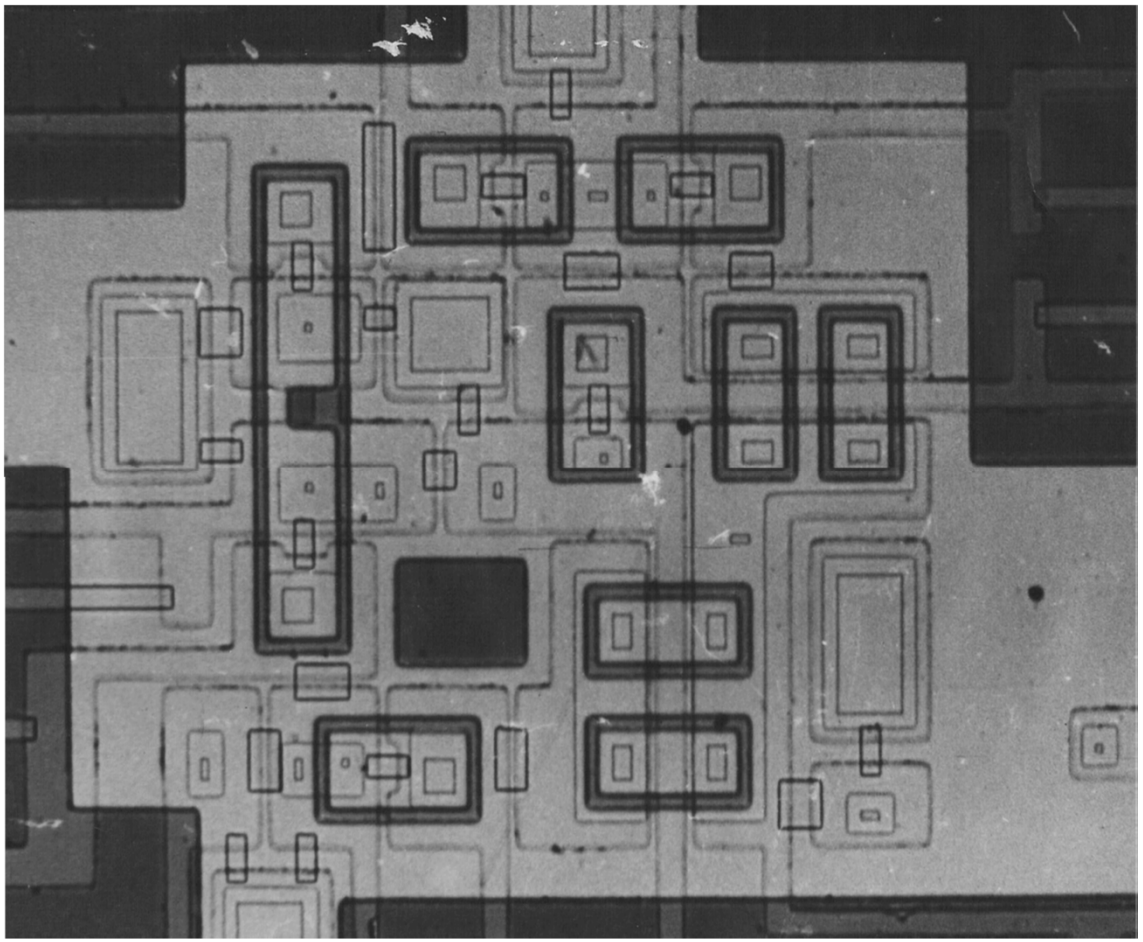


Design of the first RSFQ cells were developed using circuit simulator **COMPASS:**

- COMPASS was developed by V. Semenov and Zavaleev
- COMPASS description was submitted to IEEE Trans. Magnetics, but the manuscript was rejected.
- Run on БЭСМ-6 (BESM-6) mainframe
- With advent of desktop PCs, it was replaced by PSCAN

V. P. Koshelets *et al.*, "Experimental realization of a Resistive Single Flux Quantum logic circuit," *IEEE Trans. Magn.*, vol. 23, pp. 755-758, 1987

RSFQ Logic: First Design Tools



10 μm Inst.RadioEng.&Electronics (IRE) fabrication process, 500 A/cm^2 (Nb-AlOx-Nb JJs: 100, 150, 200 μm^2)

Layout tool @1985:

- Layout editor: pen, eraser, ruler, on millimeter paper (one sheet of paper per layer)
- Design Rule Checkers (DRC): window pane from dorm room, table light under to align layers (paper sheets)
- Layout extraction: count squares

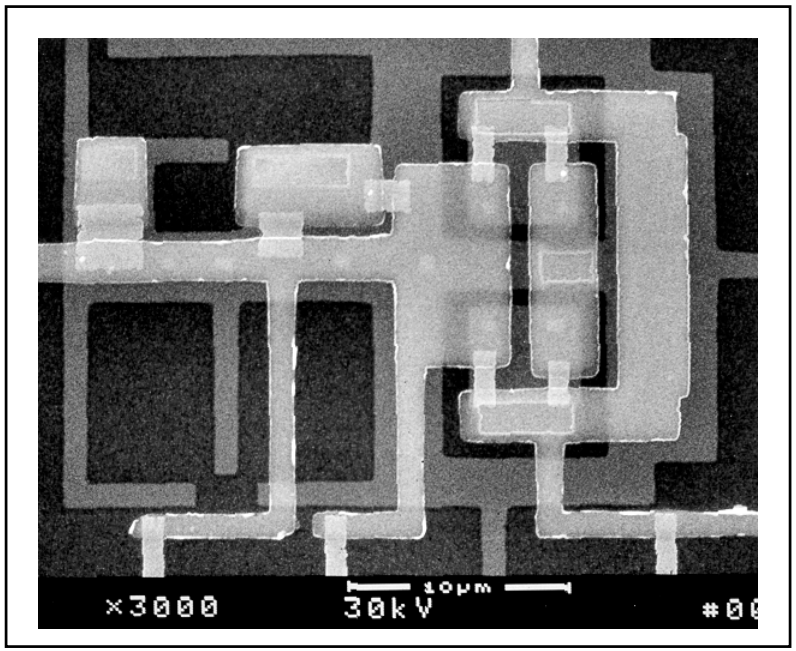
Layout tool @1987:

- AutoCAD
- First RSFQ ADC (1988) was designed using AutoCAD

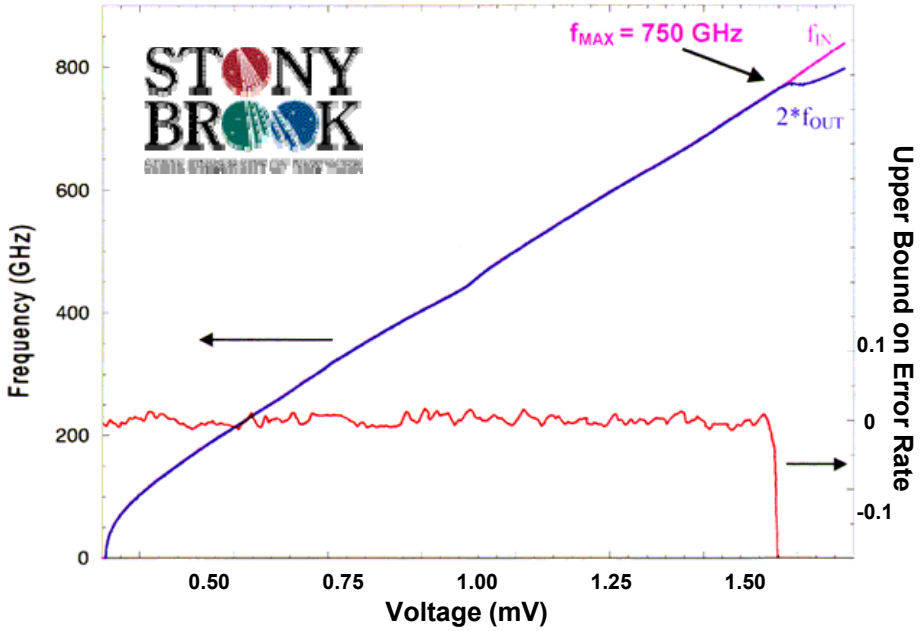
V. P. Koshelets *et al.*, "Experimental realization of a Resistive Single Flux Quantum logic circuit," *IEEE Trans. Magn.*, vol. 23, pp. 755-758, 1987

RSFQ: High Clock Speed

750 Gb/s RSFQ Digital Frequency Divider



0.25-μm Nb Fabrication Process



DFD operation for $f_{OUT} = ½ f_{IN}$

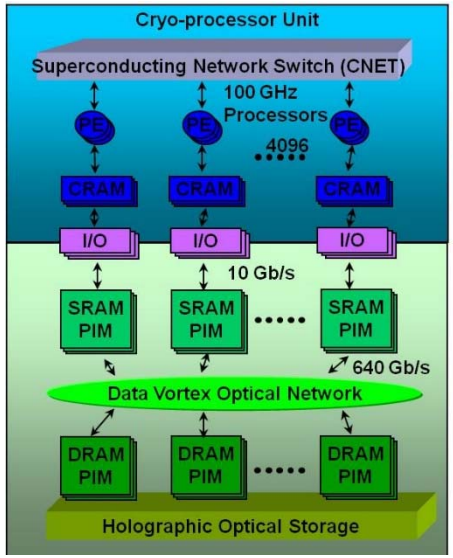
$$V = \Phi_0 \cdot f_J \text{ [bits / second]} \quad \text{- or -} \quad f_J = V \cdot (1/\Phi_0) = V \cdot K_J$$

$$\text{where, } K_J = 483.597898(19) \times 10^6 \text{ Hz/μV [accuracy 0.39 ppb]}$$

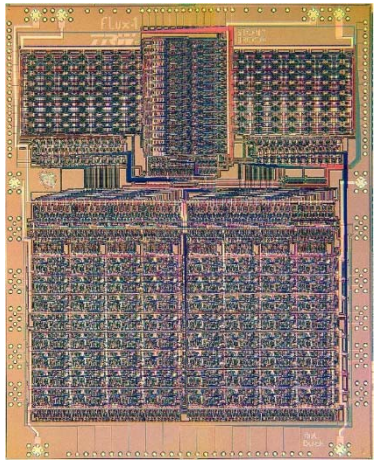
Produced with a 0.25-μm, 140 kA/cm², Nb JJ fabrication process

W. Chen, A. Rylyakov, V. Patel, J. Lukens, K. Likharev, "Superconductor digital frequency divider operating up to 750 GHz," Appl. Phys. Lett., vol. 73, p. 2817, 1998

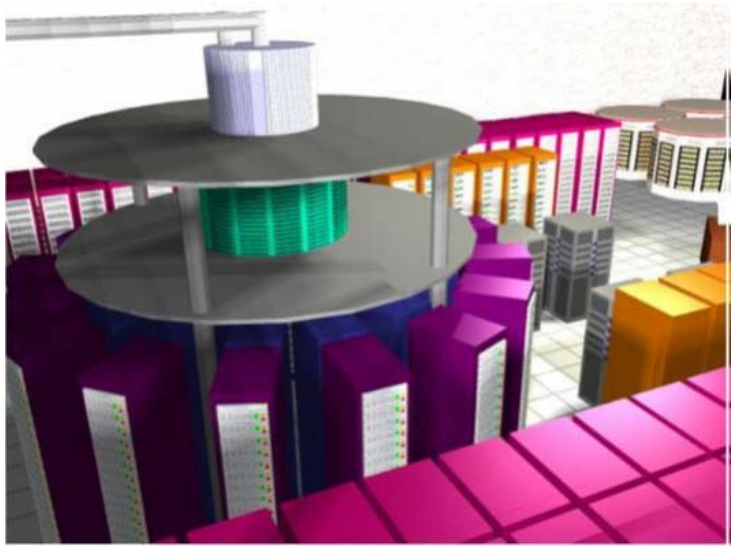
Attempt #1: Hybrid Technology Multi-Threaded (HTMT) Project (RSFQ-based computer)



Multi-threaded architecture.



"FLUX 1"
5000 gate, 8-bit (parallel) RSFQ microprocessor chip fabricated with 1.75 micron 4 kA/cm2 current density Nb-NbAlOx-Nb Josephson junctions at TRW. Projected specs: 9 mW at a 20 GHz clock (did not work).



HTMT facility (conceptual drawing). Cryopackage concept: 1 m3 package, 1 kW 4 K, built with achievable technology

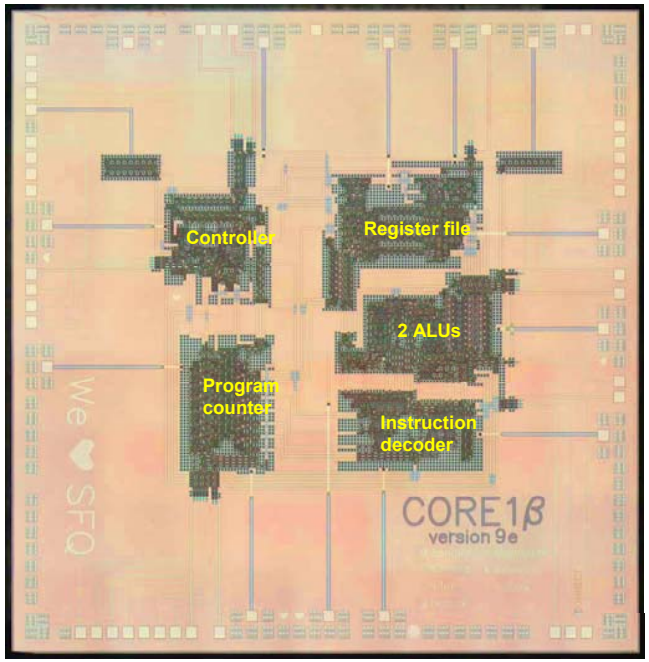
The 1st computing project for RSFQ: HTMT (Hybrid Technology Multi Threaded architecture), since multiple technologies were employed

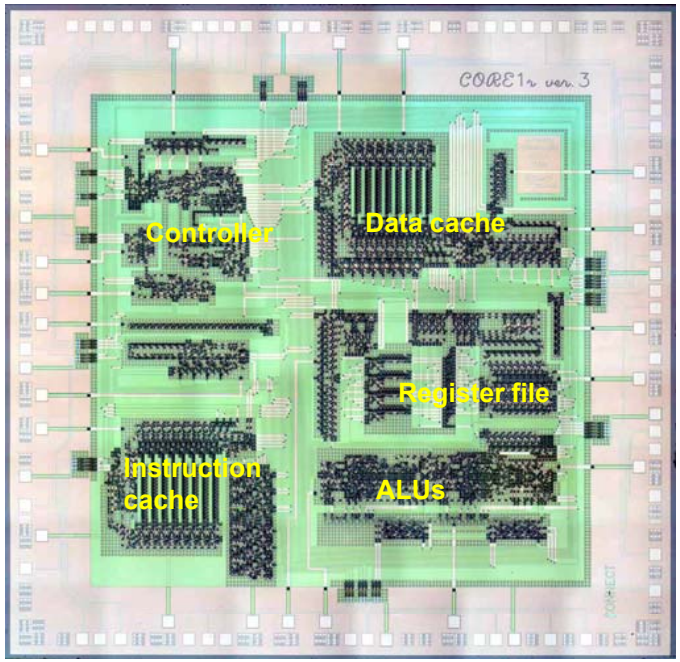
Supported by NSA and NASA (JPL/CalTech). **Goal:** building a prototype petaFLOPS computing system. Phase 1: ~1998-2000

The participants:

State University of New York (SUNY) at Stony Brook (RSFQ design), Hypres (CRAM study and fabrication of SUNY chips), TRW (design and fab),
Columbia University, University of Notre Dame, University of Delaware,
Argonne National Laboratory, California Institute of Technology, and Jet Propulsion Laboratory (JPL)

RSFQ Microprocessors in Japan





Kyoto Univ.
Nagoya Univ.

CORE 1β

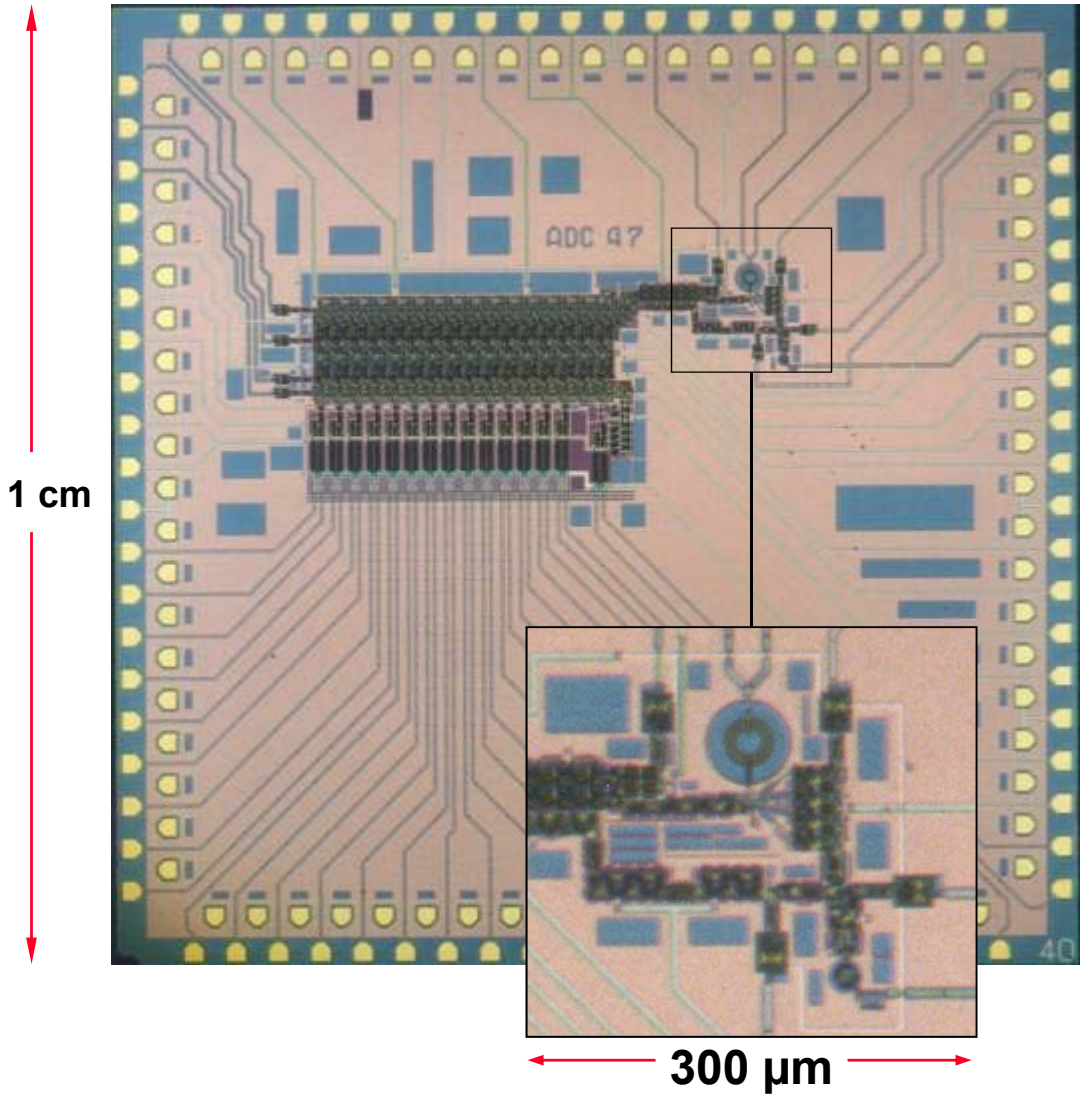
- 8 bit, bit-serial
- 1400 MOPS at peak
- **25 GHz bit-operation**
- 4-stage pipelining
- 10,995 JJs
- 1.37 A (3.4 mW)
- 5.84 x 4.56 mm^2, 8 x8 mm^2 die

CORE 1γ

- 8 bit, bit-serial,
- 128 bit instruction and 64 bit data cache
- 1000 MOPS at peak
- **25 GHz bit-operation**
- 4-stage pipelining
- 22,302 JJs
- 2.63 A (6.5 mW)
- 6.36 x 6.36 mm^2, 8x8 mm^2 die

M. Tanaka, T. Kawamoto, Y. Yamanashi, Y. Kamiya, A. Akimoto, K. Fujiwara, A. Fujimaki, N. Yoshikawa, H. Terai, and S. Yorozu, Supercond. Sci. Technol. 19 (2006) S344

Low-Pass Analog-to-Digital Converter



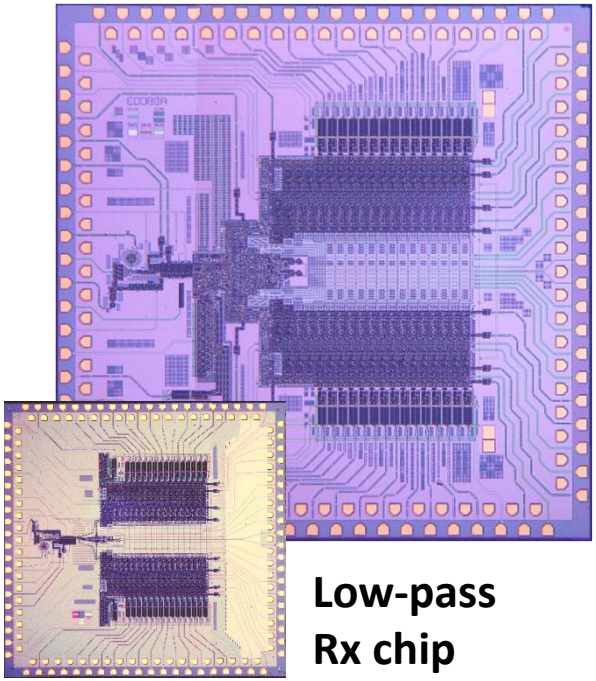
- 6,000 Josephson Junctions
- 2-channel Synchronizer
- 15-bit output
- 20 GHz Sample Clock
- Selectable decimation ratios – 1:128, 1:64, 1:32, 1:16

Based on S. Rylov's phase mod-demod delta modulator design

S. V. Rylov, et al., "High resolution ADC system," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 2649-2652, 1997

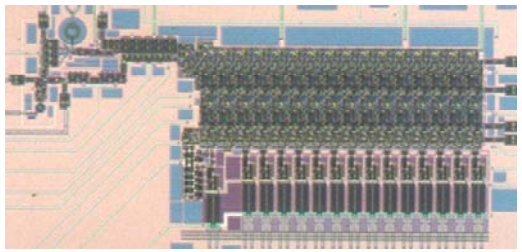
The 1st real (commercial-grade) application of digital superconducting electronics

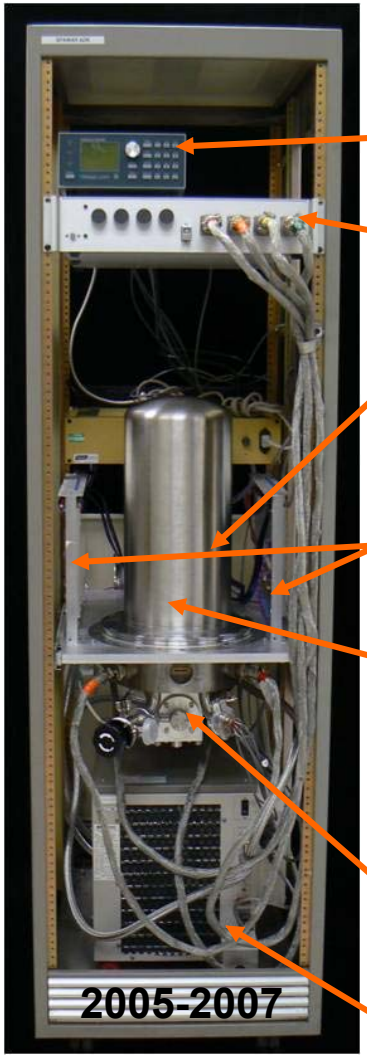
30 GS/s X-band Rx chip



Low-pass Rx chip

ADC modulator **DSP-Decimation Filter**





2005-2007

HYPRES' RSFQ Digital-RF Receiver

- temperature controller
- current source
- data acquisition and processing board (FPGA)
- output amplifiers
- vacuum enclosure with LTS chip and HTS filters mounted inside
- Sumitomo cryocooler
- compressor

circa 2010

D. Gupta *et al*., "Modular, Multi-Function Digital-RF Receiver Systems," in *IEEE Transactions on Applied Superconductivity*, vol. 21, pp. 883-890, 2011.

O. A. Mukhanov, D. Kirichenko, I. V. Vernik, T. V. Filippov, A. Kirichenko, R. Webber, V. Dotsenko, A. Talalaevskii, J. C. Tang, A. Sahu, P. Shevchenko, R. Miller, S. B. Kaplan, S. Sarwana, and D. Gupta, "Superconductor Digital-RF receiver systems," *IEICE Trans. Electron.*, vol. E91-C, pp. 306-317, Mar. 2008.

Attempt #2: IARPA Superconducting Computing Program

Cryogenic Computing Complexity (C3)

SFQ-based computer

- Approach based on:
  - *Near-zero energy* superconducting **interconnect**
  - *New* SFQ **logic** with no static power dissipation
  - *New energy efficient* cryogenic **memory** ideas
  - ***Electrical or optical*** inputs and outputs
  - ***Commercial*** cryogenic refrigerators

IARPA C3 program basis

2014 -2018

- **Logic thrust:** IBM team (Hypres), NGES
- **Memory thrust:** Raytheon BBN team (Hypres), NGES team
- MIT-LL (fab), NIST (test verification), Sandia (failure analysis) – Gov. support teams

Manheimer, M.A., "Cryogenic Computing Complexity Program: Phase 1 Introduction," IEEE Transactions on Applied Superconductivity, vol.25, no.3, June 2015.

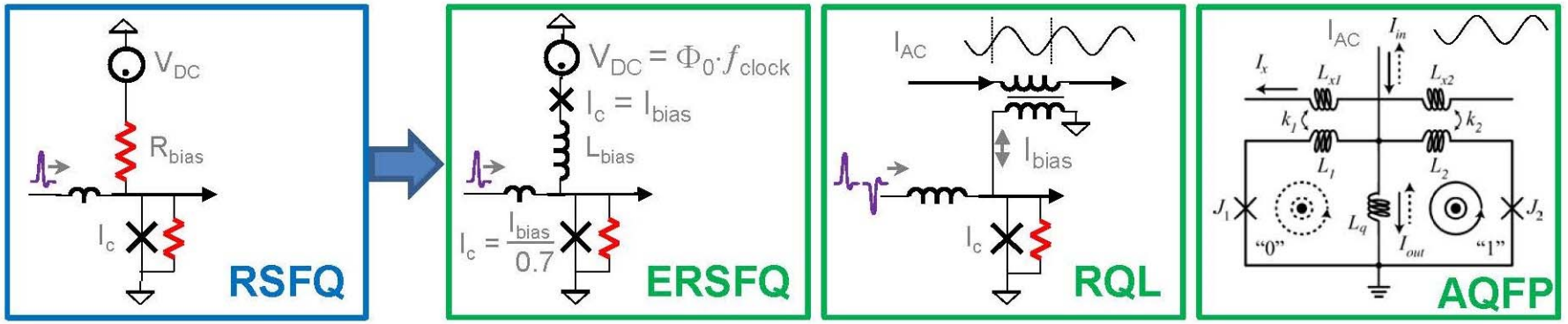
D. S. Holmes, A. L. Ripple, M. A. Manheimer, "Energy-efficient superconducting computing – power budgets and requirements," IEEE Trans. Appl. Supercond., vol. 23, Jun. 2013.

>2010 Energy-Efficient Computing

"CMOS progress levels up…"

Post-RSFQ Energy Efficient Logics:

Addressing RSFQ static power: LR-RSFQ, eSFQ, ERSFQ, RQL, LV-RSFQ, AQFP



Rapid Single Flux Quantum

Energy-efficient Rapid Single Flux Quantum (Hypres)

Reciprocal Quantum Logic (NGC)

Adiabatic Quantum Flux Parametron

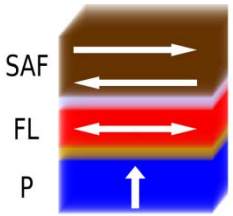
Courtesy of S. Holmes

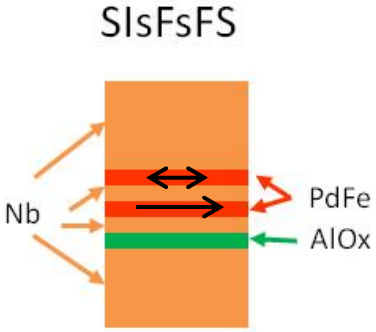
Energy Efficient and Dense Memory:

Hybridization on devices level - adding new cryogenic devices in JJ circuits

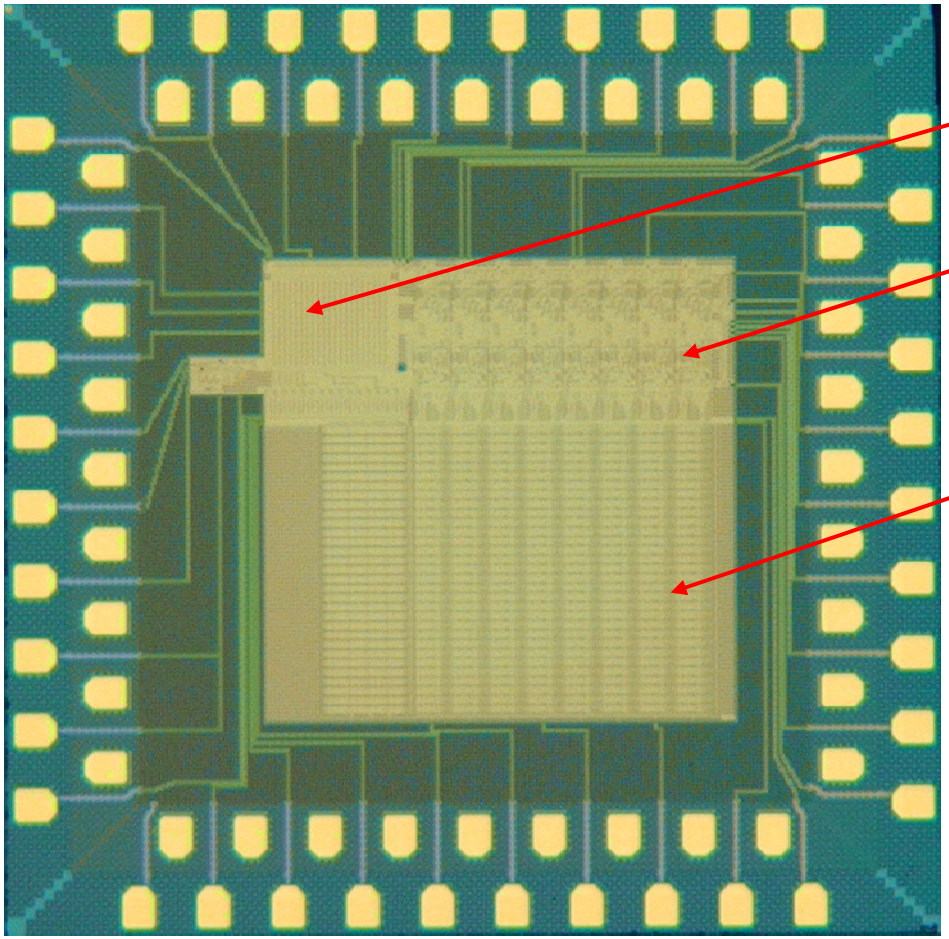
New cryogenic memory devices:

- NYU, Cornell
- Cambridge, Tubingen, Leiden, Twente
- ISSP RAS, Hypres (SeeQC),
- Northrop Grumman, MSU, ASU
- NIST





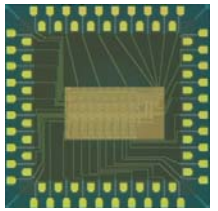
Hypres 8-bit Microprocessor



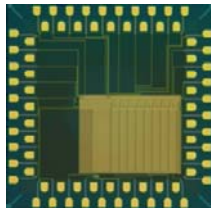
5 mm x 5 mm chip
Fabricated at MIT-LL in SFQ5ee process

Instruction Memory
(8 bit x 13 instructions)

ALU (8 bit)



Register File
(8 bit x 31 words)



The bit width of the IM is defined by three 5 bit addresses (2 read and 1 write addresses) for Register File and a 6 bit instruction code for ALU (21 bits in total).

The total area of the CPU is ~2.5 x 2.5 mm^2, total number JJs is ~ 28,000

Designed by Alex Kirichenko

Under IARPA C3 project

What is about today?

ALESSANDRO ROSSI & M. FERNANDO GONZALEZ-ZALBA, THE CONVERSATION
29 JUL 2019

A new disruptive technology is on the horizon and it promises to take computing power to unprecedented and unimaginable heights.

And to predict the speed of progress of this new "quantum computing" technology, the director of Google's Quantum AI Labs, Hartmut Neven, has proposed a new rule similar to the Moore's Law that has measured the progress of computers for more than 50 years.

Cryopackaging marvel

By Erik Lucero, Google | Wired, Dec. 2018

Google QC setup

From ICQT conf. July 2019

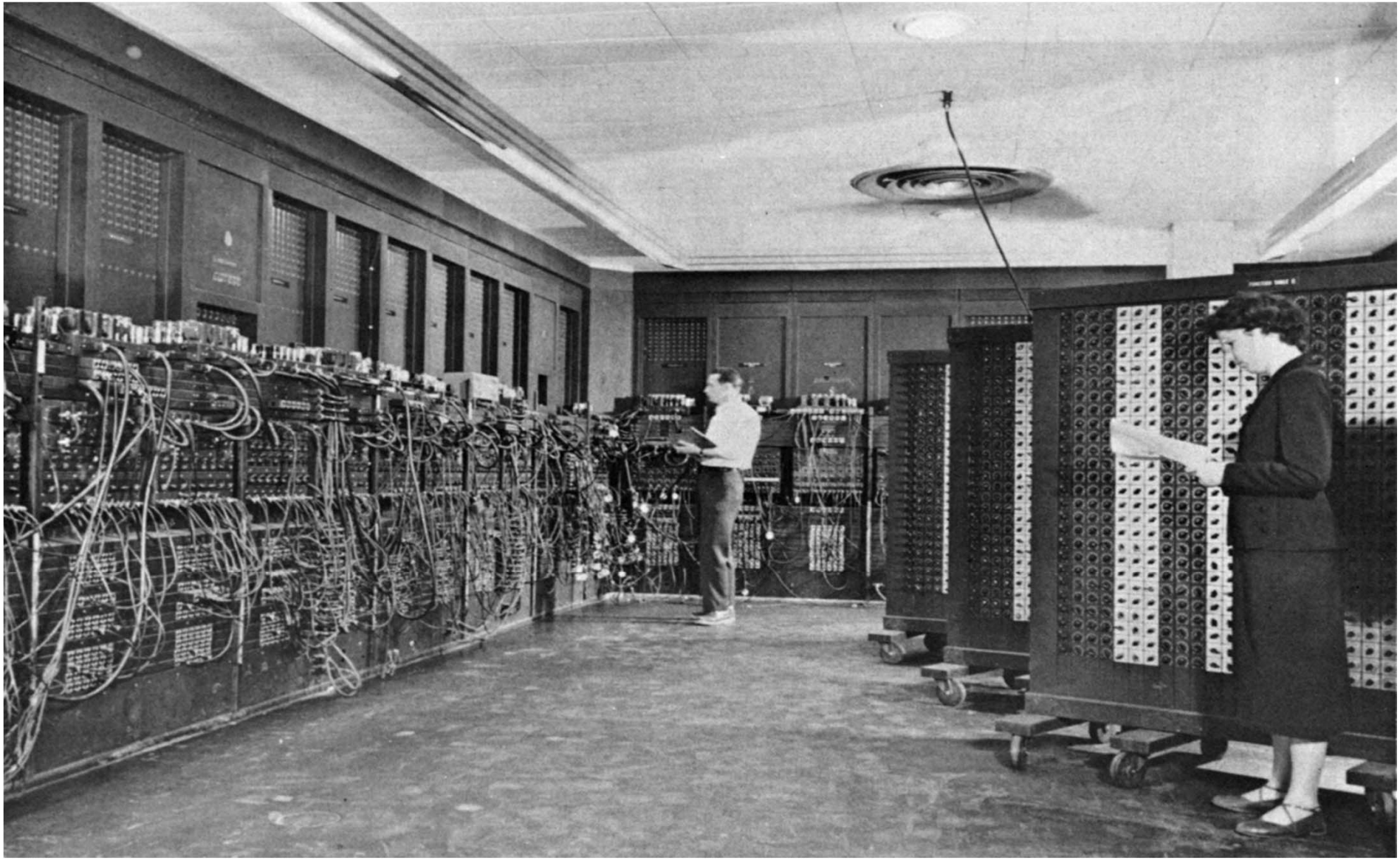
Quantum Computing: microwave qubit control

- Coaxial cabling for microwave communication with qubits.
- Typically needs >2 coaxes per qubit ($5,000/line from room temperature to 20 mK).

Dilution refrigerator setup

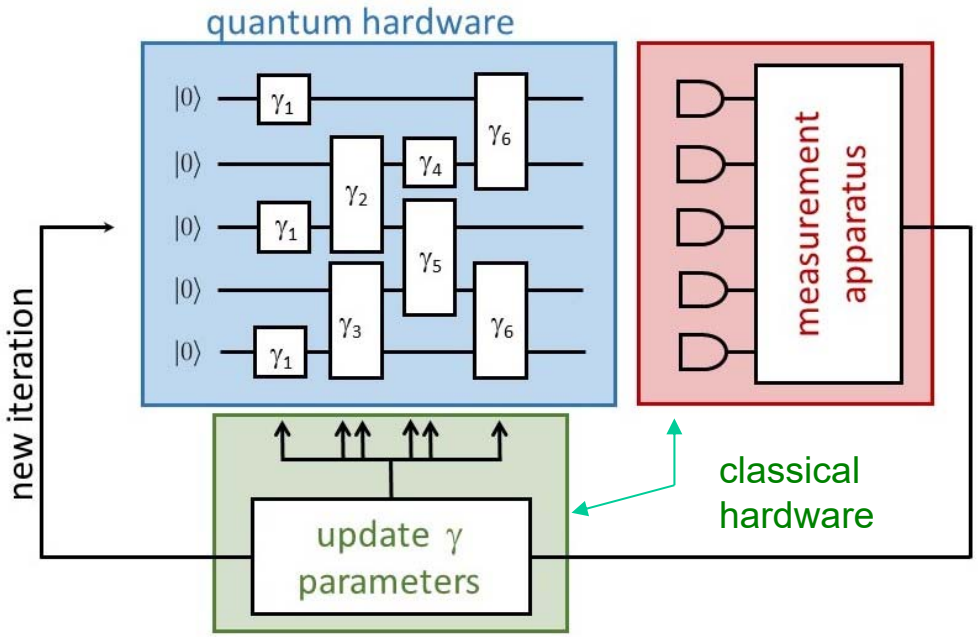
IBM 20-qubit system setup
(J. Chow, Q2B conf., Dec. 2017)

ENIAC (1946, University of Pennsylvania)



What is Quantum Algorithm

- Typical quantum algorithm is a **hybrid of quantum and classical** information processing
- Execution of quantum algorithms requires both quantum and classical computing hardware



Example of hybrid quantum-classical algorithm for quantum chemistry applications

Source: Intel Labs, 2017

"There is no quantum computer without classical computer,"

Dario Gil, Director of IBM Research

Path to Scalable Quantum Computing

- **Use cryogenic classical circuits co-located in the same cryostat:**

1. **Replace racks of equipment with embedded cryo electronics**

   Cryogenic electronics should be co-located in the same cryostat to implement high fidelity qubit readout, control and error correction

2. **Eliminate the need for coaxial cables from RT to 20mK**

   Need only min coaxial cabling for clock and ribbon cables or fiber for digital data load/unload

3. **Co-locate qubit and classical chips to form low latency hybrid hardware system**

   Reduce latency between quantum and classical modules and

   increase speed of information processing

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Options for co-located cryogenic classical circuits

CryoCMOS

- Can work in cryogenics, but still dissipates relatively large power
- Edoardo Charbon work (EPFL/TUD) readout/control for spin qubits (needs 8 dc and 2 RF lines per qubit) recreating room-temperature solution at cryogenic temperatures. Best fit is for semiconductor spin qubits.
- Google/Bardin team developed mixed-signal circuits for superconducting qubits (transmon type qubits) (ISSCC'19). Showed 2mW CryoCMOS single qubit control at 3K.

Superconductor electronics

- Low-power, fast electronics based on SFQ logic.
- Much lower integration density than CMOS
- Recreating room-temperature solutions (e.g. AWG) with SFQ logic is a complex task. The result may not be competitive.

SFQ for cryogenic classical circuits

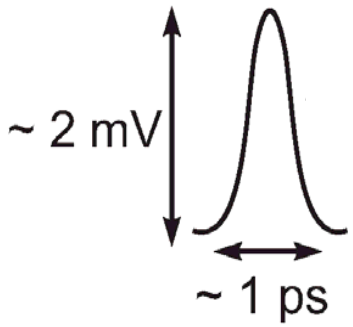
- **Qubit Control & readout + Classical co-processing**
  - Billions of transistors in CMOS controllers and .
  - How many years we need to wait until superconducting electronics will recreate this?
  - 20? 50?

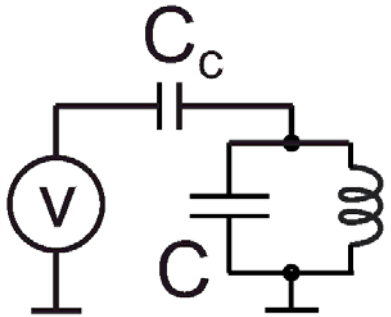
Is there an SFQ-inspired solution?

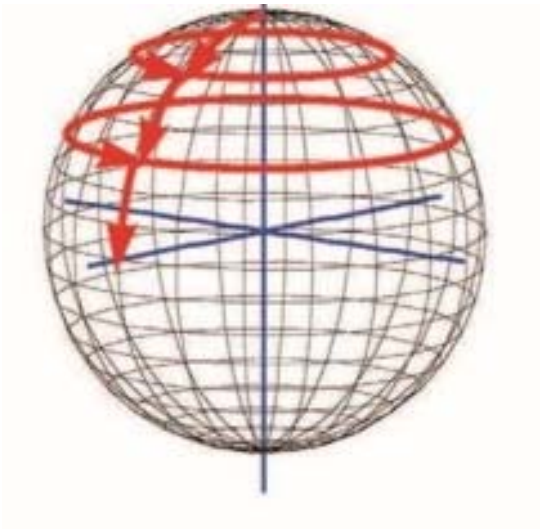
(not a copy of a CMOS solution)

Energy Coupled from SFQ Pulse

R. McDermott and M. G. Vavilov, "Accurate Qubit Control with Single Flux Quantum Pulses," *Phys. Rev. Applied* **2**, 014007 (2014)







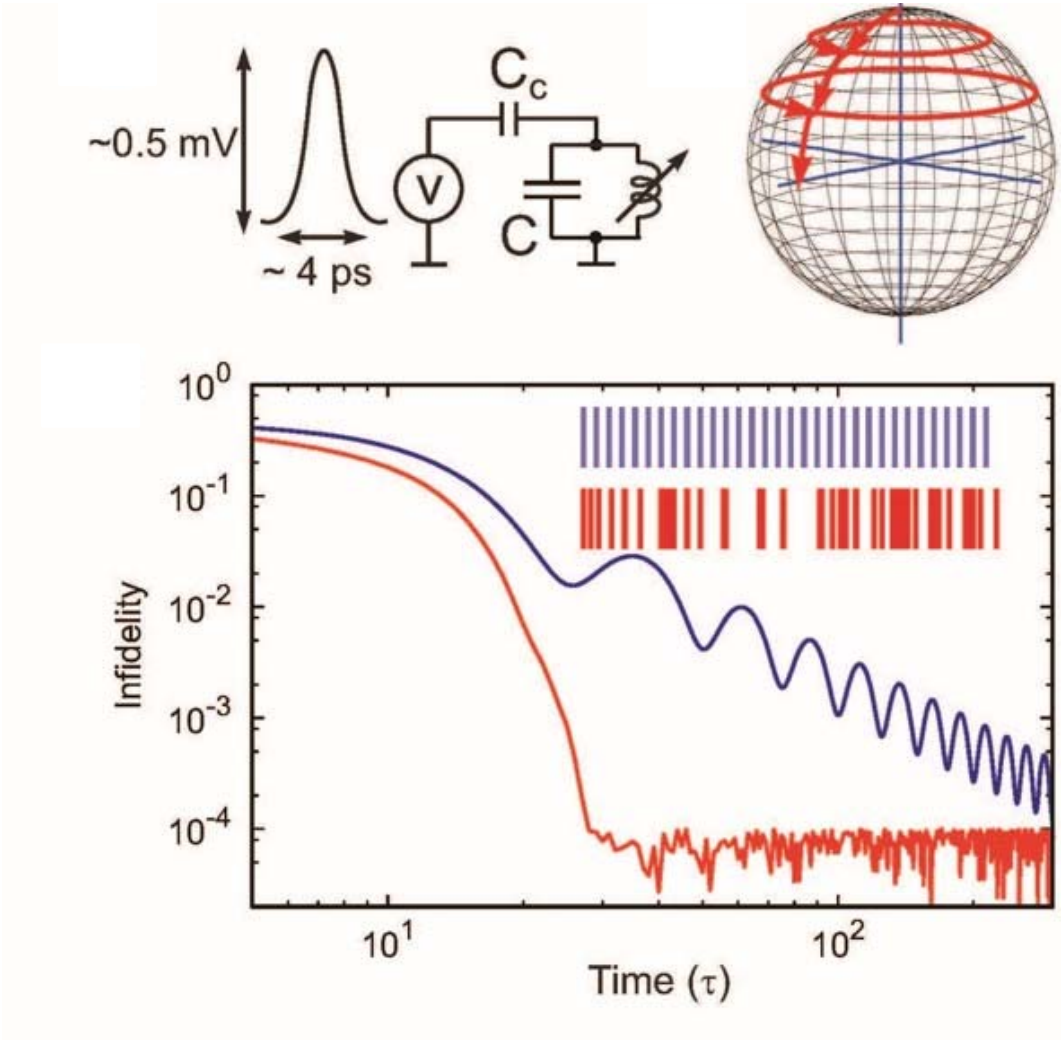
width of SFQ pulse much
less than oscillator period
→ approximate as δ-function

V(t) = Φ_0 δ(t) → $E_1 = \frac{\omega_0^2 C_c^2 \Phi_0^2}{2C'}$ **C' = C_c + C**

For C = 100 fF, C_c = 100 aF, $\omega_0/2\pi$ = 5 GHz, only 6.6e-5 quanta per SFQ pulse

Courtesy of R.McDermott, Wisconsin U.

Resonant Excitation of Qubits by SFQ pulses



- Feasibility proven by Wisconsin and Syracuse University groups
- By varying distance between SFQ pulses in the train using control theory, one can achieve higher fidelities as shown by Saarland Univ. team

R. McDermott, M. G. Vavilov, B. L. T. Plourde, F. K. Wilhelm, P. J. Liebermann, O. A. Mukhanov, T. A. Ohki, "Quantum-classical interface based on single flux quantum digital logic," *Quantum Sci. Technol.*, 2018

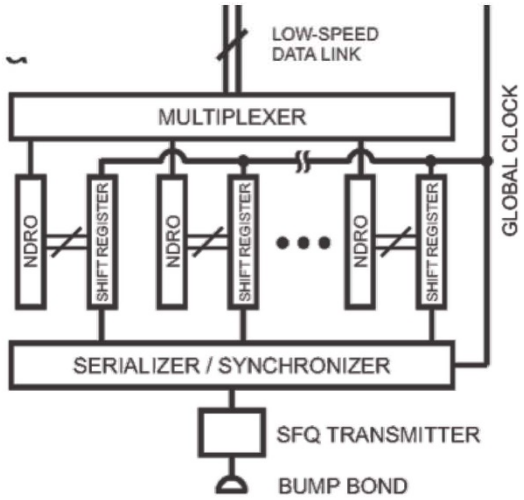
Improving Fidelity by using optimal control

SFQ Pulse Pattern Generator

- For more accurate qubit control, need to be able to generate more complex patterns of SFQ pulses

P. Liebermann *et al.*, Phys. Rev. Appl. 6, 024022 (2016)

UNIVERSITÄT DES SAARLANDES

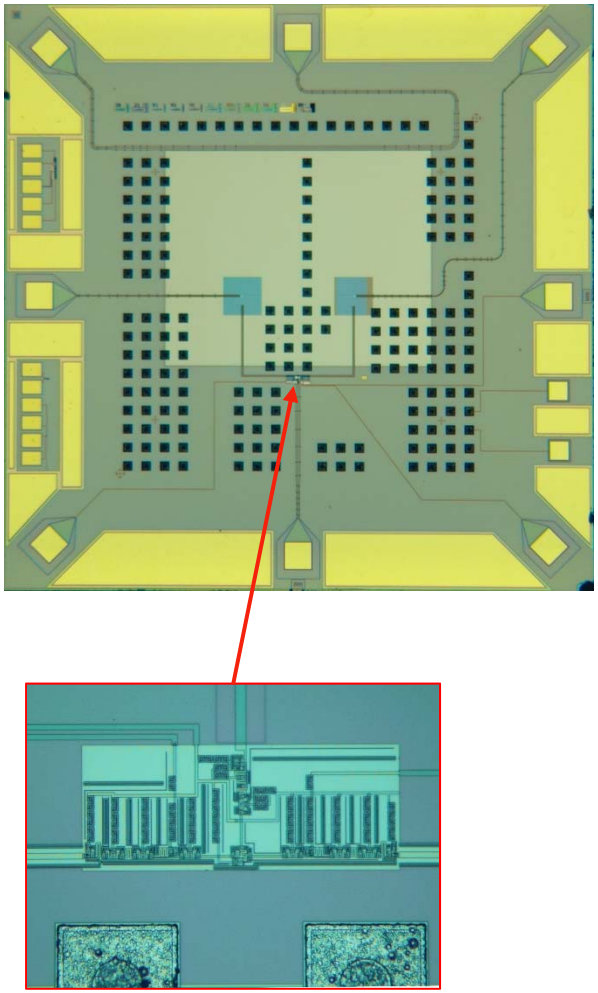


Classical SFQ controller

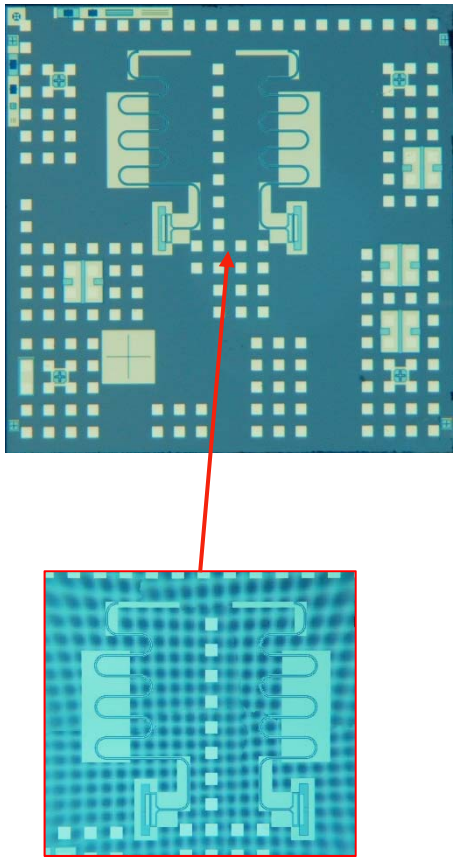
R. McDermott, M. G. Vavilov, B. L. T. Plourde, F. K. Wilhelm, P. J. Liebermann, O. A. Mukhanov, T. A. Ohki, "Quantum-classical interface based on single flux quantum digital logic," *Quantum Sci. Technol.*, 2018

- By varying distance between SFQ pulses in the train using control theory, one can achieve higher fidelities as shown by Saarland Univ. team
- Recent theoretical advance shows that achieving >99.99% fidelities is doable with low SFQ hardware complexity (55 bit shift register with 25 GHz clock)
  - K. Li, R. McDermott, M. Vavilov, "Scalable Hardware-Efficient Qubit Control with Single Flux Quantum Pulse Sequences," arXiv:1902.02911 [quant-ph]

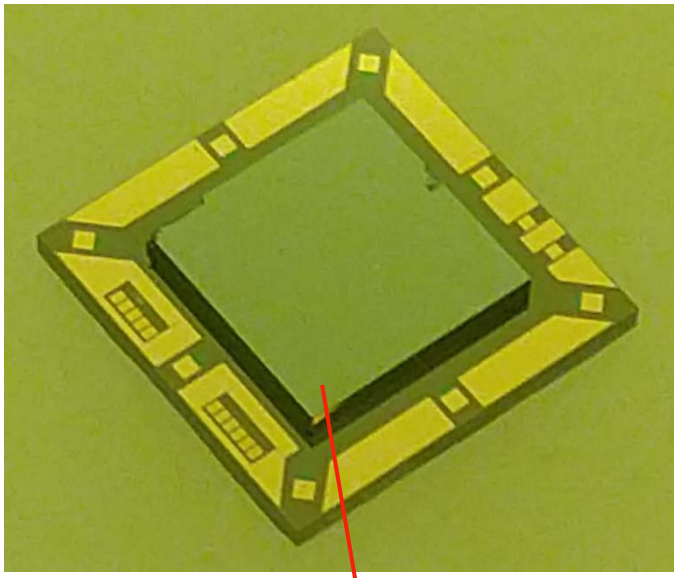
Wisconsin-Syracuse-SeeQC Project

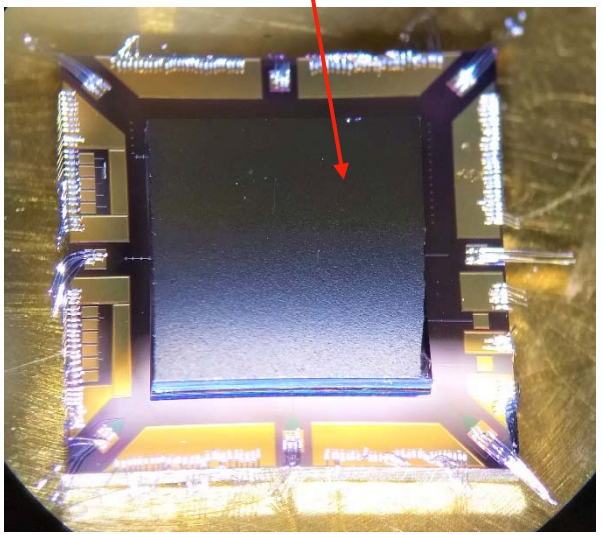


SFQ Control Chip



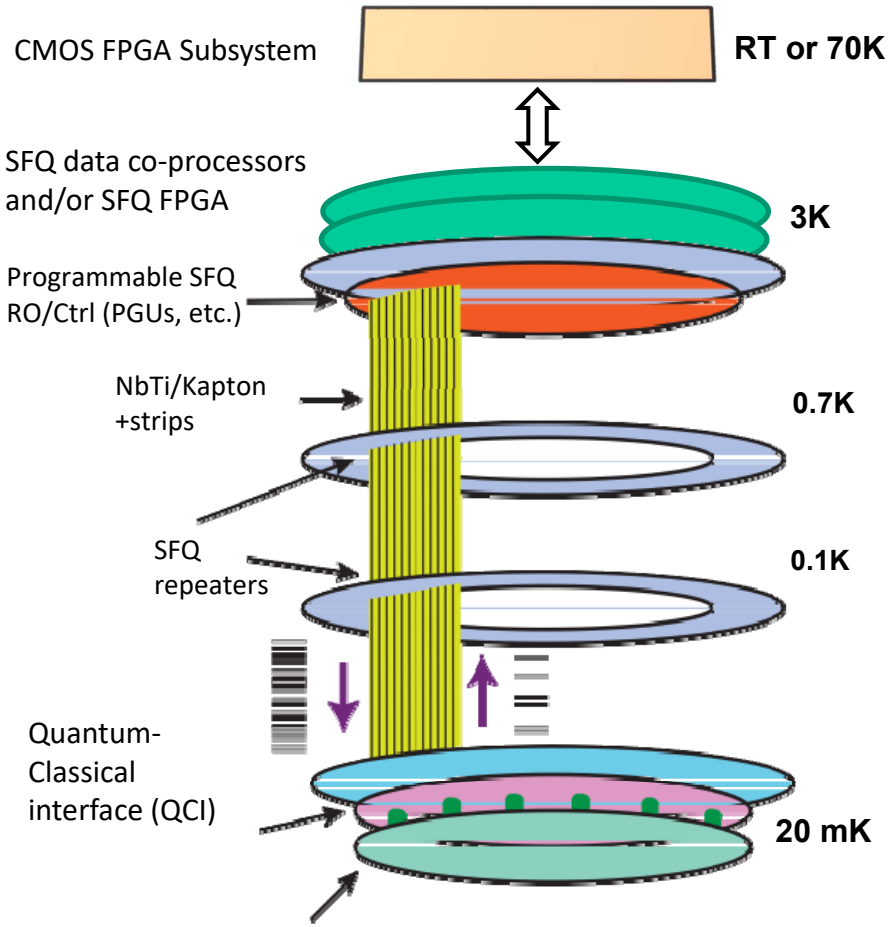
2 transmon chip





Assembled multichip module

Hybrid Quantum-Classical Processing Computer



- Classical SFQ based processors for full error-correction and execution of classical algorithms
- SFQ based readout and control for quantum layer (SFQ RO/Ctrl) co-processor
  - The Pattern Generator Unit (PGU) stores and streams dense classical bitstreams to the quantum array to induce coherent rotations and entangling gates.
  - Readout data pre-processor
- QCI mediates the interaction between the quantum array and the classical coprocessor
- Communication between the classical coprocessor and the interface layer is accomplished via superconducting microstrip flex lines, with SFQ repeater stages at intermediate temperatures to ensure accurate timing and faithful transmission of classical bitstreams

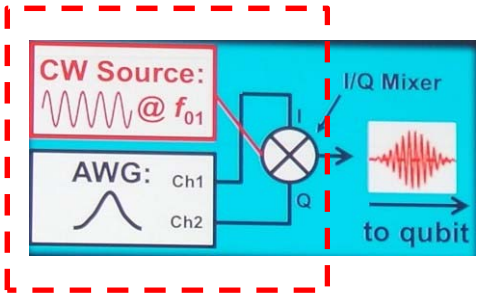
R.McDermott, M.Vavilov, B.Plourde, F.Wilhelm, P.Liebermann, O.Mukhanov, T.Ohki, "Quantum–Classical Interface Based on Single Flux Quantum Digital Logic," *Quantum Sci. Technol.*, 3 (2), 024004, 2018

Qubit Readout/Control: Analog *vs* Digital

Current approach

Large, expensive electronics racks distant from qubits

Microwave equipment



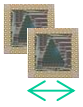
Analog qubit control:

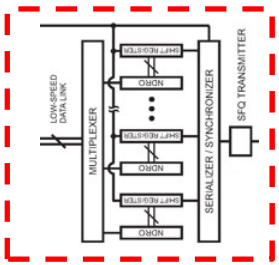
- Complex
- High latency
- Noisy
- Expensive
- Large I/O count
- Non-scalable

Not to scale

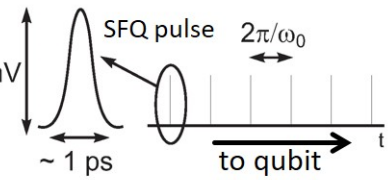
Superconducting circuit approach

Small, low-cost cryogenic chips in close proximity to qubits





SFQ digital circuits



SFQ pulse train

Digital qubit control:

- Naturally integrated
- Low latency
- Less noise
- Low cost
- Reduced I/O scaling law
- Scalable

R. McDermott, et al., "Quantum-classical interface based on single flux quantum digital logic," *Quantum Sci. Technol.*, 3 (2), 024004, 2018

- **Thank you**