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# Hybrid Semiconductor-Superconductor Fast-Readout Memory for Digital RF Receivers

O. A. Mukhanov, *Senior Member, IEEE,* A. F. Kirichenko, T. V. Filippov, S. Sarwana

***Abstract*—Results of the development of a new type of a hybrid memory for superconducting Digital-RF receivers supporting 30 Gbps memory readout speed are presented. The main feature of this memory is a combination of a high capacity room-temperature memory and a high speed on-chip superconductive cache in order to provide digital waveform templates for Digital-RF signal processing. As a room-temperature high-capacity memory with fast readout, we selected Sympuls pattern generator BMG 30G-64M capable of producing a 30 Gbps serial data stream of programmable pattern of 67,108,864 bits. We designed, fabricated, and tested an on-chip cache which receives high-speed template serial data from the room temperature memory and converts it into a stream of 3-bit words of template of local oscillator (LO) for digital mixer. We integrated the memory with a 1x3-bit digital I/Q mixer (1-bit digitized RF stream multiplied by 3-bit digital LO).**

***Index Terms*—RSFQ, SFQ, DSP, DRFM, cryogenic, RF template, waveform library, digital correlator**

## I. INTRODUCTION

A long-standing problem with a high capacity memory for cryogenic superconductor electronics can be untangled for some specific applications. These applications are related to special purpose digital signal processing which employs a substantially streamlined traditional memory hierarchy.

We have been developing Digital-RF signal processing (RF DSP) technology based on fast processing of the digitized RF waveforms rather than digital processing of baseband data [1]. The extreme speed requirements for such digital processing are met with superconductor RSFQ technology. A family of Digital-RF channelizing receivers has been successfully demonstrated [2], [3]. These receivers perform digital signal channelization of the digitized wideband RF data enabled by high-speed RSFQ digital signal processing. Such digital receivers require loading of a digital template of the selected local oscillator (LO) to set the frequency channel. Channelization signal processing requires an asymmetric memory operation: relatively infrequent memory addressing for the stored local oscillator digital waveforms and their fast loading to a processor. The LO waveforms are periodic and therefore do not take significant memory. A similar memory operation pattern is required for the Digital-RF correlation receivers [4]. For these receivers, the stored waveform digital templates may not be periodic and can require substantial memory resources. These waveform digital templates are to be loaded to the RSFQ cross-correlator(s) for correlating with the digitized RF signal. In a nutshell, Digital-RF receivers predominantly require fast loading of the stored data from larger slower memories to smaller faster cache memories integrated with RSFQ processing circuits.

In this paper we present the architecture, design, and test results of a hybrid memory for Digital-RF receivers combining room-temperature semiconductor deep memory and a cryogenic superconductor RSFQ cache. The cache is integrated with an RSFQ multi-bit digital mixer [5] – a critical DSP circuit of a Digital-RF channelizing receiver.

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Authors are with HYPRES, Inc., Elmsford, NY 10523 USA (phone: 914-592-1190 ext. 7801; fax: 914-347-2239; e-mail: mukhanov@hypres.com).

## II. HYBRID MEMORY DESIGN

### A. Hybrid Memory Configuration

Since superconducting SFQ memories do not have large capacity [6] and cryogenic hybrid Josephson-CMOS memories are not yet available [7], we pursue a **h**ybrid **t**emperature – **h**ybrid **t**echnology ($ht^2$) approach [2]. In this approach, we integrate a large capacity room-temperature semiconductor memory and a fast cryogenic RSFQ cache integrated on the same chip with an RSFQ digital signal processor. The asymmetric nature of the required memory operation – predominant readout, infrequent addressing, no writing functions, allows us to utilize pipeline loading in order to avoid latency issues.

Fig. 1 shows our hybrid memory configuration and its integration into a Digital-RF channelizing receiver. It consists of room-temperature high–capacity memory capable of fast readout and a cryogenic superconducting RSFQ cache capable of receiving serial data, its re-synchronizing and deserializing. This cache memory is integrated with the In-phase (I) and

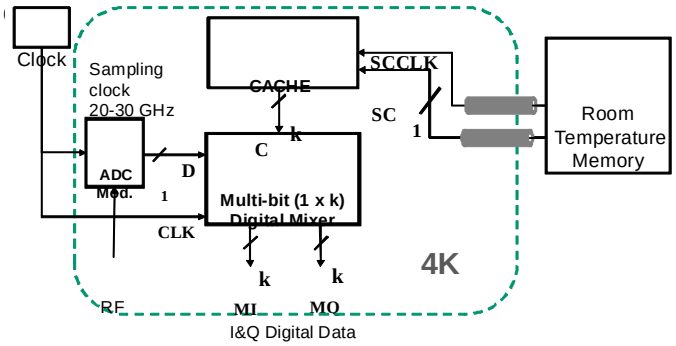



Fig. 1. Hybrid memory configuration.

For multi-bit mixing or correlation, the room-temperature memory should ideally supply multi-bit words at the sampling clock frequency (20-30 GHz). However, it is impossible to send all bits in parallel due to inevitable inter-bit jitter during transmission over the rather long distance between a room temperature memory module and a cryogenic RF DSP. To avoid this problem, we supply data serially and then perform on-chip data synchronization and deserialization. This also relaxes the specifications for the room-temperature memory.

Since our oversampling ADC modulators [8] produce a 1-bit output data stream at high sampling rate, a fast 1 x k digital mixer is required. Our estimates show that the LO template should have at least 7 bits (k = 7) to achieve a nearly ideal mixing performance even for the large oversampling ratios desired for achieving higher receiver performance [9].

### *B. Room-Temperature Deep Memory*

Our objective was to find a commercially-available memory unit with a relatively deep storage capacity (at least 64 MBit) and capable of providing a 30 Gbps single-bit output data. These functions match well to those of Arbitrary Bit Sequence Generators (ABSGs) and we chose Sympuls BMG 30G-64M 30 GBit/s pattern generator (Fig. 2) [10]. It generates programmable and pseudo random binary sequences operating with an external clock generator between 1 and 30 Gbit/s. Six different patterns are selectable: PRBS pattern with $2^7$-1, $2^{15}$-1, $2^{23}$-1 and $2^{31}$-1 bit length, one manually programmable user pattern with 256 bit length and a user pattern with 67,108,864 bit length, programmable by USB interface. At the front panel complementary data signals (NRZ and /NRZ), several clock si

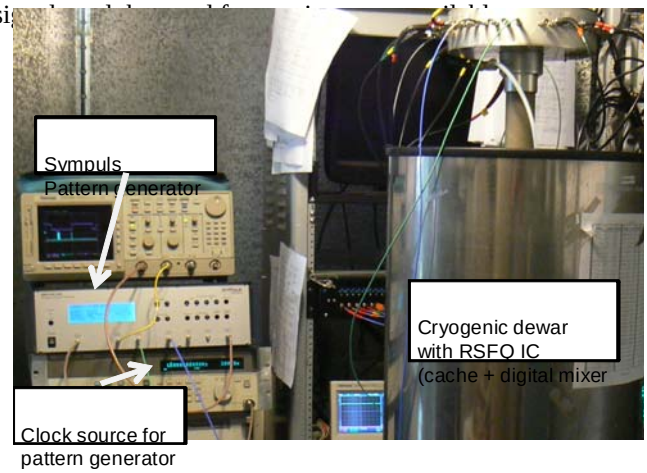



Fig. 2. Test setup including Sympuls BMG 30G-64M 30 GBit/s pattern generator as a room-temperature deep memory with fast readout.

### *C. On-chip Cache Memory*

The main function of the cache circuit is to receive high-speed serial data from room temperature, perform data synchronization (find end-of-word), and deserialize data into parallel output words for the digital mixer. To facilitate synchronization, we reserved the last bit in the data word as the end-of-word bit.

Fig. 3 shows a block diagram of the cache circuit. The deserializer part (DS) of the cache design is based on a shift-and-dump demultiplexer architecture [11] and implemented using dual-port DFF cells derived from the B flip-flops [12]. The data synchronization is performed by a clock controller circuit (CU) consisting of a static frequency divider and a synchronization circuit.

The serialized data is received by a high-speed dc-to-SFQ converter and applied to a deserializer (DS). The clock controller splits every 8 pulses of external high-speed clock SCCLK into 7 serial clock pulses and 1 parallel read-out clock pulse which destructively reads out the content of the deserializer. The last bit (sync bit) of the readout word is fed back to the clock controller to provide data synchronization. If synchronization bit is of the wrong value, the clock controller shifts the read-out clock by one period, searching for the end-of-word symbol, thus automatically recovering lost synchronization.

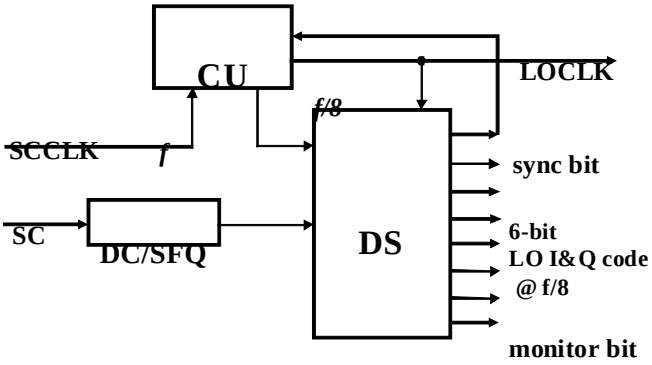



Fig. 3. Block diagram of RSFQ cache circuit consisting of an 8-bit deserializer (DS) controlled by a clock controller (CU).

### *D. Integration of Cache and Multi-bit Mixer*

The deserializing cache memory modules described above were integrated with the multi-bit digital mixer on the same chip. The design principles of this digital mixer are described in [5]. In order to facilitate the integration, the original design of the multi-bit (1 x k) mixer was modified. Fig. 4 shows the block diagram of the 1 x k mixer bit-slice adapted for the integration with the cache memory circuit. Specifically, a buffer (the rightmost DFF) was placed between deserializer and mixer for synchronizing master clock (CLK) of the mixer with LO code. The LO code is stored in RSN cells for several sampling clock (CLK) cycles until the next parallelized LO code arrives. With this timing design, the cache and the mixer can operate under different independent clocks (SCCLK and CLK) (Fig. 5). Thus, room-temperature memory does not have to be synchronized with RSFQ processor master clock. The LO code loaded to the mixer LO inputs can be used for multiple cycles of RF data.

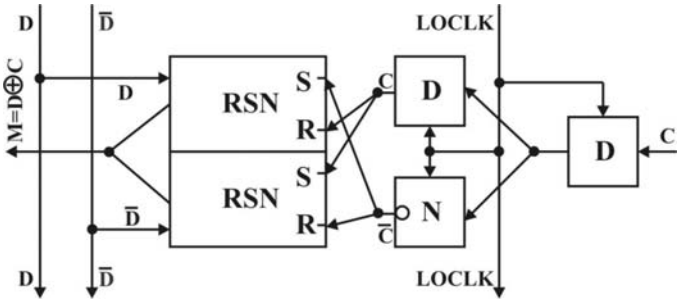



Fig. 4. Block diagram of 1 x k mixer bit-slice modified for integration with cache memory module.

Due to the test chips space limitation (5 mm x 5 mm chip), it was decided to limit LO word length to 3 bits for *I* and *Q* components (Figs. 5 and 6). Subsequently, the 8-bit cache was divided into a 4-bit block I-DS and a 4-bit block Q-DS in order to accommodate 1 bit for synchronization, 6 bits for LO code payload (3-bit I and 3-bit Q), and 1 bit for monitor.

Fig. 6 shows a layout of the integrated cache circuit and the 1 x 3 digital mixer fabricated using HYPRES 4.5 kA/cm$^2$ fabrication process [13]. The 7 bit cache circuit is divided using a set of microstrip lines traversing synchronous pulse distribution network (SPDN) section. The SPDN is a co-flow shift register to distribute data and it's complementary from ADC modulator to digital mixing units [5]. It also delivers Nyquist clock and digital filter readout clock from frequency divider to digital decimation filters (not shown in Fig. 6) that follow mixer. The distribution of all SFQ pulse streams are controlled by master clock (CLK). These frequency divider and decimation filters are the required parts of Digital-RF Receiver (ADR) systems [2], [3]. Clock controller (CU) is integrated with the I-DS cache block but serves the entire 8 bit ca

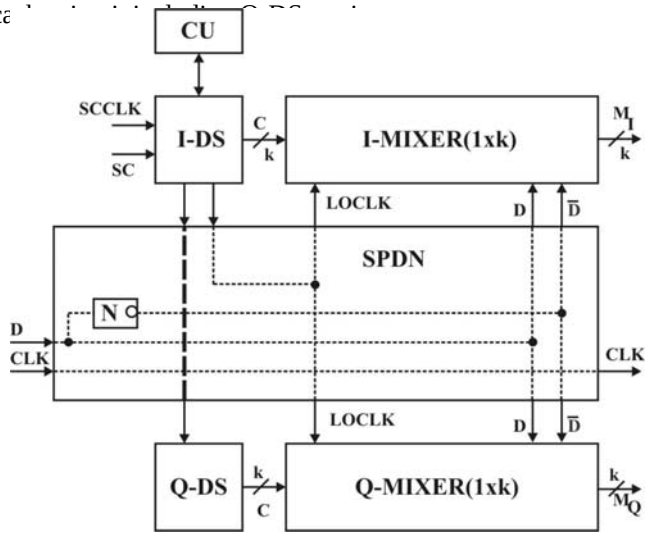



Fig. 5. Block diagram of the integrated I and Q cache blocks (I-DS, Q-DS, respectively) with the 1 x k digital mixer. The I and Q cache blocks are controlled by controller unit (CU) and integrated with I and Q mixers, res

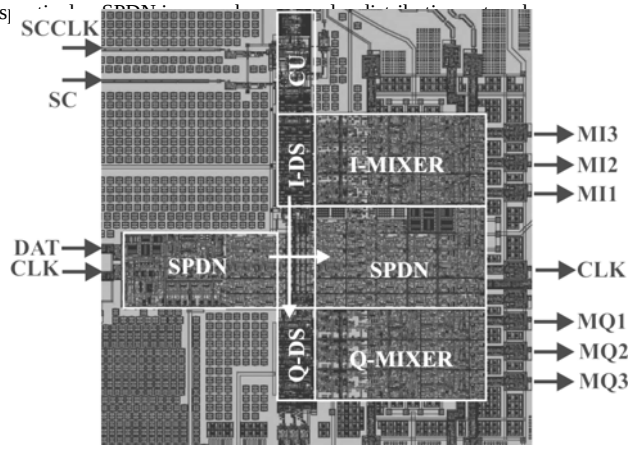
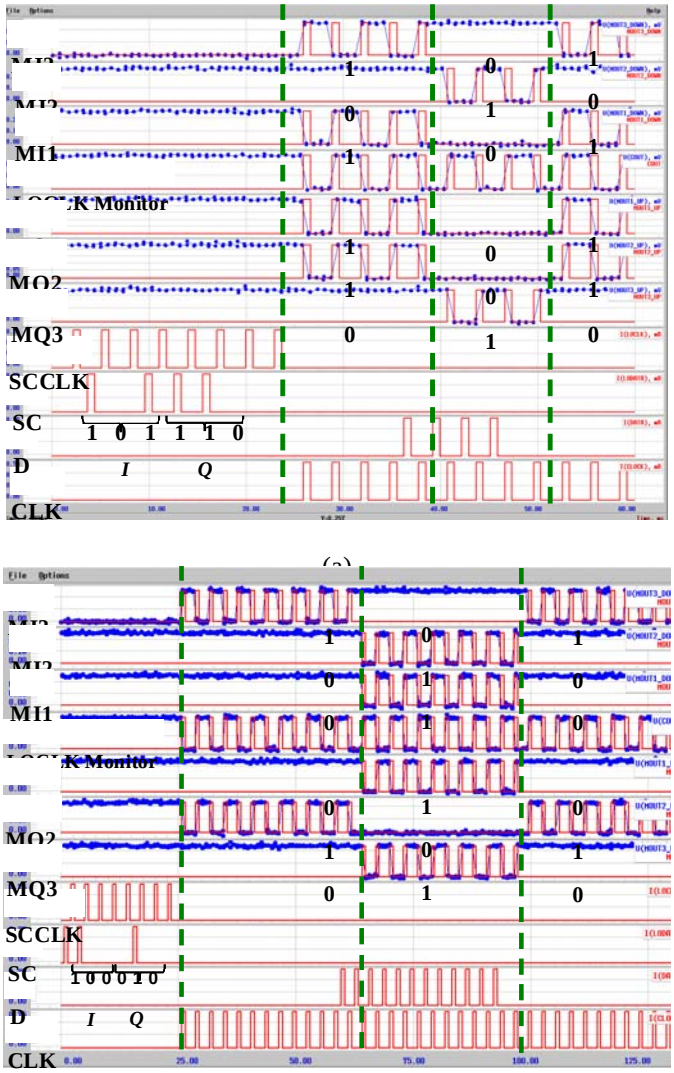



Fig. 6. A layout fragment (2.5 mm x 3.0 mm) of the integrated on-chip cache and a 1 x 3 digital mixer. A 8-bit cache is divided into a 1-bit sync with 3-bit In-phase (I-DS) cache and a 3-bit Quadrature (Q-DS) cache with 1-bit monitors connected by passive transmission lines.




(b)

Fig. 7. Correct functionality of the integrated circuit of a 1 x 3 mixer and a 8-bit cache accommodating a 6-bit LO code payload (3-bit I and 3-bit Q). It demonstrates correct mixer operation with loaded 6-bit LO patterns: (a) 101110 and (b) 100010. Dashed lines separate sets of 0s,1s, and 0s of 1-bit D.

## III. Test Results

We have built and verified high-speed operation of all main components of our hybrid memory including separate cache circuits and digital mixer blocks. Here we describe testing of the integrated cache and multi-bit mixer in more detail.

Fig. 7 shows a functional test of the fabricated chip with integrated cache and digital mixer circuits (Fig. 6) for two examples of LO codes (101110 and 100010). This code containing 3-bit *I* and 3-bit *Q* LO words is loaded into I-DS and Q-DS caches, respectively. Then, 1-bit data (D) is applied - three sets of all "0"s, all "1"s, and all "0"s. As output data indicates, the 1 x 3 digital mixer correctly multiplies the 3-bit I&Q LO codes with the 1-bit data. One can notice that LO codes remains stored in the mixer for all sampling clock (CLK) cycles until they are reloaded with the next codes arriving serially from the room-temperature memory.

In order perform a high-speed testing to verify the full speed of the hybrid memory, it is necessary to have a chip with digital decimation filters capable of reducing the output

data rate to the rate suitable for the interface [2], [9]. The fabricated to date chip does not have digital filters.

## IV. Discussion

We have assembled a hybrid semiconductor-superconductor memory based on room-temperature large-capacity external memory with fast readout and a cryogenic (4K) RSFQ cache. The cache has been integrated on the same chip with fast RSFQ processing circuit - a multi-bit digital mixer. The cache is necessary to provide an adequate timing and physical conversion of digital data loaded from external memory into the digital mixer. It receives the serial data from the external memory and loads the deserialized parallel 2k-bit words to the RSFQ 1 x k mixer. The loaded data is used by the mixer for several cycles of the fast sampling clock – this allows one to operate a fast RSFQ DSP without latency limitations of the external memory. We verified the correct operation of the on-chip cache integrated with a 1 x 3 digital mixer. The full speed test of the entire hybrid system will require the integration of a whole digital channelizing receiver with decimation digital filters. The 7-bit I&Q cache modules (14-bit payload in total) and a 1 x 7 digital mixer are necessary to achieve sufficiently high performance with large oversampling ratios.

The losses in cables connecting the room-temperature memory and the cryogenic chip can be a serious detriment at 30 Gb/s. Therefore, it is important to minimize the length of the cables and to use a predistortion circuit to increase fidelity of the transmitted digital data. Once the RSFQ chip is integrated onto a cryocooler, the room-temperature memory can be located in a close proximity and the cable length can be shortened compared to ones used in the present dewar-based test setup shown in Fig. 2.

The implemented cache design is adequate for the channelizing receivers, since LO code is relatively short. The loading rate of the room temperature memory limits the maximum frequency of LO – for a 30 Gbps loading rate, a 3.75 GHz maximum LO frequency can be realized. For higher LO frequencies, multiple parallel cache modules would have to be used in a pipelined fashion. For longer templates necessary for the cross-correlating receivers, a longer on-chip cache would be required.

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