Progress with Physically and Logically Reversible Superconducting Digital Circuits

Jie Ren and Vasili K. Semenov

***Abstract*—We continue to develop a new Superconductor Flux Logic (SFL) family based on nSQUID gates with fundamentally low energy dissipation and the ability to operate in irreversible and reversible modes. Prospective computers utilizing the new gates can keep conventional logically irreversible architectures. In this case the energy dissipation is limited by fundamental thermodynamic laws and could be as low as a few k_BTs per logic operation. Highly exotic and less practical logically and physically reversible circuit architectures are more attractive for us because they allow to reduce specific energy dissipation well below thermodynamic threshold $k_BT\ln 2$. The reversible option attracts us because we like to experimentally demonstrate that all technical mechanisms of the energy dissipation could be cut below the fundamental thermodynamic mechanism. In other words, we like to set the absolute energy dissipation record for all conventional digital technologies that (if measured in k_BT) is about one million times below the best figures achieved in commercially available semiconductor circuits. Besides, we believe that diving below the thermodynamic threshold would have impressive scientific and philosophical impacts. In the paper we introduce a new timing belt clocking scheme and present new circuits. We still work with test circuits but some of them contain two 8-stage shift registers, one with direct and the other with inverted outputs. The energy dissipation per nSQUID gate per bit measured at 4 K temperature is already below the thermodynamic threshold. So we are confident that we passed through the critical phase of the project and we simply need more time to make more sophisticated circuits. The extremely low energy dissipation converts our circuits into a natural candidate to support circuitry for any sensors operating at milli-Kelvin temperatures.**

***Index Terms*—Superconductor digital devices, reversible computing.**

I. INTRODUCTION

THIS is our fourth IEEE paper devoted to reversible computing and here we report our recent progress. However, our approach is still not widely accepted and we think it is appropriate to give a general introduction partly repeating our earlier papers.

The general history of reversible computation was written by Bennett in 1988 [1] so brilliantly that the paper was reprinted by the journal again in 2000 [1]. In particular Bennett wrote that "…the development of electronic digital computers had naturally raised the question of the ultimate thermodynamic cost of computation, especially since heat removal has always been a major engineering consideration in the design of computer... A major turning point in understanding the thermodynamics of computation took place when Landauer … was able to prove a lower bound of order kT for some data operations, but not for others. Specifically, he showed that "logically irreversible" operations – those that throw away information about the previous logical state of the computer – necessarily generate in the surroundings an amount of entropy equal to the information thrown away… A major step … <was> Edward Fredkin<'s> … discovery of the billiard-ball model for computation…" This long quotation briefly covers Bennett's history of reversible computations.

At that time implementation of any reversible digital circuit was considered unthinkable and even insane. However, in 1977 Likharev assumed that a prospective reversible computer could be implemented using Josephson junction technology [2]. Two similar but hard to find publications are dated 1976 [3] and 1974 [4]. In 1982 more detailed estimations for ultimate energy dissipation within the suggested model for reversible computations were made [5]. But only at ASC-84 did we present optimized parameters of our reversible gate (parametric quantron) [6].

At that time we came to the conclusion that a higher speed rather than lower energy dissipation should be the major optimization goal. As a result, RSFQ logic was suggested [7]. However, a new logic gate similar to parametric quantron was suggested by a strong Japanese research team. The gate received the new name Quantum Flux Parametron (QFP) and it was selected as a key component of a large multi-year project [8]. The energy dissipation of practical QFP gates was still far from the thermodynamic threshold (about $1{,}000\,k_BT$ according to the introduction in [8]) but theoretically it could approach and cross the threshold [9].

Recently it became clear that a minimization of the energy dissipation could be vitally important for some new applications, in particular, those related with quantum computation. Then more conservative estimations of energy dissipation in superconductor digital circuits, that took into account the low efficiency of cryo-coolers and a parasitic heat flow, dramatically diminished the energy saving advantages of conventional superconductor RSFQ technology over the best energy-efficient CMOS technology. In other words, the energy efficiency is now a dramatically more important optimization factor than the speed. As a result, circuits able to operate in the

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reversible mode could be the ultimate winners of the race for prospective computation technologies.

This is why we returned to potentially reversible circuits eight years ago [10]. The main problem with known reversible gates was rather evident. We knew that the multi-phase AC power supply is the main or even fatal drawback of known reversible solutions. The drawback originated from large ($\sim 10^3 k_B T$) energy streams that should flow to and then back from any reversible gate at each clock cycle. The extremely low energy dissipation is achieved because the energy streams almost completely compensate each other. Electrical losses in the AC power lines should definitely be considered as part of the total energy dissipation and we must keep the losses per gate below $k_B T$ level. In plain words this means that the power line should recycle 99.9% of the applied energy or it should operate as a resonator with quality factor exceeding 10^3. This alone is an almost impossible task if the opposite sides of "the resonator" are at room and helium temperatures. The complexity of the task grows dramatically when we recall that we need three similar power lines with identical resonant frequencies.

In [10] we pointed out that a DC biased Josephson junction is a natural and fundamentally accurate DC/AC converter able to AC bias reversible gates. Moreover, each converter is integrated with its gate. As a result, our new device operates as a DC biased reversible gate. The first DC biased reversible gate was suggested earlier [11] but the new nSQUID is dramatically more robust. The second key component of our circuitry is a Long Josephson Junction (LJJ). We should refresh LLJ properties to explain our original "timing belt" clock scheme.

II. Long Josephson Junctions

A. General properties of LJJs

An enormous variety of LJJs have been thoroughly investigated both theoretically and experimentally. Properties of continuous LJJs are described by the sine-Gordon equation traced back to 1870 [12]. The equation is really unique because its solutions can be described as a combination of resting or freely moving vortices or solitons. In physical language these vortices can be described as quasiparticles able to move along LJJs with arbitrary speeds and without any dissipation. More exactly, the speed of a nondissipative movement is limited by the Swihart speed that is the "local" speed of electromagnetic waves in the device if Josephson effect is not taken into account.

The potentially nondissipative motion of a uniform train of vortices along ring LJJs described above is already utilized in some clock circuits that demonstrate an outstanding timing stability [13]. Our circuits utilize a similar motion but the implementation is quite different. This is because our primary optimization goal is lower energy consumption rather than the better clock stability. Besides, the circuit should cover the whole chip instead of being a compact device. Figure 1a illustrates a LJJ "timing belt". The light gray area marks the space to be occupied by logic gates. An incorporated vortex pump injects into the ring LJJ the required number of Josephson vortices. The timing of gates is provided by densely packed vortices that uniformly move along the belt (or ring). We decided to show in Fig. 1b a ribbon timing belt that can be found in many cars. We did it because their timing mechanisms are almost identical. In particular, each vortex acts as a tooth of the rubber belt. However, a translational symmetry for vortices in LJJ belts gives them a great advantage. Simply put, the vortices are absolutely identical, they are not affected by wear and tear and distribution of currents in the belt before and after its rotation on any integer number of vortices are fundamentally identical.

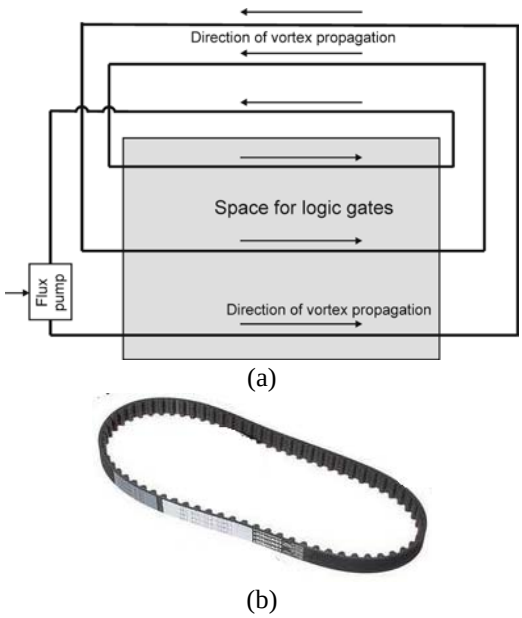

Fig. 1. Two functionally similar "timing belts". One is built as a long ring Josephson junction (shown as a black line) filled with vortices (a), while the other is a rubber belt used in cars (b).

Of course the complete lack of dissipation is only a convenient idealization and we should control the impact of parasitic factors responsible for highly undesirable losses. In fact, we deal with discrete rather than with continuous LJJs. Our LJJs can be described as microstrips made of two thin superconductor films sewn together by uniform stitches of equally distanced unshunted Josephson junctions (Fig. 2a). As we mentioned earlier the vortices are densely packed in the LJJ and, as a result, the size of a squeezed vortex coincides with the vortex period a but is still much larger than the distances between the junctions d (nominally $a = 8.5 \cdot d$). Unfortunately *the discreteness itself eliminates completely lossless solutions*. More exactly, mathematical solutions for discrete LJJs are mixture of vortices with electromagnetic waves [14]. These waves actively interact and, in particular, resonate on discrete components [15]. Another feature to be aware of is "acoustical" vibrations of vortices that are similar to the vibrations of a chain of masses connected by springs (Fig. 2b).

B. Static properties of LJJs

Measurement of the energy dissipation in LJJ and nSQUID based circuits is quite straightforward. As we mentioned in the previous papers [17] it can be reduced to direct measurement of

DC bias current *I*. Such unique simplicity is explained by the Josephson voltage to frequency relationship that connects the voltage drop with the clock frequency and therefore excludes the voltage drop from equation for dissipated energy

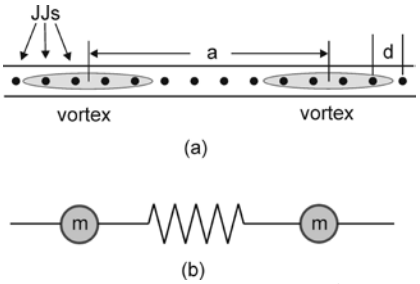

Fig. 2. Geometry (a) and mechanical model (b) [16] of the discrete LJJ.

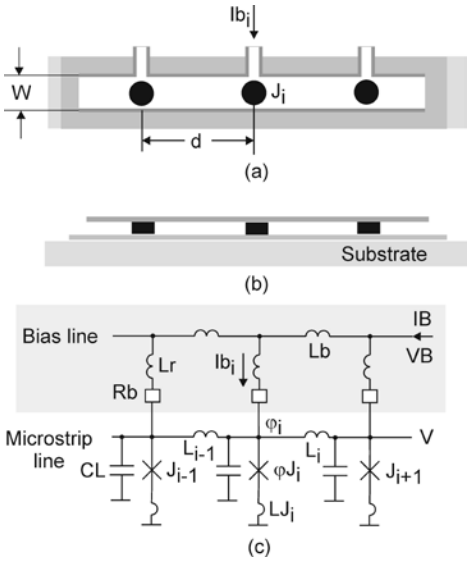

Fig. 3. Design (a, b) and equivalent circuit (c) of LJJ. Basic parameters could be as following: d=150 μm, W=12.6 μm, Ic=10 μA, L=4.44 pH, CL=378 fF, LJ=8.18 pH, Rb=0.7 Ohm.

$$E = I \cdot \Phi_0 \qquad (1)$$

This equation immediately gives the value of threshold current (per gate) that corresponds to the thermodynamic threshold current:

$$I_{th} = (\ln 2 / \Phi_0) \cdot k_B T \qquad (2)$$

Its numerical value at 4.2 K temperature is about 0.02 μA. Continuous uniform LJJs with vortices at low voltages have quasi-linear volt-current characteristics (without any critical currents). As a result, this device with vanishingly low currents at voltages approaching zero easily passes the reversibility test (2). However, as we mentioned earlier, the discreteness is able to spoil this unique advantage. Critical currents of discrete LJJs have been calculated many times. However, we did not find accurate analytical results and numerically calculated dependences of critical currents on dimensionless stage inductance β_L for an interesting range of vortex densities (Fig. 4). We calculated the depression of LJJ critical current caused by vortices. We measured the vortex density by the number of Josephson junctions per vortex period nJJ. (The current target vortex density lies between 8 and 9 junctions per vortex.) But to see a wider picture we carried out the calculations for a wider range of vortex densities. We also show (dashed line) analytical result (at $A = 626$) that has been originally derived for large distances between the vortices [18]

$$I_D = A \exp(-\pi^2 / \sqrt{\beta_L}) . \qquad (3)$$

There is a known technique dealing with Peierls-Nabarro potential [14] that could be used, particular, for calculations of critical current depression but we still could not find analytical results covering our range of parameters. This is especially true for the more favorable for us incommensurable number of junctions per vortex [19]. The upper plot (Fig. 4a) corresponds to a conventional LJJ with vanishingly low inductances LJ connected in series with Josephson junctions.

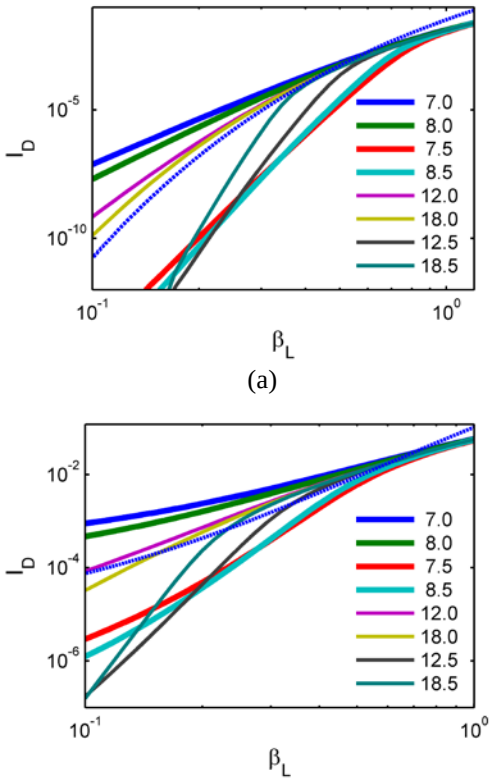

Fig. 4. Dependences of critical current of LJJ normalized on total critical current of all junctions on β_L. Different lines correspond to different magnetic fields shown as the numbers of junctions per vortex period. Dependences are calculated for vanishingly low LJ (a) and for $\beta_{LJ} = 0.3$ (b).

A depression of the LJJ critical current to about 10^{-3} of its value measured without Josephson vortices inside approximately corresponds to threshold bias current (2) per junction. Our target for the depression of the critical current is currently about 10^{-4}. Figure 4a shows that this level of depression corresponds to easily achievable β_L ranging from 0.4 for nJJ=8 to 0.6 for nJJ=8.5.

nSQUIDs are approximated by Josephson junctions connected in series with a relatively large ($\beta_{LJ} \cong 0.3$) inductance LJ. The lower plot (Fig. 4b) shows critical current depressions calculated for this β_{LJ}. Just to simplify our engineering we searched for the best approximation similar to (3) but with some effective inductance needed for calculation of

β_L presented as

$$Leff = L + \alpha LJ \quad (4)$$

The dashed line in Fig. 4b corresponds to $\alpha = 0.96$. According to Fig. 4b dimensionless inductance $\beta_L = 0.2$ at nJJ=8.5 depresses critical current 10,000 times.

C. Dynamic properties of LJJs

Measurements of dynamic properties are easier than their numerical simulations. We designed several versions of ring LJJs that have been fabricated at HYPRES, Inc. [20]. We report here measurement of circuits fabricated with a custom process with 1 kA/cm^2 critical current density for Josephson junctions and with 2 Ohm sheet resistance for main resistive layer. Ring LJJ shown in Fig. 5 contains 77 Josephson junctions.

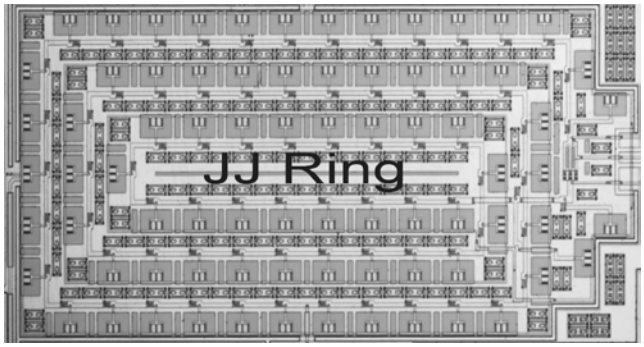

Fig. 5. Fragment of IC with ring LJJ.

We measured current-voltage (IV) curves at different numbers of vortices that could be changed using a built-in vortex pump. The IV curve without vortices (Fig. 6a) is similar to those of a conventional tunnel junction with about 0.7 mA critical current. The IVs measured with injected vortices are rather messy. However their operation areas at low voltages and large numbers of vortices (Fig. 6b) are more regular and rather close to our expectations.

The most distinguished feature of the curves in Fig. 6b is the low (about 0.1 mA) heights of their tallest points corresponding to vortices travelling with about Swihart speeds. Such low heights contradict simple theories assuming a motion of uniform vortex grid with a constant speed. More exactly, peak heights in such theories (see, for example, [21]) should be about as high as 0.7 mA corresponding to the cumulative critical current to of all junctions in the ring.

The discovered deviation from the theory is caused solely by the implemented biasing technique shown in Fig. 3c. The correct heights of the peaks could be estimated in the frameworks of old theories. This is because low value bias resistors Rb acts similarly to subgap junction resistance. However, they are connected not with the ground plane but with the terminal with another voltage very close to measured voltage *V*. If we discount by bias inductances Lr and Lb shown in Fig. 3c then the dynamic impacts of bias resistors could be taken into account by a modification of subgap resistance to parallel connection of bias and real subgap resistances. As the last step we should withdraw nonexistent dc current flowing via bias resistor from the numerically obtained $I(V)$:

$$I(V) \to I(V) - V / Rb. \quad (5)$$

The results of these calculations (dashed lines Fig. 6b) reasonably match the experimental data. However, the numerical values of bias resistors corresponding to the best match are about 7 times higher their real values. This mismatch is because of neglected inductances Lr and Lb that, in fact, rather effectively attenuate ac currents.

The numerical values of resonant voltages correspond to the periodic motion of vortices along the ring with Swihart speed. Indeed, the voltage drop corresponding to rotation of a single vortex along the ring with Swihart speed is about 15 μV. This voltage drop grows proportionally to the number of travelling vortices and resonances observed at 9, 10 and 11 vortices to be expected at 135 μV, 150 μV and 165 μV. Besides, we definitely see "permanent" resonances at

$$Vm = \frac{\Phi_0}{\pi\sqrt{LC}} \sin(m\pi / N), \quad (6)$$

where L and C are inductance and capacitance of a single stage, *m* is the resonance number and *N*=77 is the number of stages in the ring. This formula is a simplified revision of several different formulas that can be found in [22]. The next important observation is a definitely more regular resonant structure at 11 vortices in the ring. This is because this case corresponds to an integer (seven) number of Josephson junctions per vortex period. The mentioned peculiarities are discussed in detail, for example, in [19], [22]. The peculiarities serve us as extremely valuable diagnostic tools; however, they are not important for circuit operation. This is because at this time we plan to operate our circuits at sufficiently slow clock frequencies. The lowest observed resonance takes place at about 15 μV or about 7 GHz clock frequency.

The observed 10 μA to 20 μA critical currents of the ring correspond to 0.13 μA to 0.26 μA per stage and still exceed the threshold. But we are satisfied with these results because after the experimentation with the circuit we indentified several parasitic factors. The most intuitive explanation would be a fabrication spread of critical currents. However, this explanation does not work because several copies of the chip showed similar results. The next simplest explanation is flux trapped in the ground plane. This is closer to reality because the measurement results are somehow different after each thermo-cycle and we show the best collected after about 20 thermo-cycles. We also found several design irregularities. In particular, not all inductances L and LJ (see Fig. 3) are identical. Then there are several irregularities responsible for the dynamics of the circuits. The biggest is caused by the vortex injector. We supposed that in a passive mode it could behave as a regular LJJ section. But the injector capacitance is 3 times larger than capacitances of regular sections. Besides, there are unaccounted capacitances of wires that are needed to apply the bias current and to measure the voltage.

But the greatest mistake is because of irregularities of the bias distribution scheme highlighted by light gray in Fig. 3c. Our idea was to make bias resistors as low as possible. The idea of low bias resistors by itself is not new, see for example [23]. But it is perfectly good for us because of purely periodic processes in biased junctions. Moreover, due to the dense

location of the vortices the AC voltage component is lower than those for a stand-alone unshunted Josephson junction. As a result, we can assume that the value of bias resistance may approach zero.

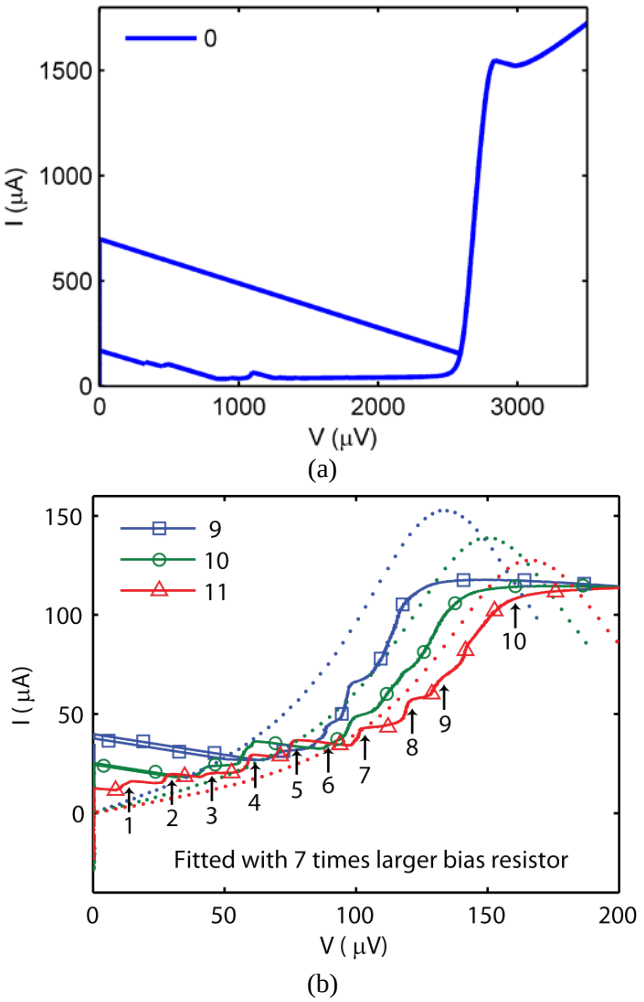

Fig. 6. Voltage-current characteristics of the ring LJJ measured (a) at 0 and (b) at 9, 10 and 11 injected vortices. Negative slopes are caused by a resistive bias current divider with 4.7 Ohm "load" resistance.

However, in this extreme case of "zero" bias resistors the inductances of the power distribution system (grey area in Fig. 3c) become parts of clock line shown below in Fig. 3c. To reduce the impact of power distribution inductances we keep them large. However, they are not large enough and unfortunately we did not keep them equal.

III. nSQUID Circuitry

The nSQUID circuits currently in use were introduced at the last ASC [18] and ISEC [24] conferences. But at that time the measurements were spoiled by parasitic coupling of a SQIF sensor of bias current with high-current auxiliary circuitry. The problem has been identified and solved. Below we refresh details that are necessary to explain our new results.

A string of nSQUIDs (Fig. 7) is similar to the LJJ discussed above but with Josephson junctions replaced by nSQUIDs. Each nSQUID [18] is a 2-junction SQUID with a negative mutual inductance between its inductive arms. This negative mutual inductance resolves the two conflicting requirements for the two degrees of freedom of the system [18]. In a common mode, which represents common dynamics of the two-junction SQUIDs, one would like to keep the low effective inductance ($\beta_l \sim 0.3$), and therefore, simple dynamics of this mode governed by the current bias of the junctions via the clock line. For the differential mode, which represents the current circulating along the SQUID arms, one needs to provide a larger effective inductance ($\beta_l \sim 1.4$), so that there are two stable states possible in this degree of freedom.

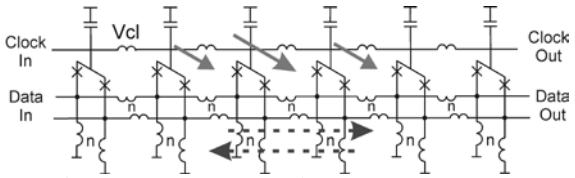

Fig. 7 Data flow diagram in a string of nSQUIDs coupled through pairs of inductive strips with negative mutual inductance between them.

The low ($\beta_l \approx 0.3$) inductance of the common mode of the strings of nSQUIDs connected as in Fig. 7, implies that the strings support propagation of vortices along the strings as in LJJ. (This low inductance connected in series with Josephson junctions is already included into the analyzed (Fig. 4b) and measured (Fig. 6) LJJs.)

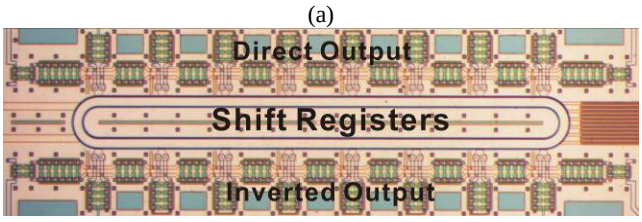

Fig. 8. (a) Equivalent circuit, and (b) the microphotograph of 2 shift registers with a common clock ring. Note that the lower register contains one inverting wire connection and therefore inverts the data. The length of one cell is 180 μm, the length of the ring is 1410 μm. Only 6 of 8 cells are shown in schematics (a).

The main difference between the LJJs and nSQUIDs is that the nSQUIDs located near the current centers of the moving vortices experience approximately $\Phi_0/2$, i.e. π, magnetic (clock) bias and therefore find themselves in one of the two stable states that can be distinguished by the sign of the current circulating along the nSQUID. Because of the relatively strong magnetic coupling of the nearest-neighbor nSQUIDs in the string (Fig. 7), all nSQUIDs which belong to one vortex share the same logic state. This state can be naturally used to carry

one bit (“0” and “1”) of logic (digital) data.

We have eliminated the dissipation of energy in the shunt resistors and diminish bias voltage in LJJs to nano-volt level. For this relatively short circuit bias resistors have been completely eliminated. There is still, however, a considerable energy flow associated with the clock vortices themselves. To avoid dissipating this energy, the vortices, together with their energy, can be “recycled”, e.g., by connecting the clock lines of the two shift registers to form a ring as shown in Fig. 8. The dynamics of vortices in this structure are similar to the vortex motion in ring LJJs discussed above.

Figure 9 illustrates the measured digitization effect: at lower values of the analog input signal, the digital output shows constant (digital) output corresponding to a negative differential state of the nSQUIDs (logical “0”), while at higher input signal, the differential state is positive (logical “1”). The overall process, viewed as “calculation”, is rather simple. It involves 3 primitive functions: writing bits of data into a shift register, propagating them by about 2 mm distance, and reading them out.

As we mentioned earlier, the measurement of the energy dissipation is reduced to measurement of the bias current (Fig. 10). The lower plot shows variations of this current within the whole range of clock frequencies, while the upper plot blows up the range of frequencies when bias current reaches its lowest values slightly below 0.1 μA. This is current applied to both 8-stage shift registers or to 16 nSQUIDs. If we suggest that each register is a logic gate consuming 0.05 μA of bias current then the energy dissipation is still 2.5 times higher than its thermodynamic threshold. But each nSQUID could be treated as a gate that consumes only 0.007 μA of current or dissipates per operation *less than one third of the threshold energy* (2). These figures are close to our expectations for this particular circuit.

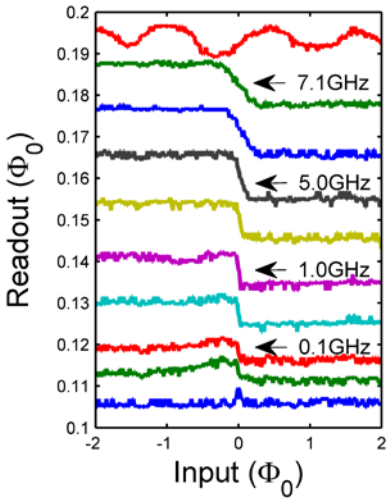

Fig. 9. Digitization and propagation of the digitized data along the shift register. From bottom to top, clock frequencies are 0, 0.05, 0.1, 0.5, 1.0, 4.0, 5.0, 6.1, 7.1 and 8.1 GHz. Analog input magnetic flux is created by current Iin, Digitized output is extracted at the other end of the register by the readout SQUID.

IV. Discussion

We demonstrated all nontrivial single-input logic functions: F=A and F=NOT(A). Definitely they are still functionally incomplete. Usually functional completeness is achieved by adding to the set one two-input function. However, earlier [6] we have shown that parametric quantron and therefore nSQUID gates are more suited to execute less common but more valuable three-input 2/3 majority function. The majority gate being used with inverter (NOT) offers a functionally complete set of logic functions. Let us remind that majority function M(A,B,C) returns the value as those of majority (at least 2) inputs data. Three-input M gate is converted to two-input OR or AND gates by applying to the third input permanent logic “1” or “0” signals.

We like to show the next prospective circuit that if successful definitely could be treated as a digital reversible integrated circuit (Fig. 11). It looks like the timing belt (Fig. 1a) but with 13 junctions replaced by nSQUIDs. Positively and negatively magnetically shifted nSQUIDs performing OR and AND functions are shown as diamonds and squares, while unbiased nSQUIDs used in the shift registers are shown as circles. Single and double lines indicate a weaker and two-times stronger data coupling between the gates. Crossed data lines mark NOT function that is implemented by twisting straight signal wires shown in Fig. 8a. In fact E=XOR(A, B) is calculated in 3 steps: C=(NOT(A) AND B), D=(A AND NOT(B)), E=(C OR D). The rest of the gates perform buffer functions and under certain circumstances could be omitted. “Timing belt” connections inside the XOR gate are shown as wide grey lines. Ellipses are symbolic notations for timing vortices travelling along the belt.

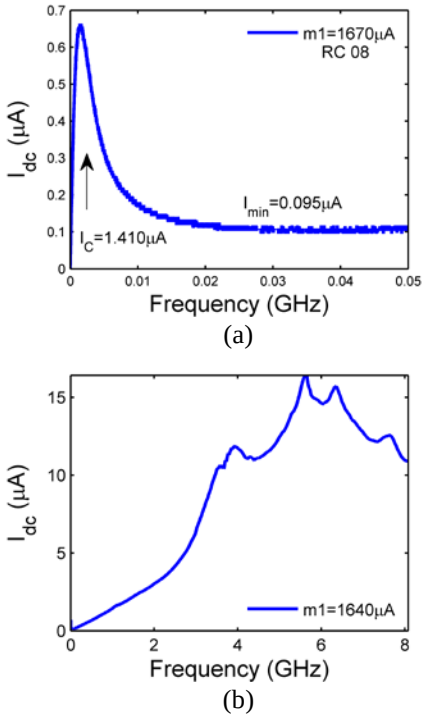

Fig. 10. Measurements of the energy dissipated in the nSQUID shift registers. The sample RC08 is fabricated using 30A/cm^2 technology.

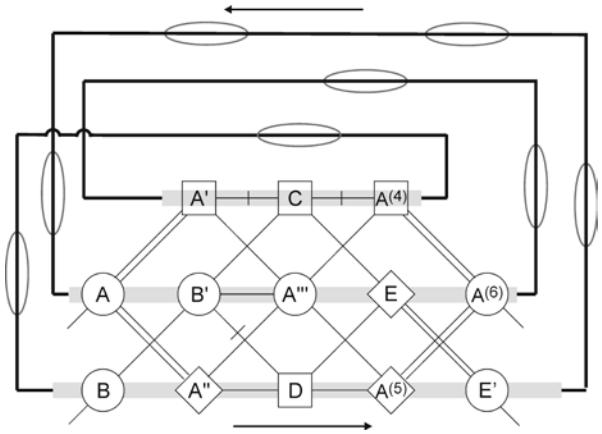

Fig. 11. Structure and timing of a test circuit with the reversible XOR gate. Long JJs clock lines are shown by solid black lines with gray ellipses showing moving Josephson vortices. Clock lines in nSQUID grid are shown in light grey.

Most of the mentioned components have already been tested and we do not expect new big problems. Here we would like to highlight the main advantage of the new timing scheme in comparison, for example, with multi-phase AC bias. AC microwaves unavoidably are attenuated and distorted while they are propagating along the chip. Moreover, the mentioned attenuation and distortion could be data dependent. In contrast, the vortex timing belt is fundamentally accurate. It can be stopped and run again and *its states before and after a rotation for any integer number of vortex periods are fundamentally indistinguishable*. One can say that this is a rare example of a timing scheme potentially free of clock skews. As we mentioned earlier the speed of the timing belt rotation could be extremely stable [13].

V. Conclusion

Superconductor electronics has been competing with semiconductors for decades. The first superconductor 50 μs speed record was established in 1954; and in 1999 it reached 1.3 ps (or more exactly a T flip-flop operating up to 770 GHz has been reported [25]). It is perhaps symbolic that there is an overlapping author in [25] and in a semiconductor paper reporting record (100 GHz) speed demonstrated with SiGe T flip-flop [26]. So the superconductors won the speed race. This success was sufficient for some niche applications such as satellite communications [27]. However, the clock rate of modern high-end computers is "artificially" reduced because it is less important than numerous technical and economic requirements. Probably the strongest requirement is to keep low specific energy dissipation. Unfortunately some advantages of conventional RSFQ circuitry in specific energy dissipation are partly offset by low cooling efficiency and other complications related with the low operation temperature. It is natural to expect incremental improvements in energy efficiency for both semiconductor and superconductor circuits. Several such advanced superconductor techniques have been described in [28].

Our approach is fundamentally different. This is because we pretend that we drastically diminish all technical dissipation mechanisms to leave logical irreversibility as the main dissipation channel. As a result, we will be able to experimentally set the absolute record for low energy dissipation about few k_BT per binary operation. Any other prospective digital technology will only be able to repeat the record but never to beat it.

The promised few k_BT per irreversible operation are about 10^6 times less (if measured in k_BT units) or about 10^8 less (if measured in absolute values) than figures demonstrated at the state-of-the-art semiconductor technologies [28]. Such an impressive gain could not be wiped out by the cooling inefficiency. As a result, we do not see any emergency with a revision of known computer architectures to eliminate or even to reduce the number of irreversible operations in practical circuits. Moreover, the new SFL and RSFQ technologies including new ERSFQ/eSFQ families [28] are compatible and can be integrated on a single chip. Our next task is to demonstrate interfaces between SFL and eSFQ circuits. The hybrid SFL/eSFQ circuits would speed up the insertion and acceptance of new SFL technology.

However, it is vitally important to demonstrate several reversible circuits with energy dissipation well below the thermodynamic threshold. These demonstrations would serve as solid proof that we, indeed, reduced the cumulative impacts of all other dissipation mechanisms below the thermodynamic threshold.

Besides, crossing any fundamental threshold is psychologically important because it allows us to see things differently. For example, the impossibility of reversible computation is a statement that can be easily found in road maps and assessments. We would like to render this statement obsolete. Finally, we think that reversible circuits could serve as natural prototypes of prospective quantum computers.

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