Paper based on this presentation was published by Superconductor Science & Technology (SuST, IOP) 27, No. 4, 044018 (2014)

SuNAM developed new process named RCE-DR:

The practical highest throughput process

Seung Hyun Moon
SuNAM Co., Ltd.

2013. 9. 16.

EUCAS 2013
September 15 – 19, 2013, Genova, Italy

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Contents

- Introduction
  - Requirements from market : performance & price.
  - Strategy to achieve the requirements : throughput & yield
- RCE-DR : The highest throughput unique SuNAM's process
  - RCE-DR : Amorphous deposition & fast conversion at once.
  - Understandings of RCE-DR process
- SuNAM's results
- Summary

SuNAM

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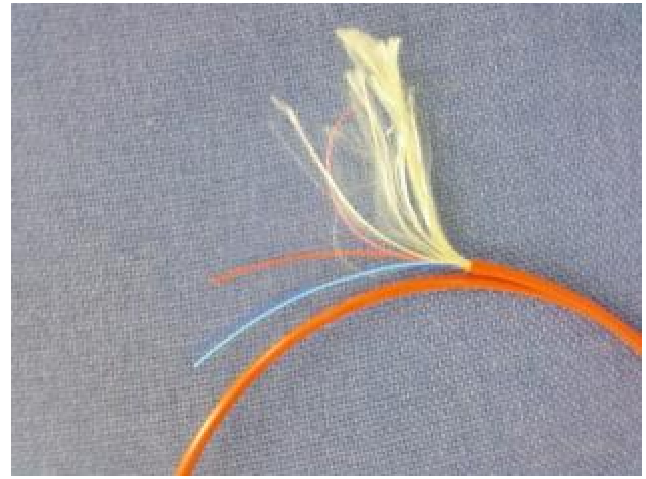
Paradigm change in Electrical Power Industry

In communication(or IT) industry,

Cu wire

vs.



Optical fiber

In electocal power industry,

Cu wire vs. HTS 2G wire

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Applications of Superconductivity

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For real industrialization, ..

- For practical application of HTS(high Tc superconductor) ceramic material, high performance and low cost conductor is essential .
- It's a big challenge to make a km long tape using coating technology, but almost all obstacles have been solved through years.
- And now the price & the availability of 2G wire is the real issue for industrialization. Not only material cost, but throughput and yield is the very important factors for practical wire production.

→ **" Throughput" & "Yield"**

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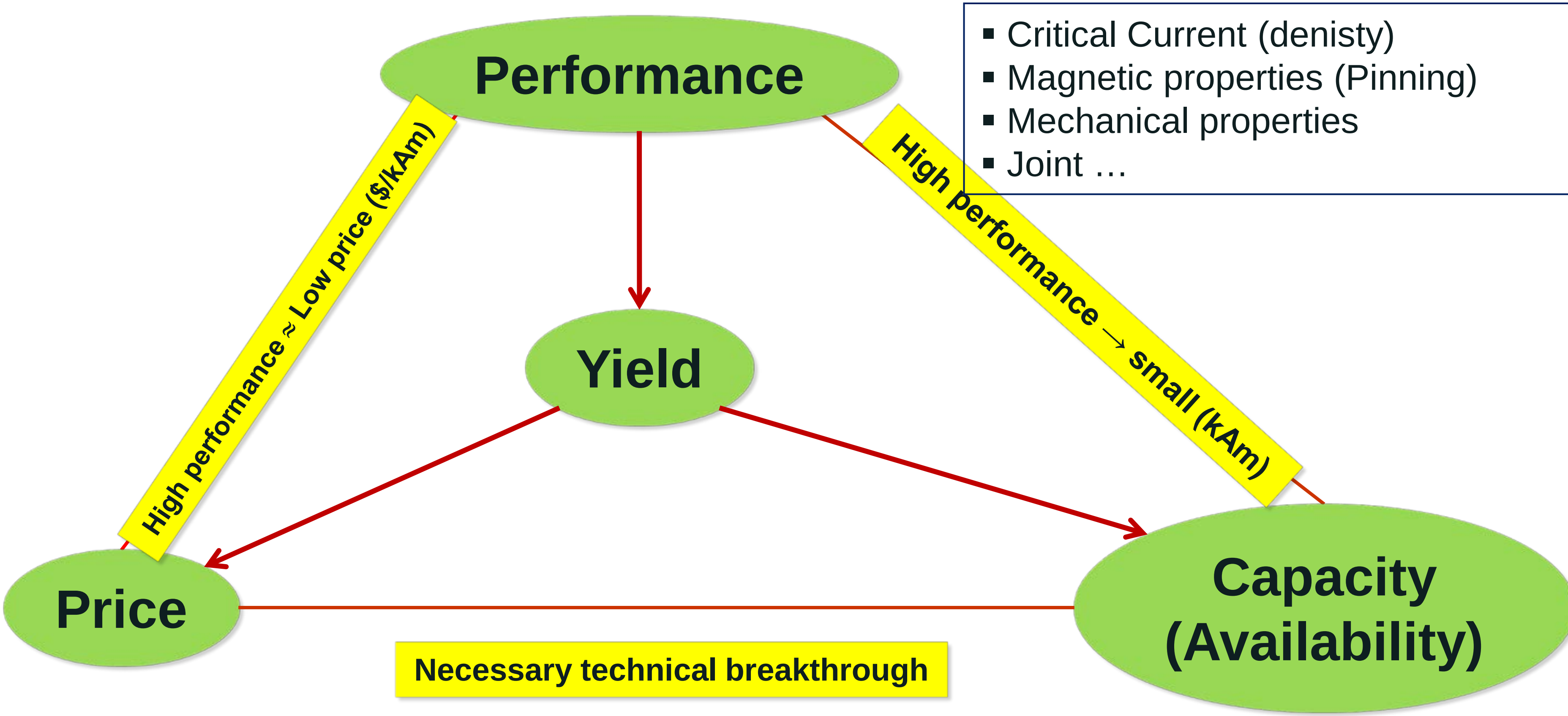
Complex problem of Performance, Price and Capacity

- Critical Current (denisty)
- Magnetic properties (Pinning)
- Mechanical properties
- Joint …



- Simplified process
- New process
- Wide web compatible process
- Large volume (> 10,000 km/yr-line)

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Which process should we develop?

- Total Cost = Equipments + Labor + Materials



- Cost /length = Total cost / Total production length
- Total production length = Throughput X Time X Yield
- Low materials cost
- High Throughput
- Engineering / Q.C for high Yield

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Cost Analysis : what's the limiting factor?

- Assume 500 A/cm-width CC & 4 mm width equivalent wire.
- Assume throughput/single line & 100 % yield.

Through - put (m/hr)	Run time/week (hrs)	Annual Production (km)	Equipment depreciation/ yr (M$)	Labor cost (M$)	(Depreciation + labor)/length	
					($/m)	($/kA-m)
50	60	150	1.5	1.5	20	100
100	100	500	2	2	8	40
500	60	1,500	2	2	2.7	13.3
3,000	100	15,000	4	4	0.53	2.7

- Considering yield, the minimum cost increases much higher value.
- In large volume case, material cost & yield is much more important.

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Price factors for HTS 2G Wire

- **Throughput means volume production rate.**

- P = A (processing area) x R (thickness growth rate)

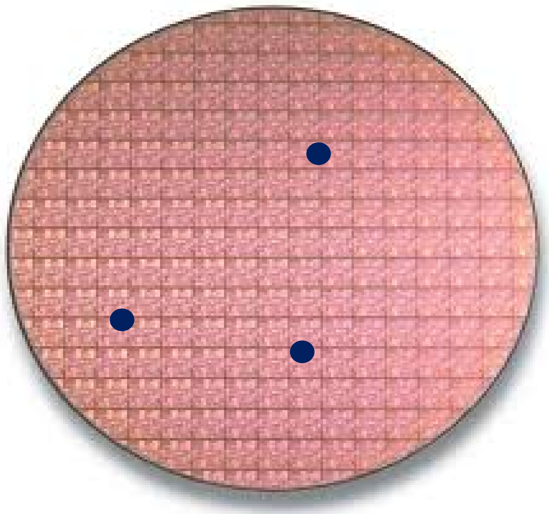
Wide web process.

- ➢ RCE DR : ~ 100 nm/sec or faster (SuNAM)
- ➢ PLD, MOCVD ~ 10 nm/sec, MOD ~ 1 nm/sec

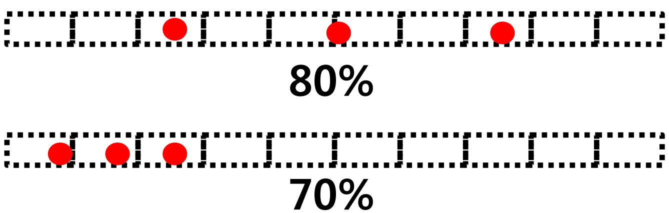
- RCE-DR process : easy to scale-up to wide strip.

SuNAM

Yield is too low?



- If we were to make 100 chips in a wafer, and there are 3 defects, yield can be as low as 97% (loss as high as 3 %) (at most, 88 %)



- If there are 3 defects in a 1 km wire and minimum piece-length is 100 m, yield can be as low as 70% (loss as high as 30 %)
- Thing get worse if customer wants longer piece-length wire
- Even though we reduce the defect density, customer's demand for ever-longer wire could over-'compensate' our efforts
- This yield 'trap' would persist until we reach 1 km defect-free wire(for many applications) or 2 km wire(for the most of the applications)
- Or, we need a new definition of yield for CC

- **Keep up QC(quality control) & develop new QC tools.**

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RCE- DR

(Reactive Co-Evaporation by Deposition & Reaction)

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Semi in-line pilot line for 2G wire



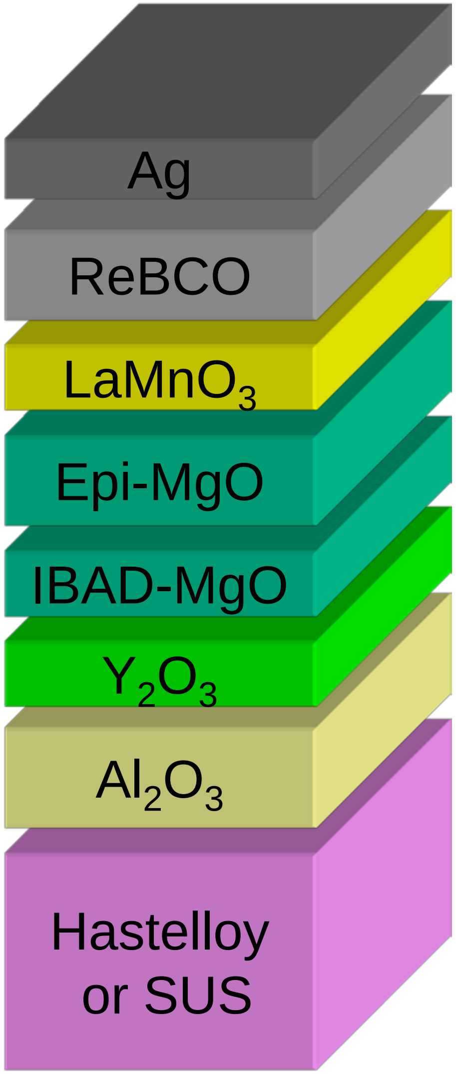



- Site area : 5,500 m^2, Building area : 1,750 m^2, Gross floor area : 3,050 m^2.
- Class < 10,000 clean room area : 1,000 m^2 .





SuNAM's 2G Wire Architecture – 12 mm width



Protecting layer (0.6 μm)	DC sputter
Superconducting layer (1.2 ~ 1.8 μm)	RCE-DR
Buffer layer ~20 nm	sputter
Homoepi-MgO layer ~ 20 nm IBAD-MgO layer ~ 10 nm Seed layer (Y_2O_3) ~ 7 nm Diffusion barrier (Al_2O_3) ~ 40 nm	IBAD (sputter & E-beam)
Hastelloy C276 (Ni-alloy tape) or Stainless Steel-tape	Electro -polishing

or SDP (Solution Deposition Planarization)

(+ Cu electroplating (+ lamination))

* Linear speed of each process : 120 m/hr or more.

- Typical I_c ~ > 600 A/12 mm at 77 K self-field (J_c ~ > 4 MA/cm^2)

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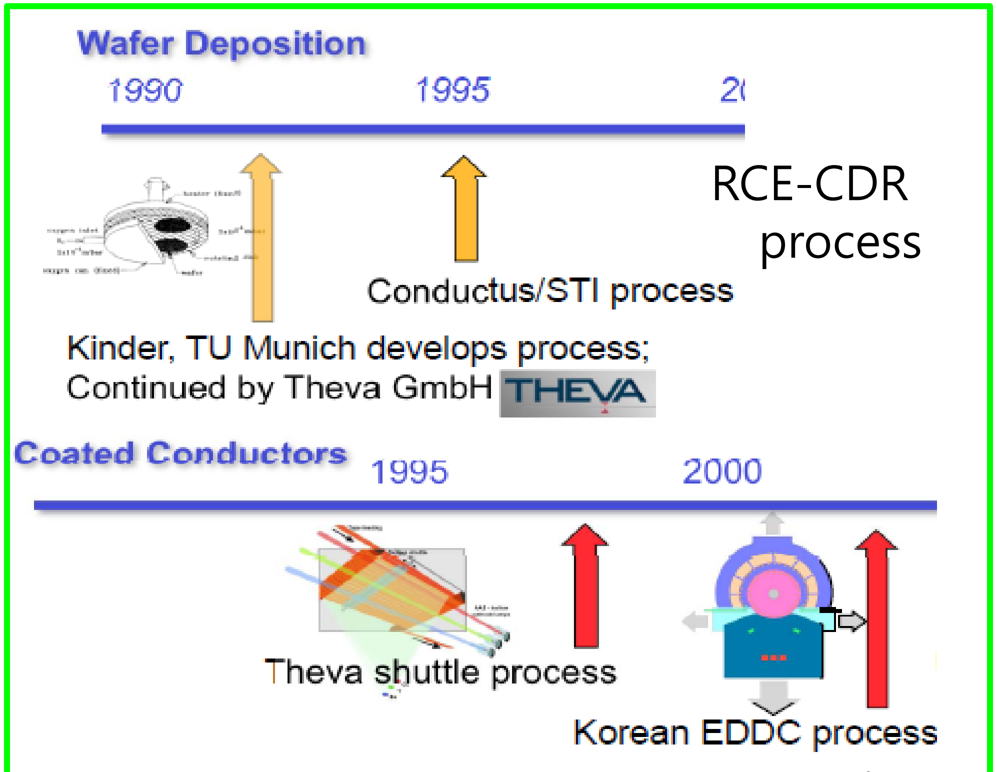
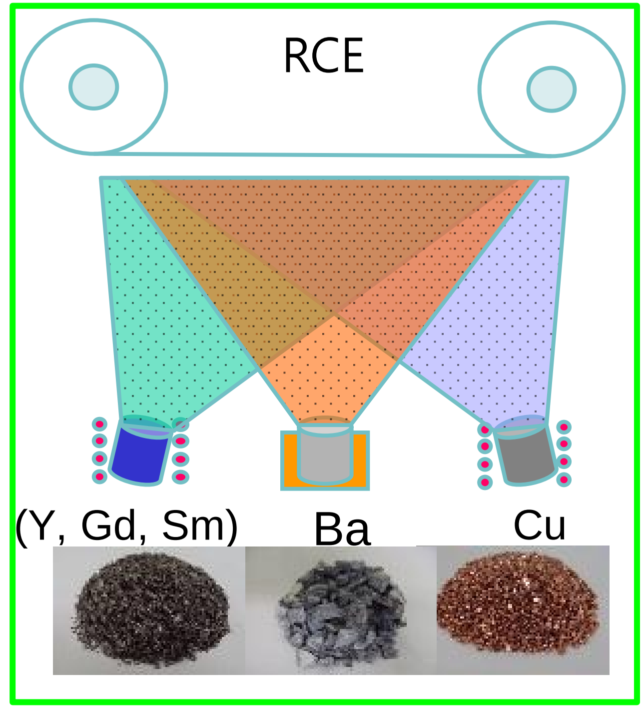
RCE process

- Reactive Co-Evaporation (RCE) :
  - Using inherently least expensive sources
  - High deposition rate can be used & adjustable composition
  - Especially easy to scalable to large deposition area
  - Very promising methods for HTS wafer production : Theva, STI





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SuNAM develops RCE-DR process.

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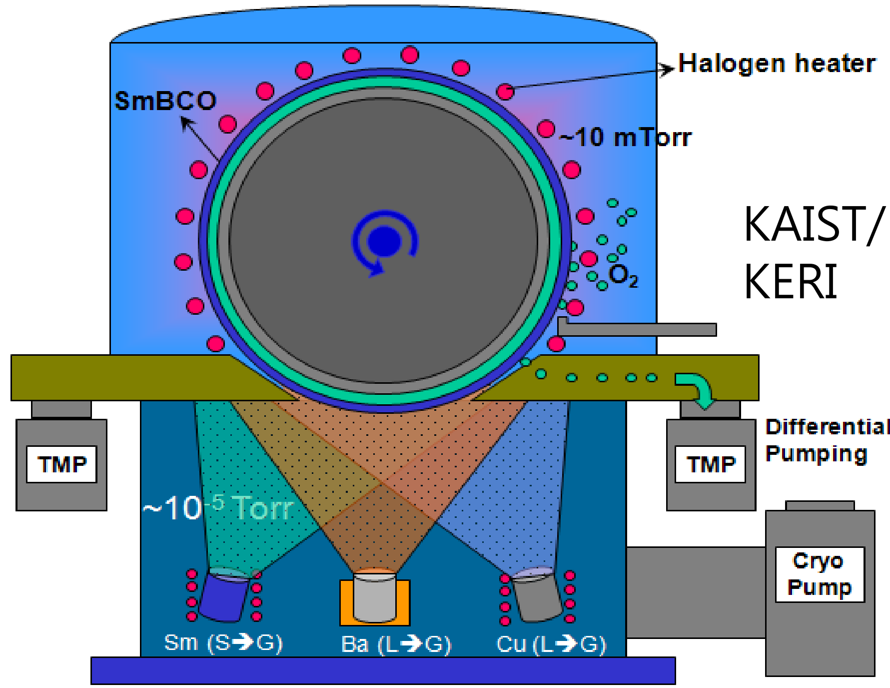
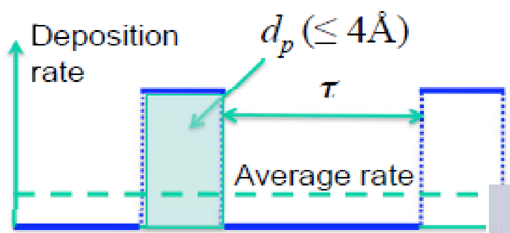
Conventional RCE-CDR process

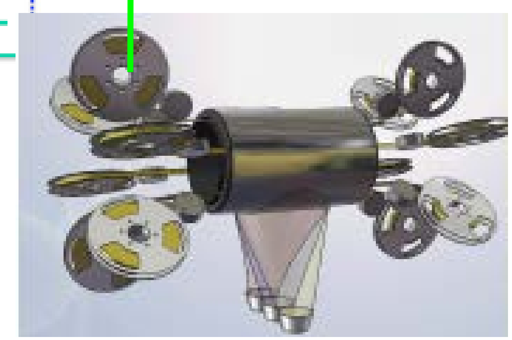
- RCE-CDR : Reactive Co-Evaporation by Cyclic Deposition & Reaction (EDDC(KAIST/ KERI, batch) & STI, R2R(planned))
- CDR : Co-evaporation at low O_2 pressure followed by reaction in high PO_2 in cyclic manner.
- Pulsed deposition : low average growth rate.
- High speed(> 100 rpm), high temperature(> 800 °C) mechanically rotated drum is required : complexity, cost, difficult to scale up



KAIST/
KERI



Massive(> 100's of kg on scale-up)



LANL/
STI

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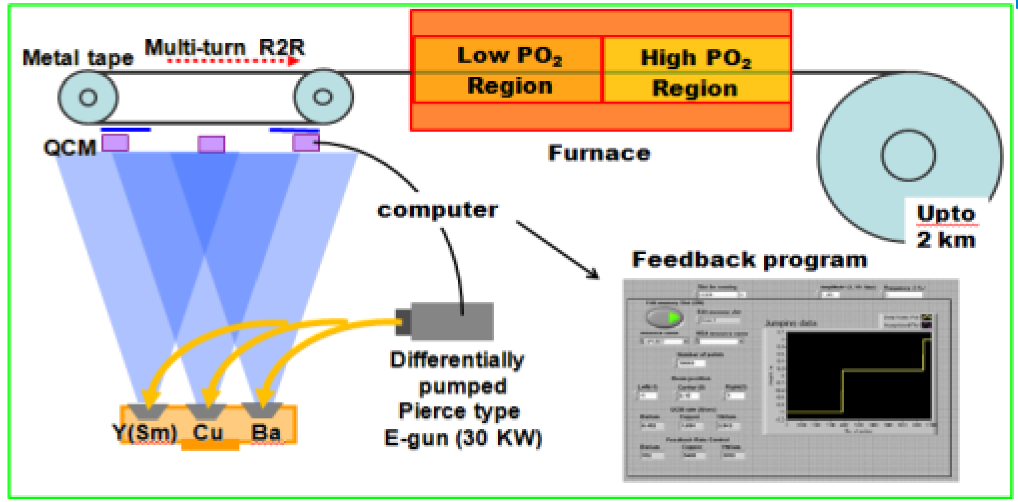
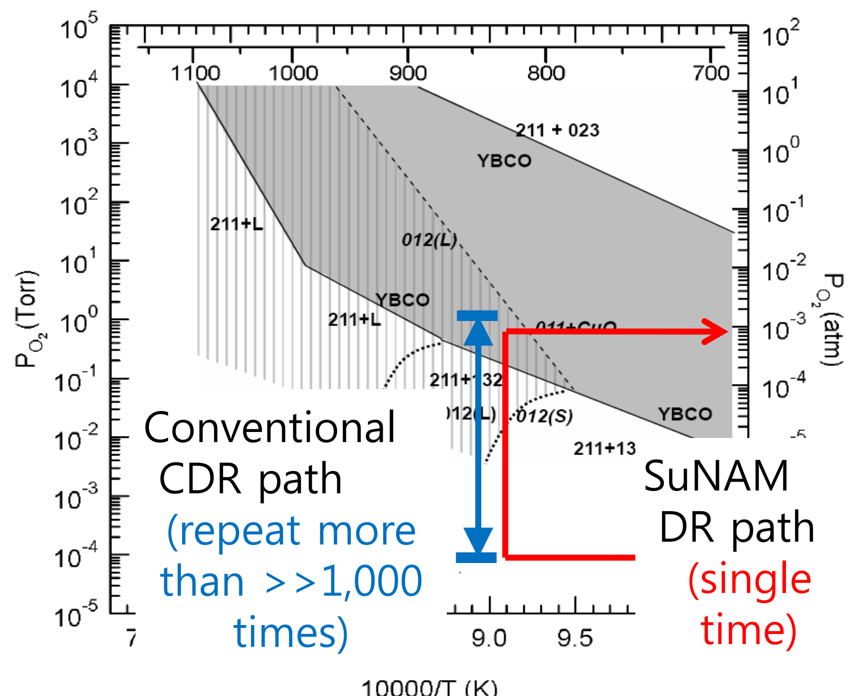
New SuNAM RCE-DR process

- RCE-DR : Reactive Co-Evaporation by Deposition & Reaction (SuNAM, R2R) : Patent pending(PCT)
- High rate co-evaporation at low temperature & pressure to the target thickness(> 1 μm) at once in deposition zone (6 ~ 10nm/s)
- Fast (<< 30 sec.) conversion from amorphous glassy phase to superconducting phase at high temperature and oxygen pressure in reaction zone
- Simple, higher deposition rate & area, low system cost
- Easy to scale up :single path





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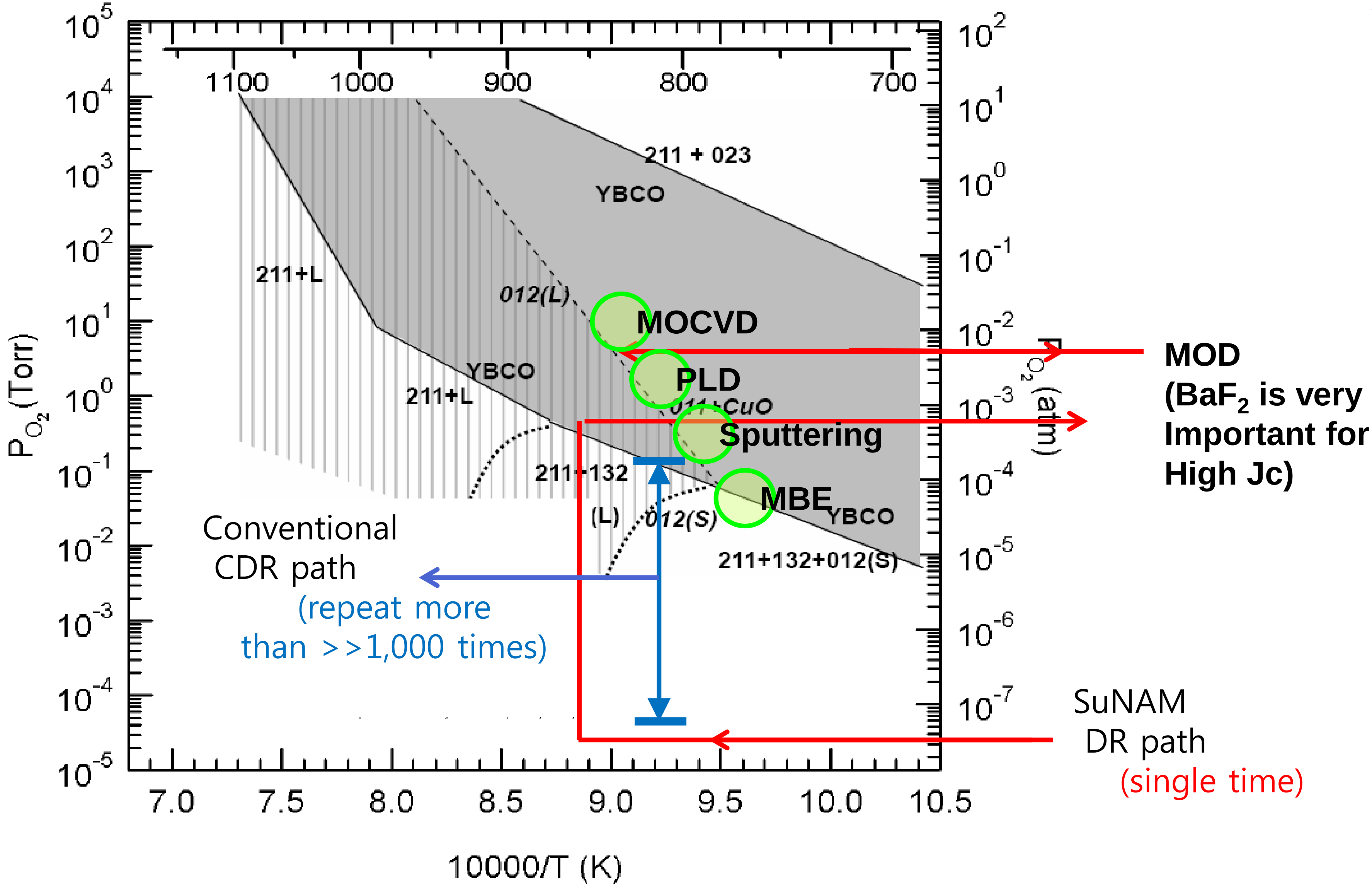
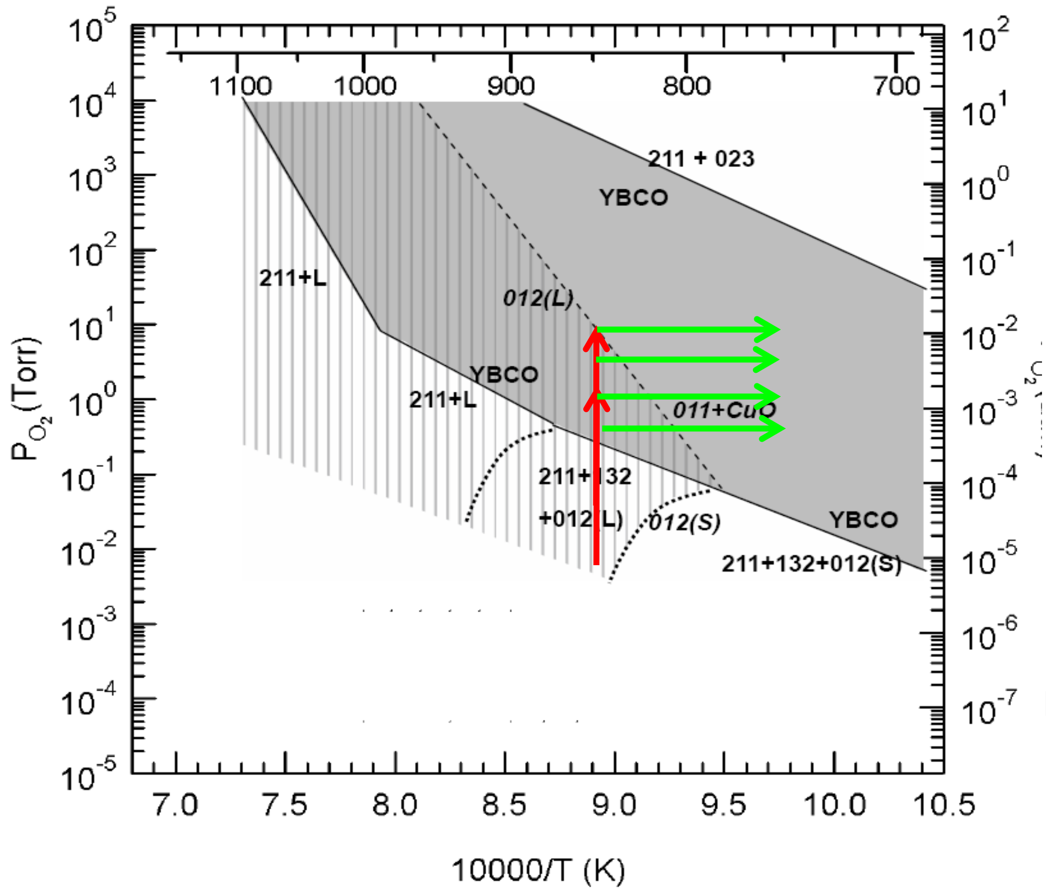
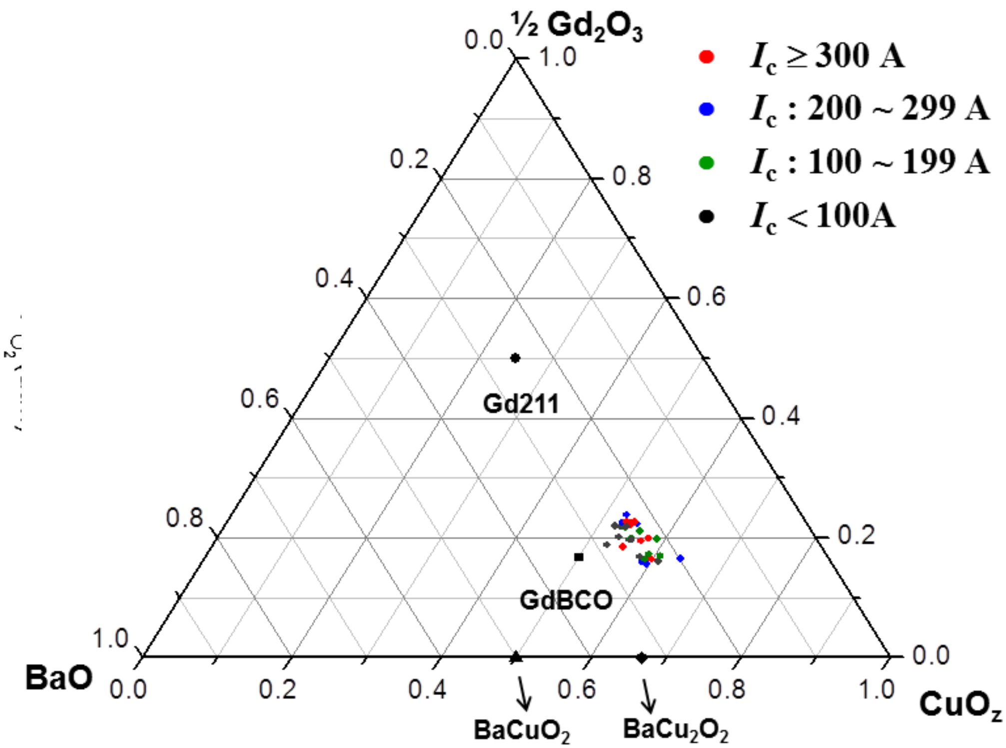
Comparison of various deposition methods



Paper based on this presentation was published by Superconductor Science & Technology (SuST, IOP) 27, No. 4, 044018 (2014)

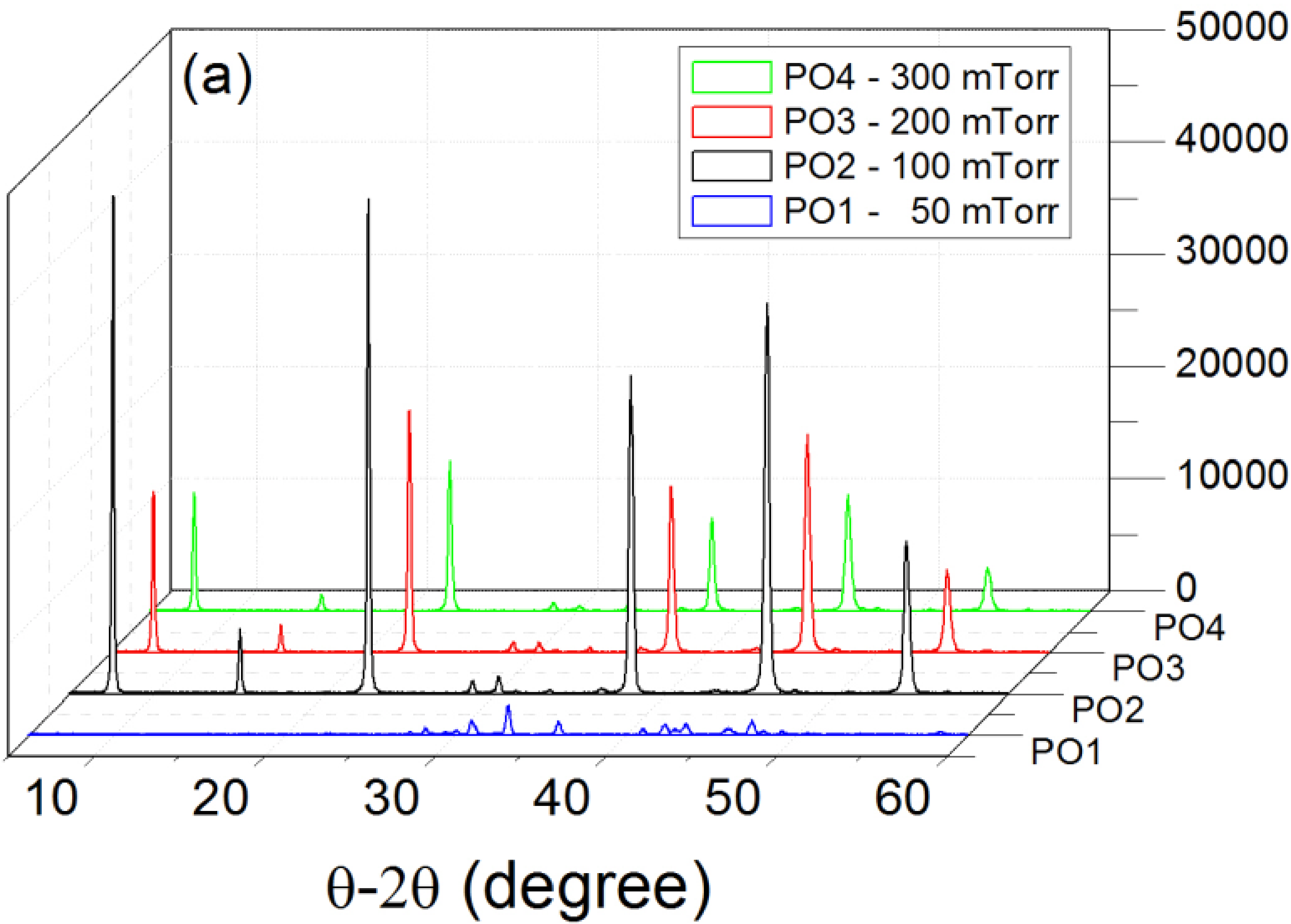
RCE – DR Process : Phase Diagram





- Understanding of phase diagram at low PO_2
- Liquid phase is very important

RCE – DR Results : XRD θ-2θ



- **The same batch, PO_2 increases.**

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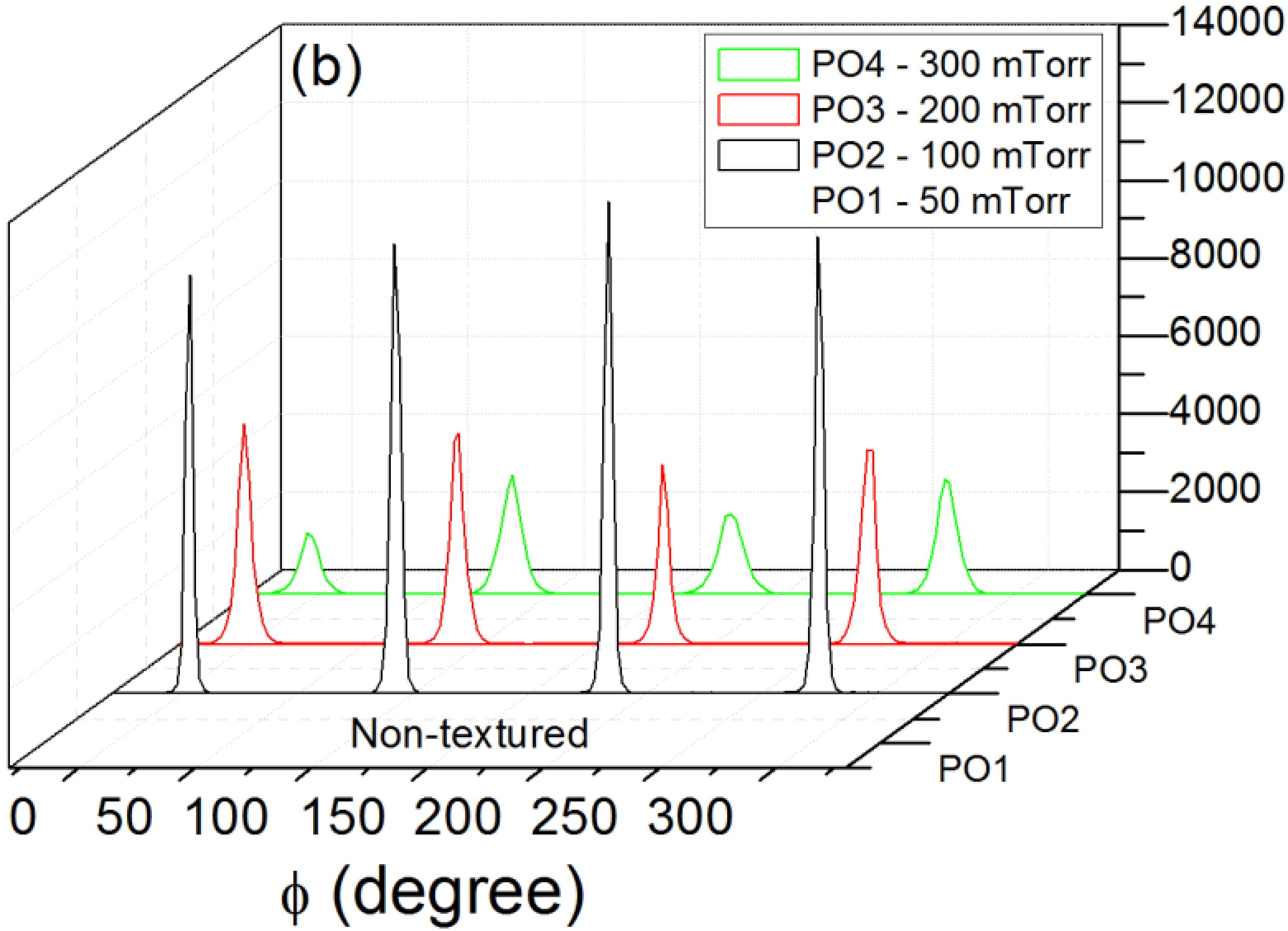
RCE – DR Results : XRD ϕ-scan (103)



- The same batch, PO_2 increases.

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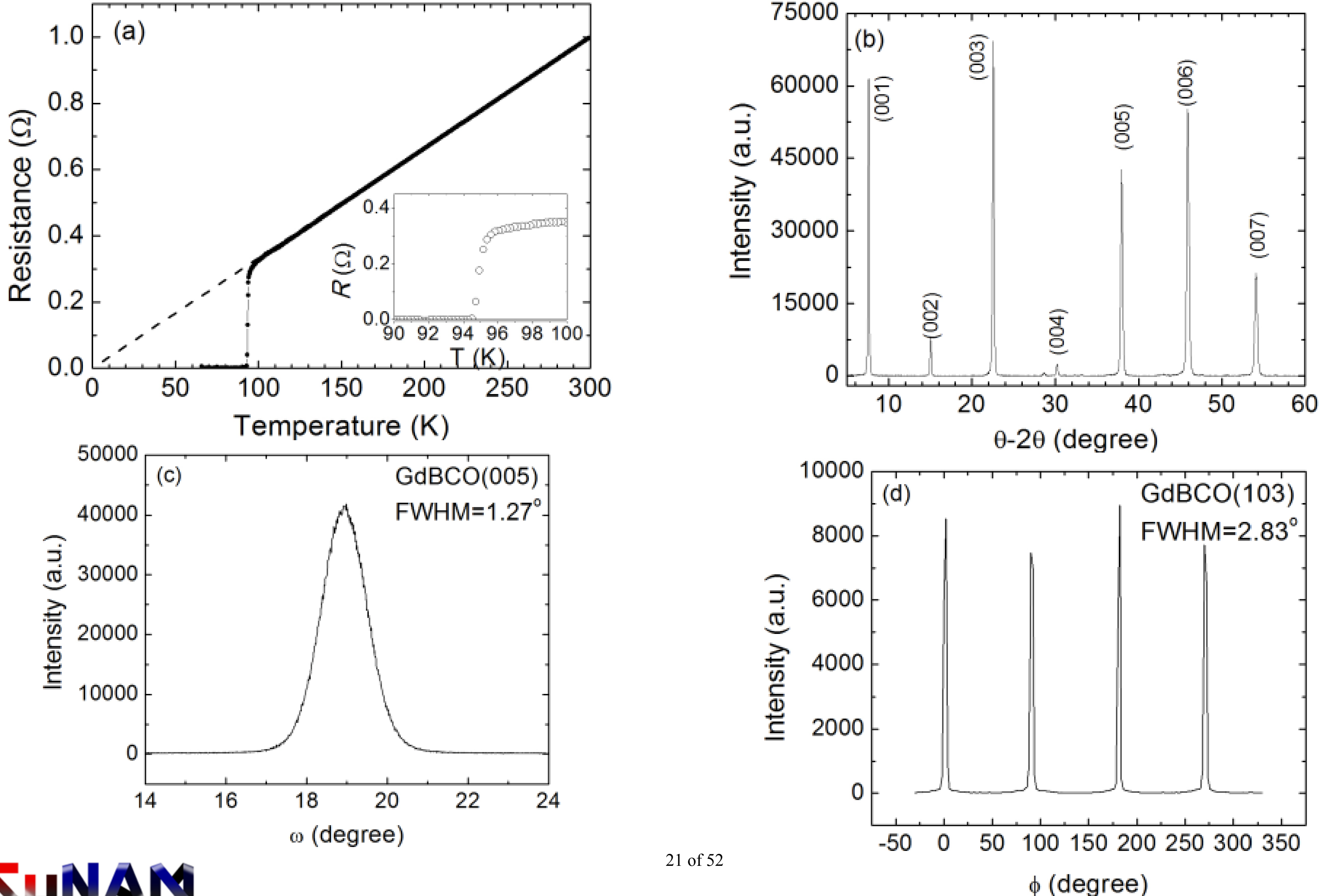
R-T & XRD for optimized tape by RCE – DR



Stability phase diagram of GdBCO

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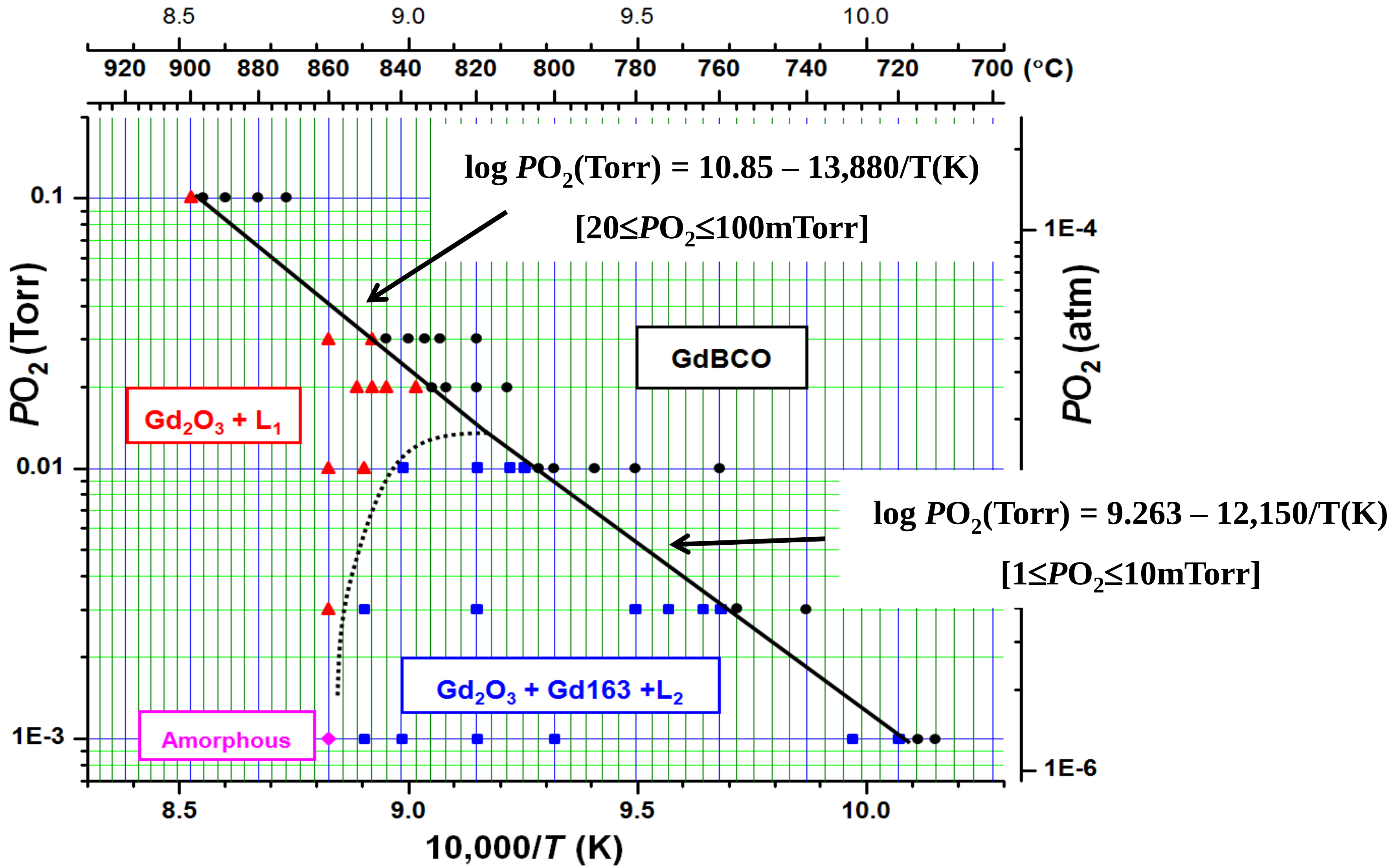

Our understanding of Gd123 Phase diagram

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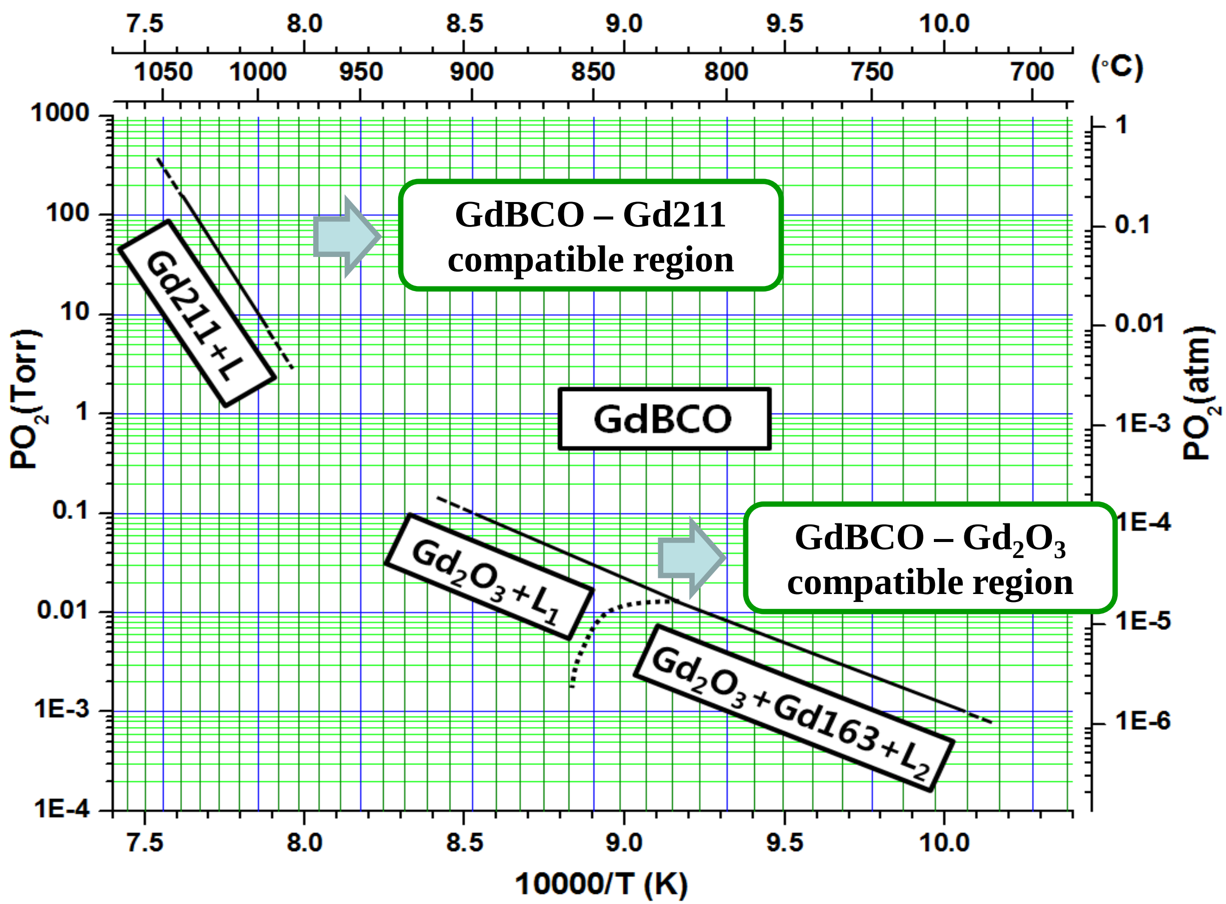

Growth mechanism of the GdBCO film by RCE-DR

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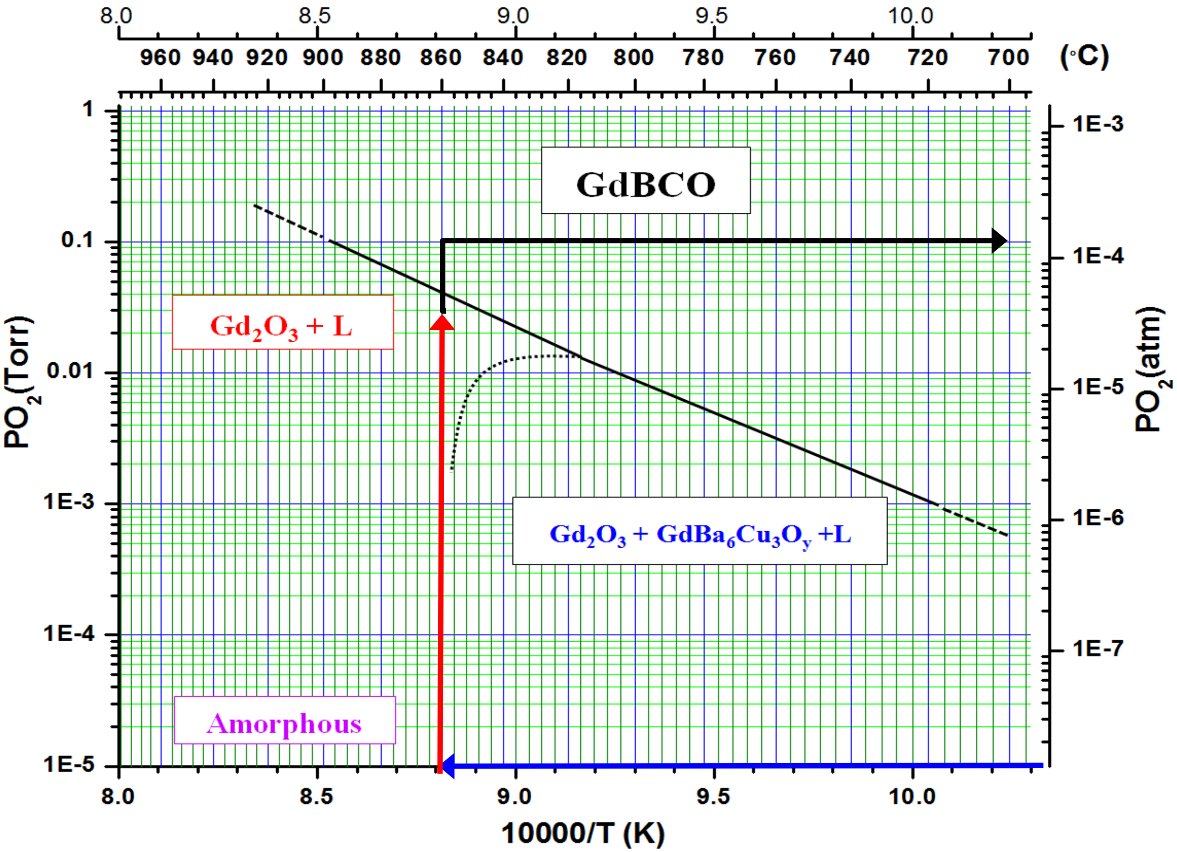

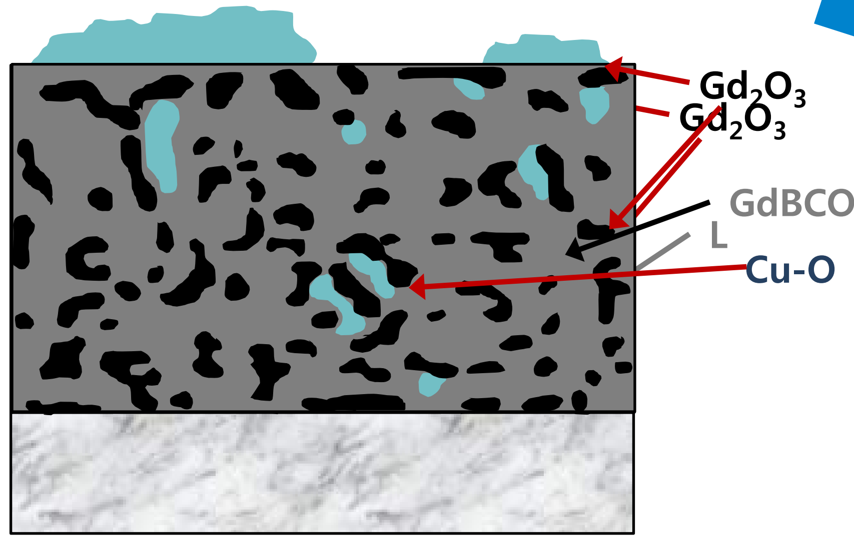

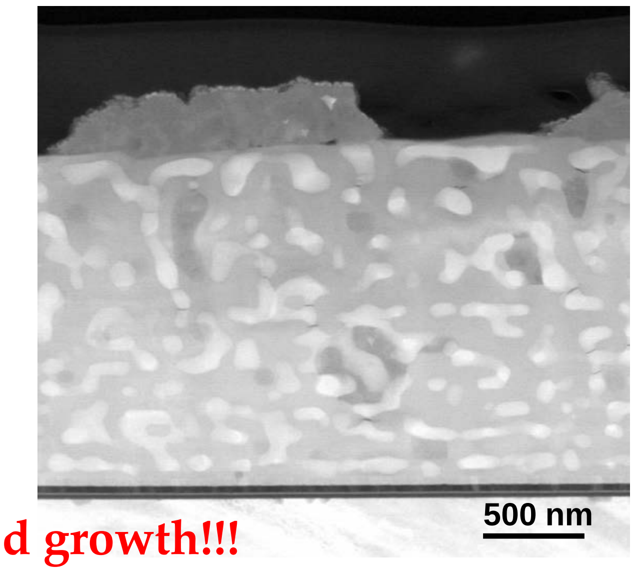

- Very low PO_2 zone (~ 10^{-5} Torr): **Amorphous Film**
- Lower PO_2 zone (~30 mTorr): **Gd_2O_3 + Liquid (< 5 sec)**
- Higher PO_2 zone (~100 mTorr): **GdBCO Film (< 20 sec)**

GdBCO growth mechanism: a seeded melt-textured growth!!!

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SuNAM's Results

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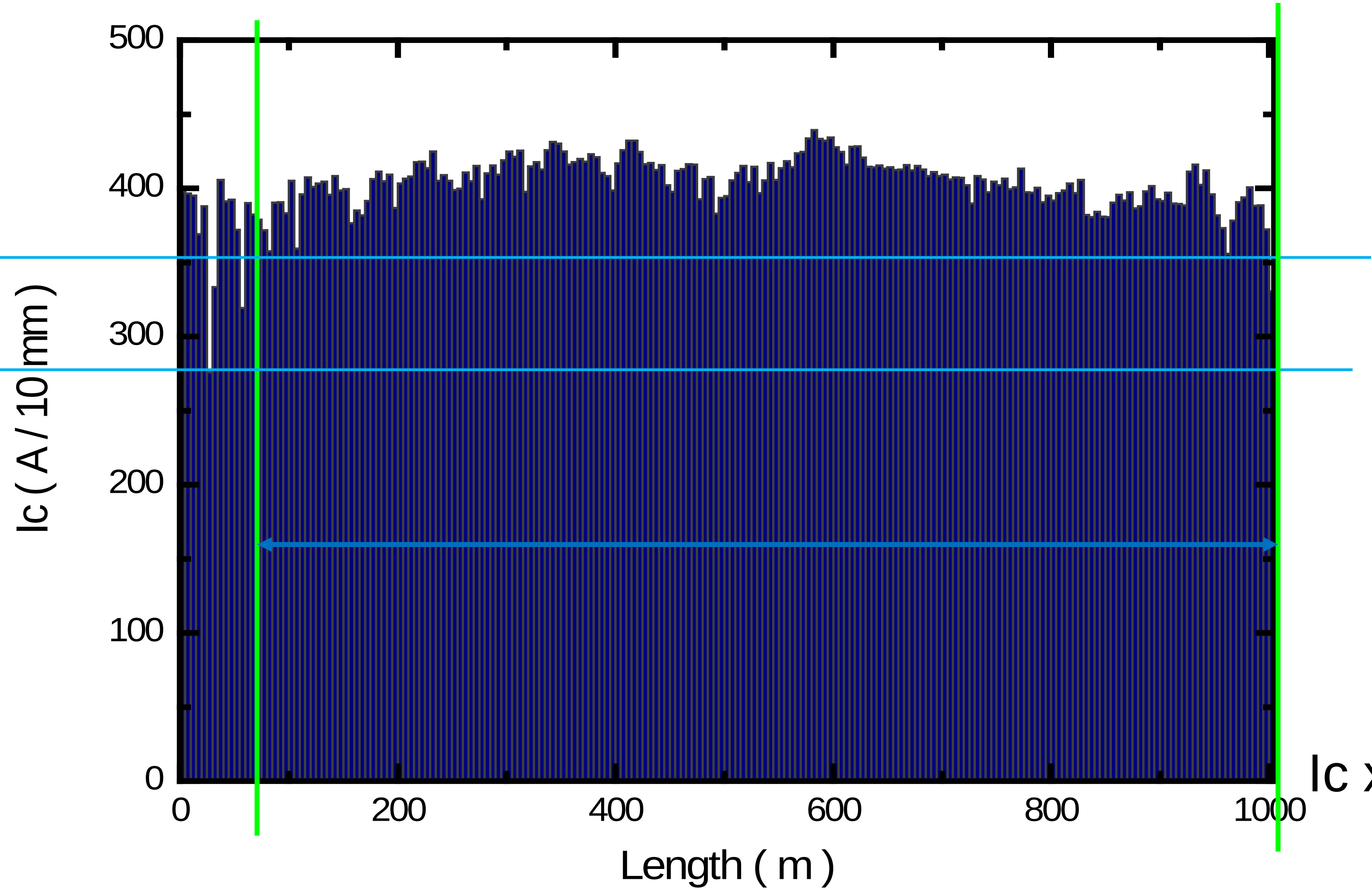
RCE – DR Results on Stainless steel substrate (2011. 10)



Ic x L :

(1) 275A x 1,005m = 277,380

(2) 355A x 920m = 326,600

Length (m)	Ave Ic (A)	Max Ic (A)	Min Ic (A)	1 sigma (%)
1005	402	439	276	5.0

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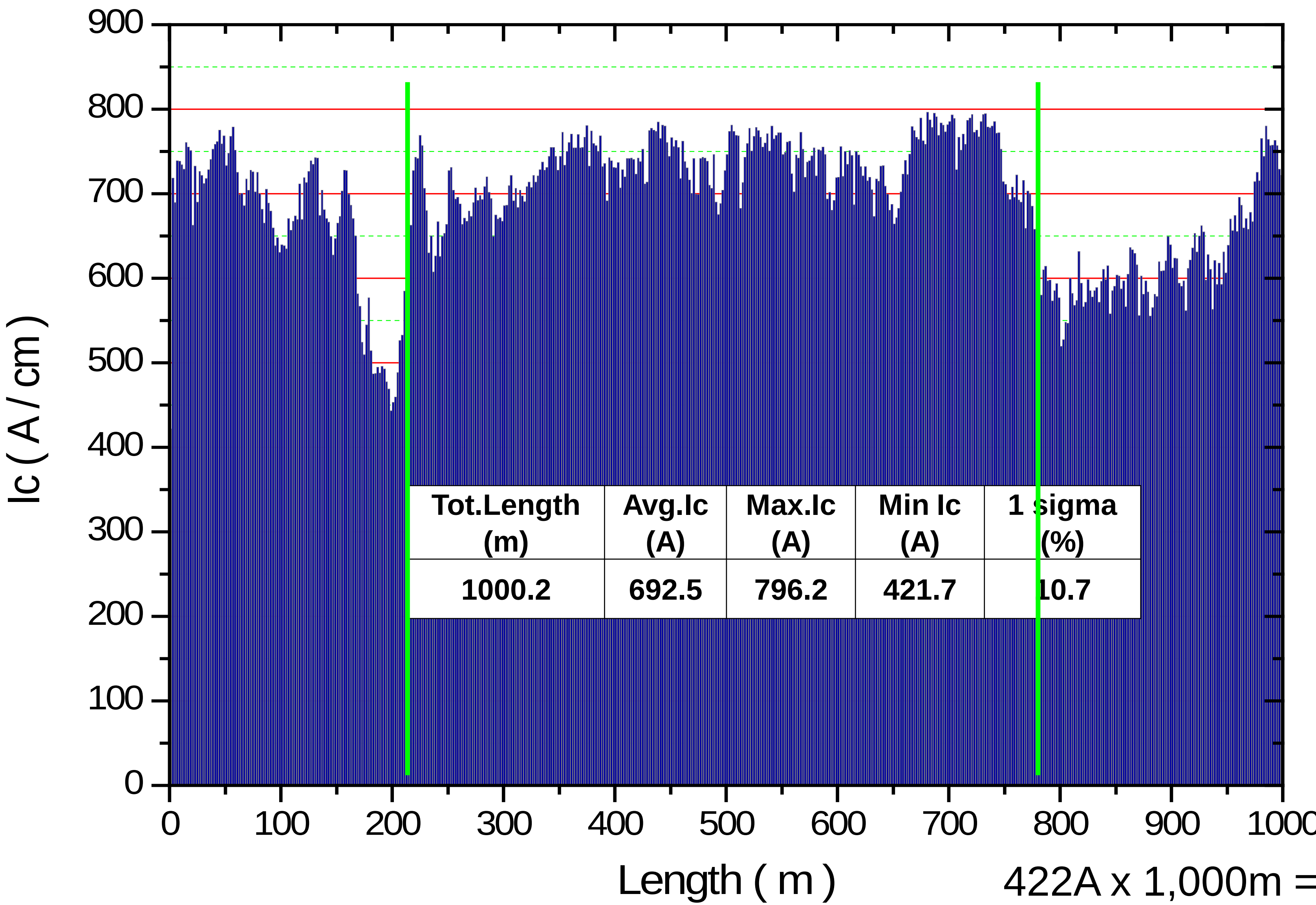
RCE - DR Results on Hastelloy substrate (2012. 01)



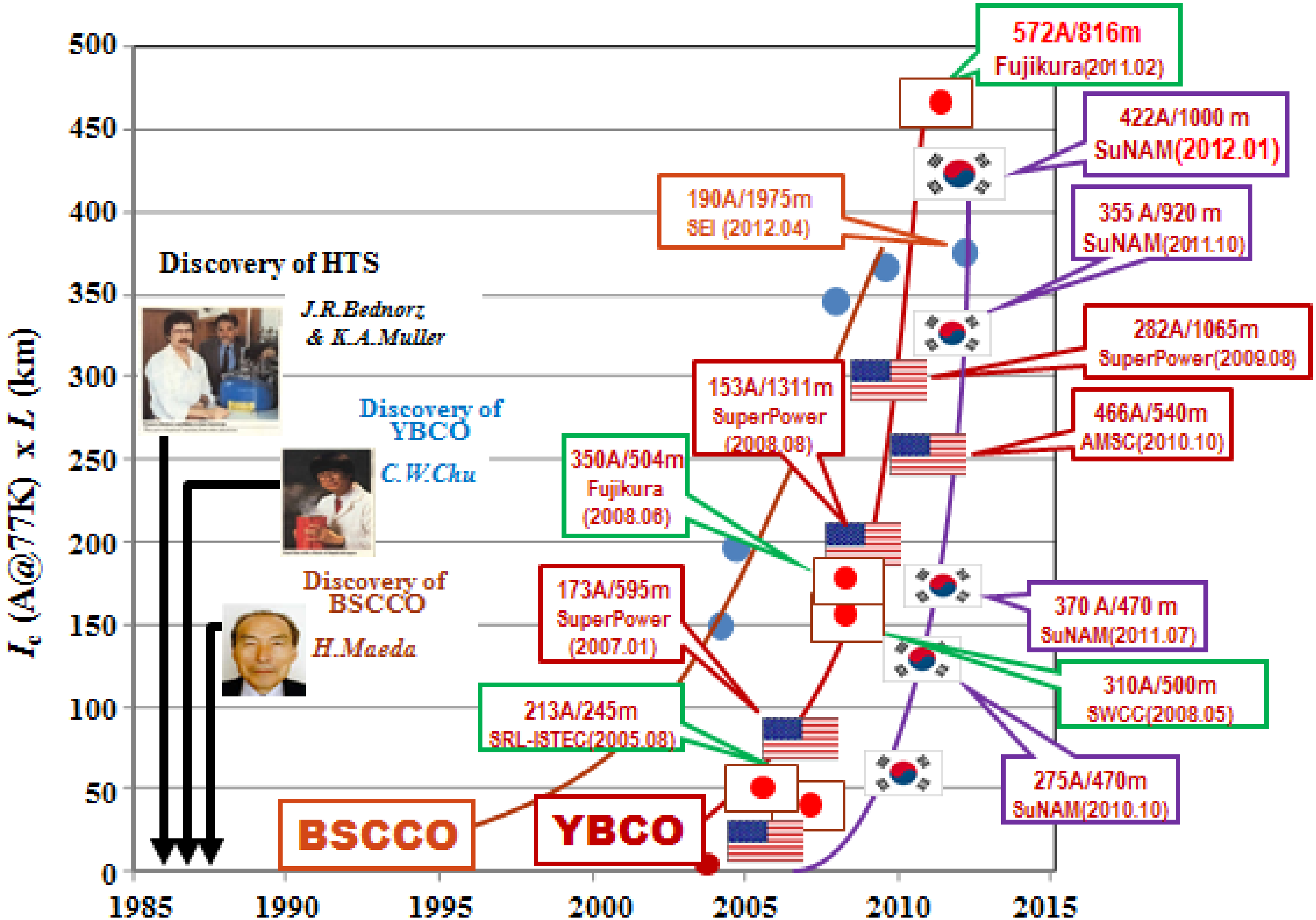
Tot.Length (m)	Avg.Ic (A)	Max.Ic (A)	Min Ic (A)	1 sigma (%)
1000.2	692.5	796.2	421.7	10.7

Ic x L :

422A x 1,000m =421,700

This shows the average vlaues for each 2 meters.

Development of HTS 2G Wire



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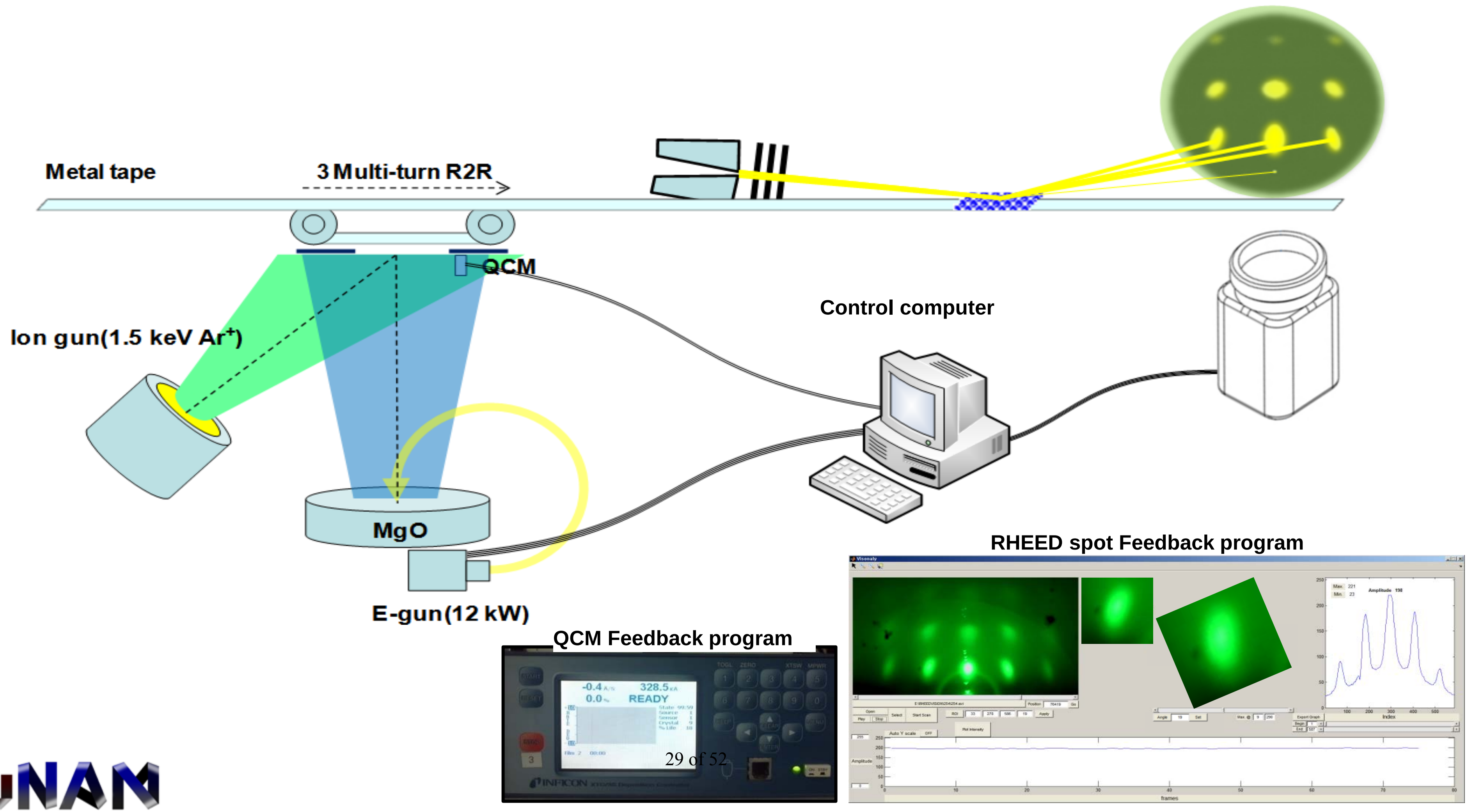
(by Dr. Izumi @ ISTEC-SRL)

Quality Control : RHEED Vision System

- An appropriate feedback algorithm can keep the shape of the RHEED spot in the specific range, while QCM monitoring to adjust the e-gun power.



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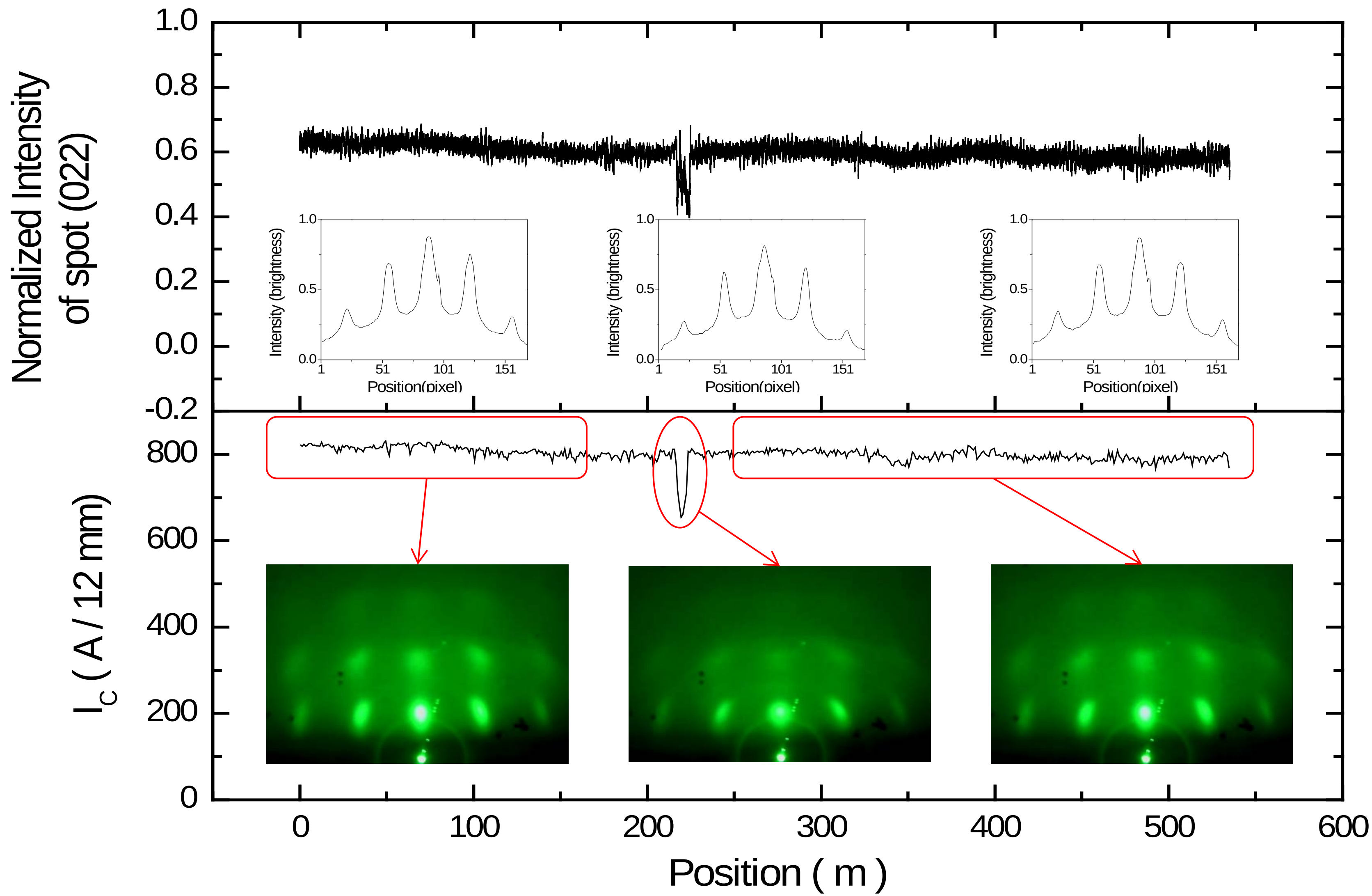
QC : RHEED vs. Ic



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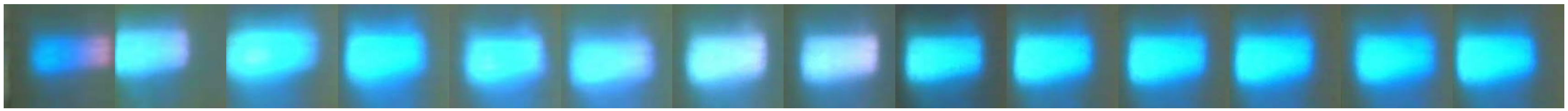
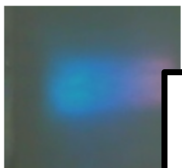
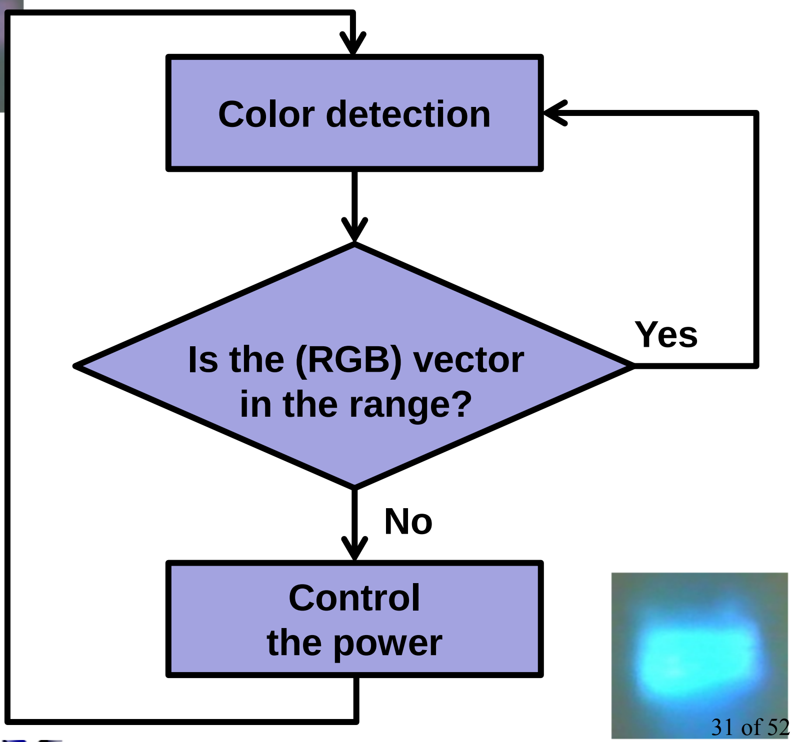
Quality Control : RCE Vision System

- RCE Vision System will be introduced for increasing the uniformity of composition in RCE-DR process. The control computer takes (RGB) values in three-dimensional vector space which is transformed from the color of the tape surface.

[Start]  [End]

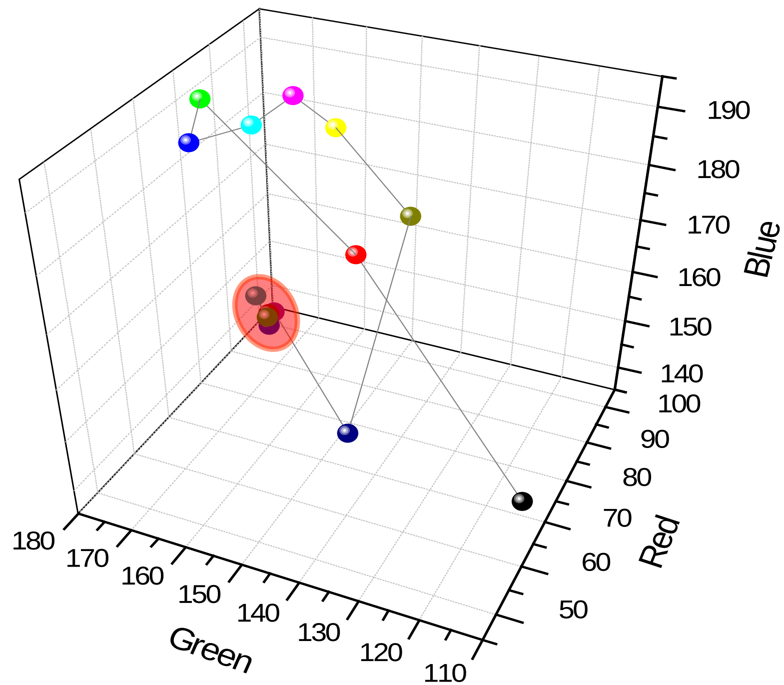


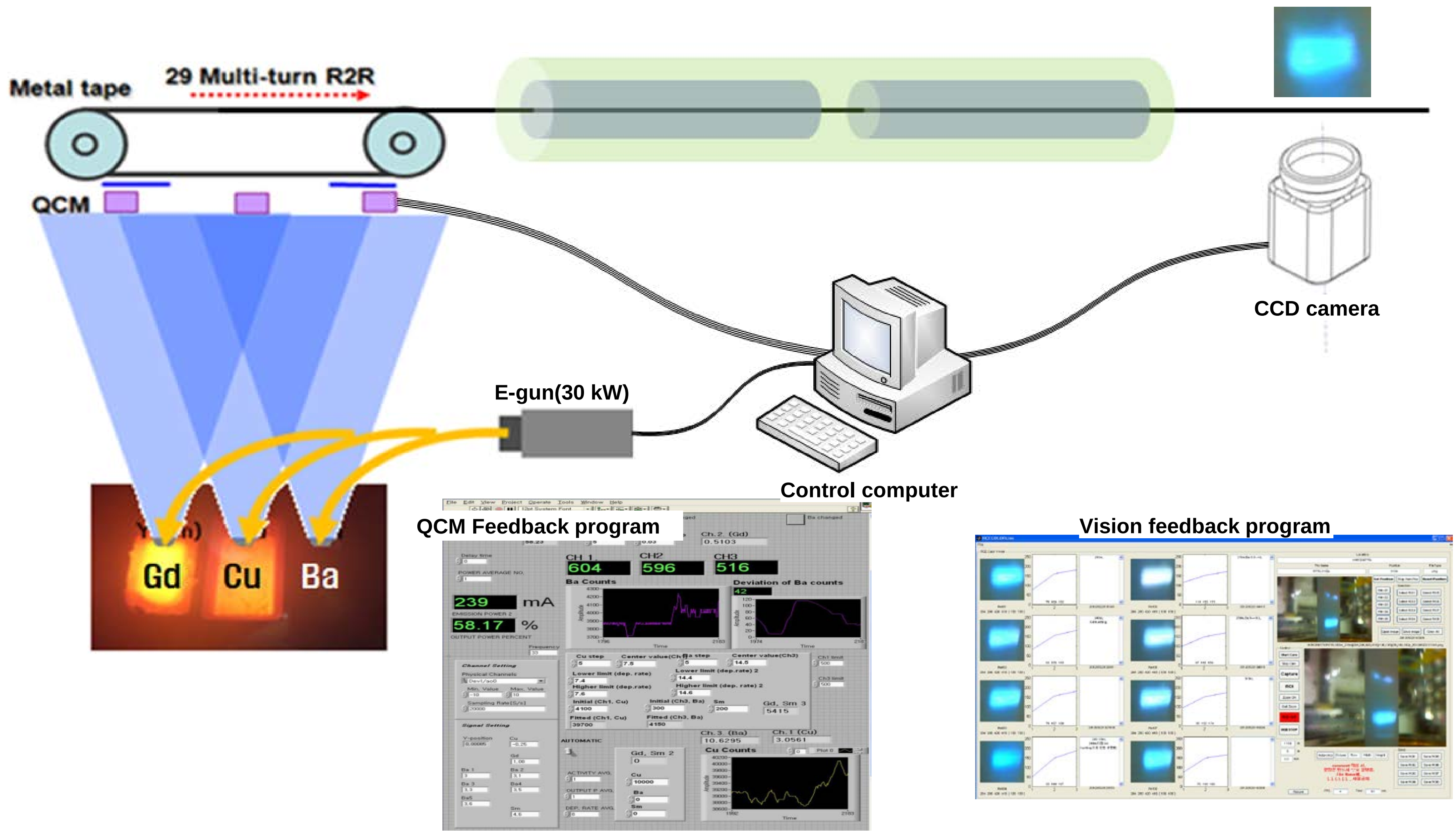
Start color



End color

(79,166,189)





- An appropriate feedback algorithm can keep the color of the tape surface in the specific range, while QCM monitoring to adjust the e-gun power.

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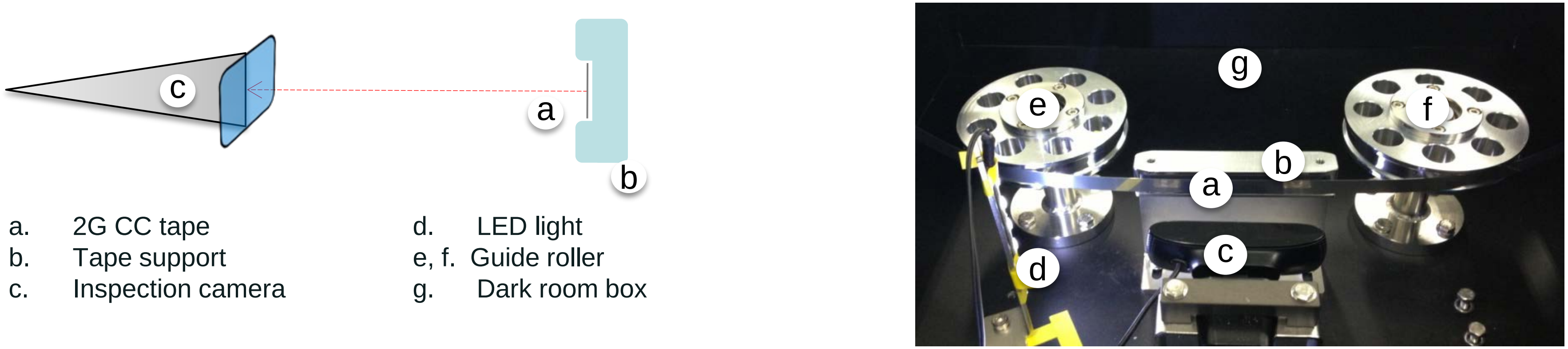
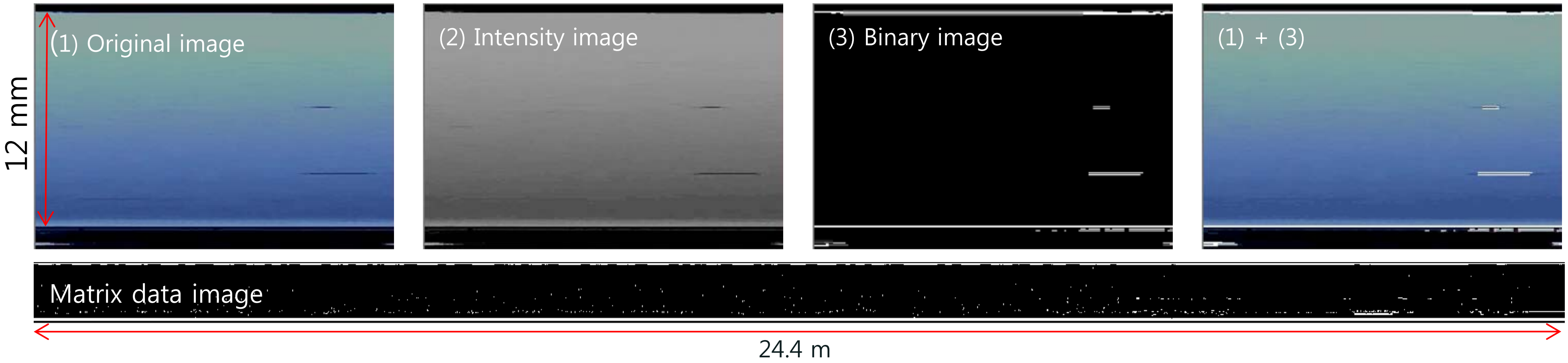
Quality Control : Visual inspection



a. 2G CC tape
b. Tape support
c. Inspection camera
d. LED light
e, f. Guide roller
g. Dark room box

※ Defect information is taken from the binary image.
※ Matlab program converts images into data real-time. 12 mm width can be sliced as 55 lines with the resolution 0.22 mm size.



- Installation of the inspection equipment for zero surface defect on the silver sputtering process.
- Digitalize the silver sputtered surface of 2G CC tape.

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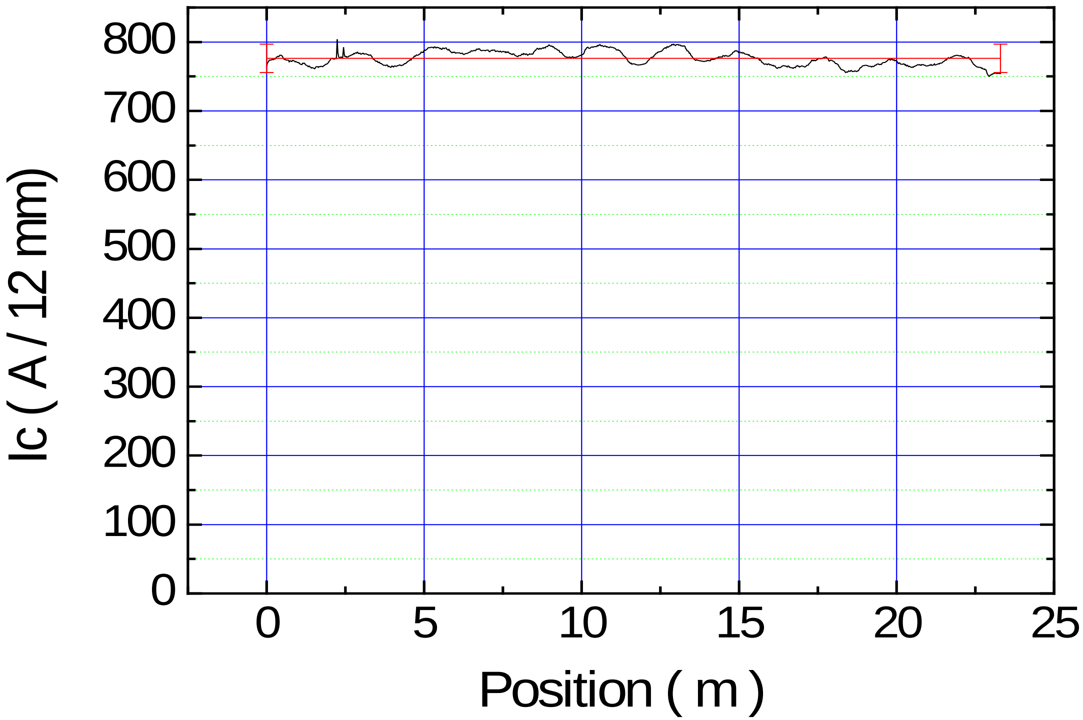
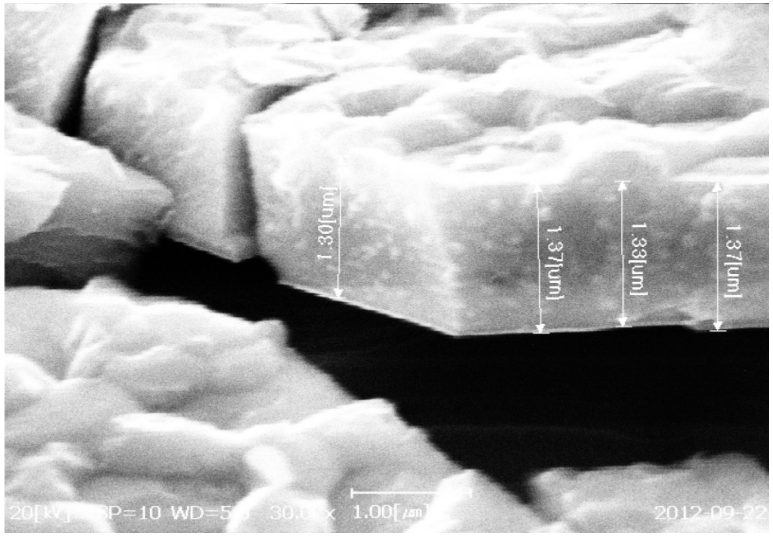
Optimization properties of GdBCO CC on STS substrate



Thickness : ~ 1.32 um



Section	Avg. I_C	SD	min. I_C	max. I_C	Uniformity(%)	
(m~m)	(A)				SD	min-max
60 cm section Continuous I_C (A/12mm)						
0~23.3	776	10	750	804	98.7%	96.4%

Average Ic = 647 A/cm
Jc ~ 4.9 MA/cm^2
1sigma ~ 10 A (1.3 %)

$$Min-Max\,Uniformaty\ (\%) = Max\left(\frac{Max.I_C - Avg.I_C}{Avg.I_C}, \frac{Avg.I_C - Min.I_C}{Avg.I_C}\right)\times 100$$

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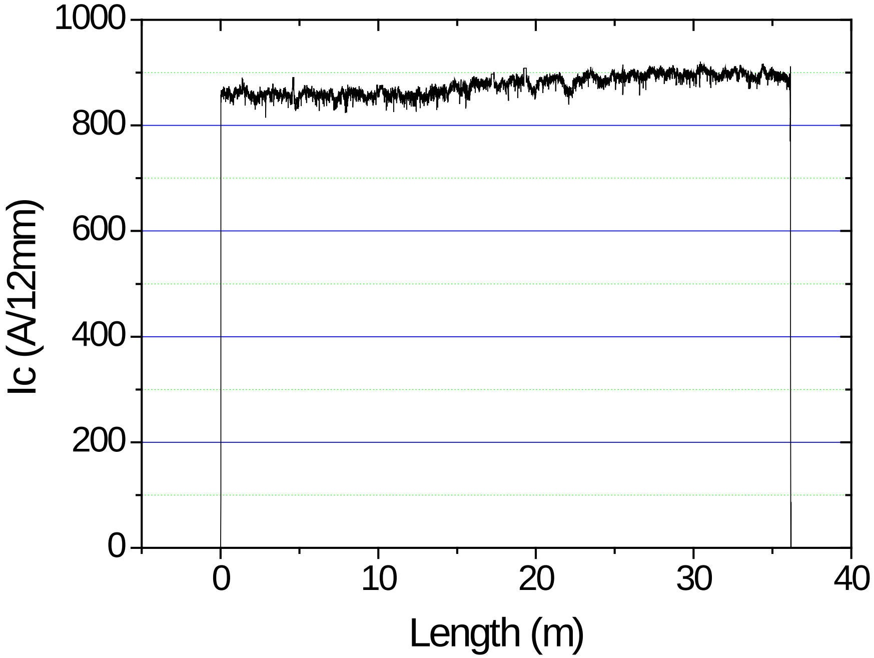

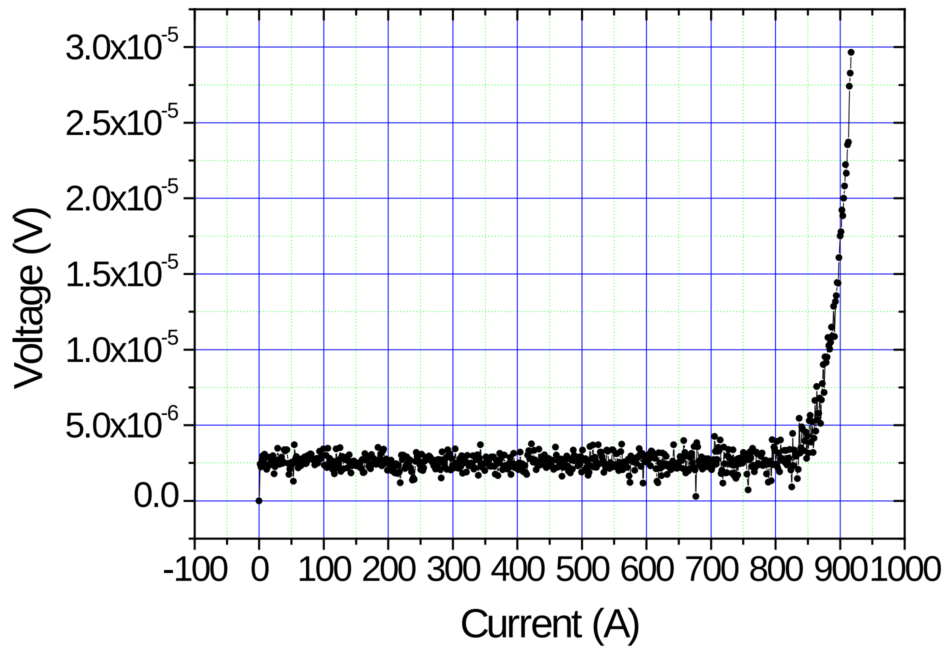

Average Ic = 742 A/cm

Jc ~ 5.3 MA/cm^2

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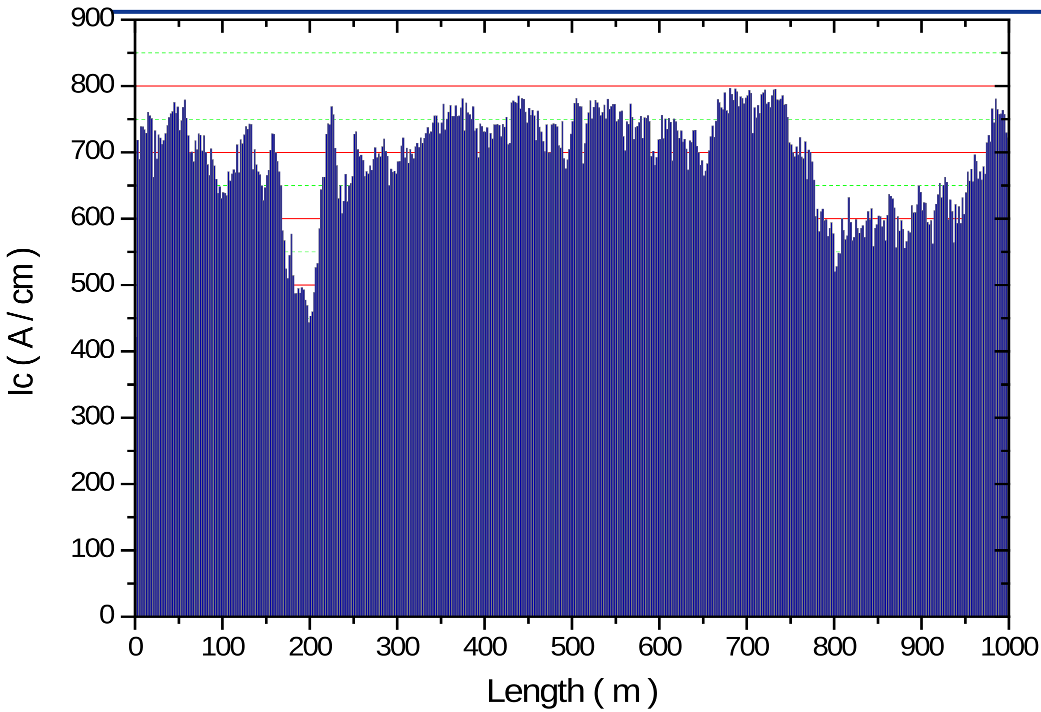
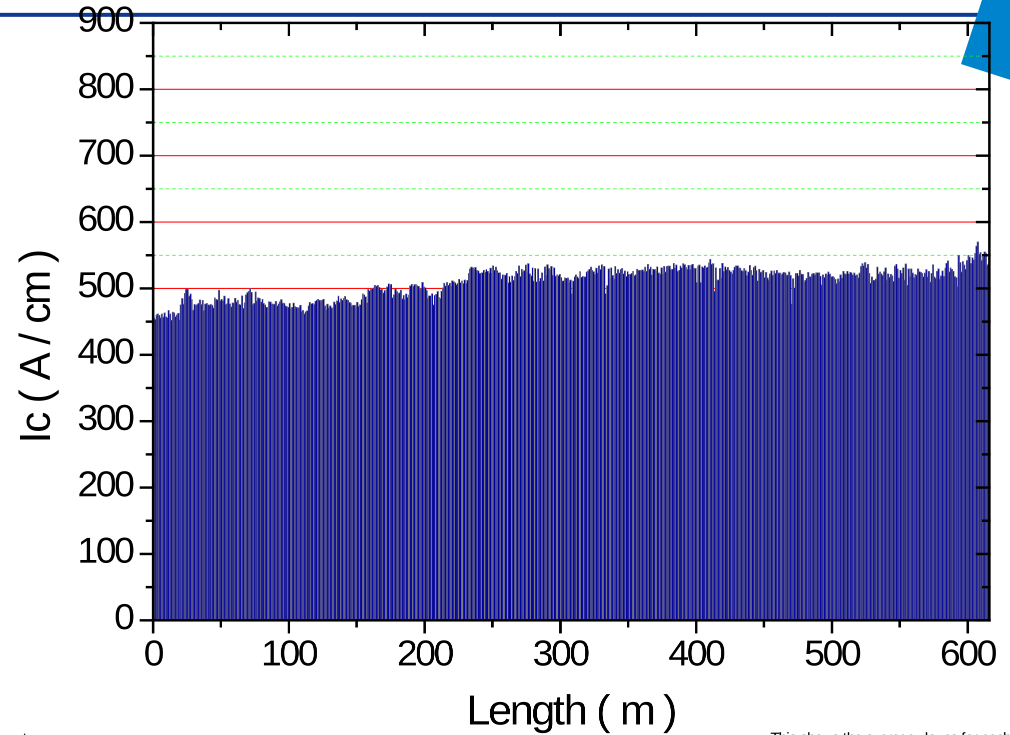
RCE – DR Results on Hastelloy substrate



This shows the average vlaues for each 2 meters.



This shows the average vlaues for each 1 m

Tot.Length (m)	Avg.Ic (A)	Max.Ic (A)	Min Ic (A)	1 sigma (%)
1000.2	692.5	796.2	421.7	10.7

	Mean	Standard Deviation	Minimum	Maximum
I_C (A)	510	19.3	452	570

Min-Max Uniformity(%)	COV (%)	$COV_{\|min-max\|}$ (%)
88.2	4.5	23.2

Ic x L : 422A x 1,000m =421,700

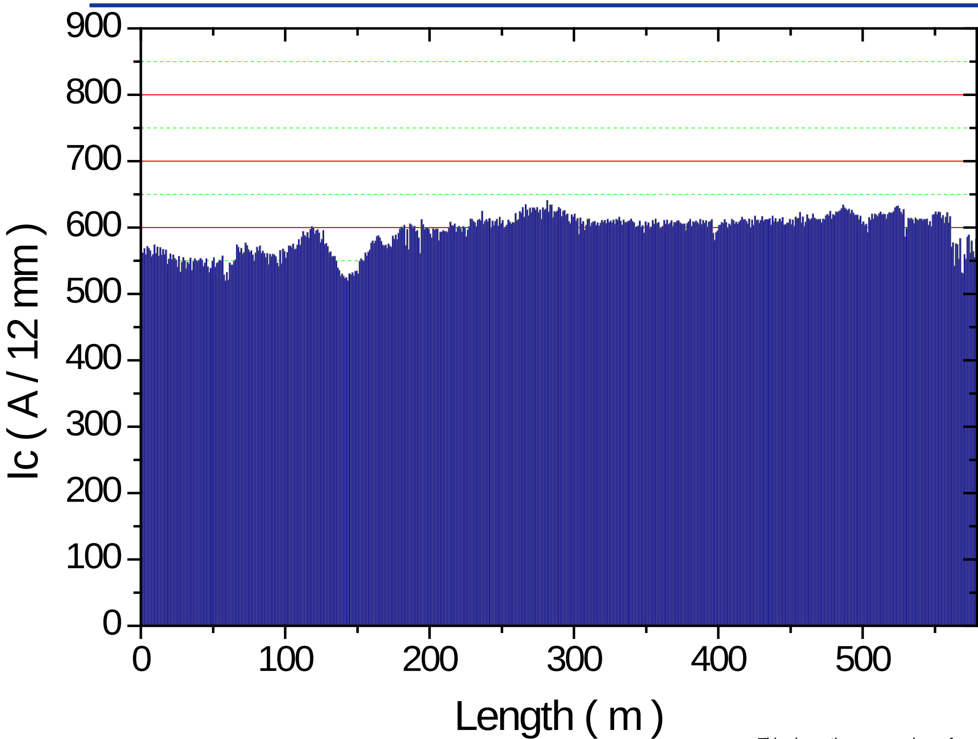
$$\mathrm{COV}_{|\mathrm{min-max}|} = \frac{|I_{C,\max} - I_{C,\min}|}{\overline{\chi}} \times 100(\%)$$

σ : Standard Deviation, $\overline{\chi}$: Mean I_C

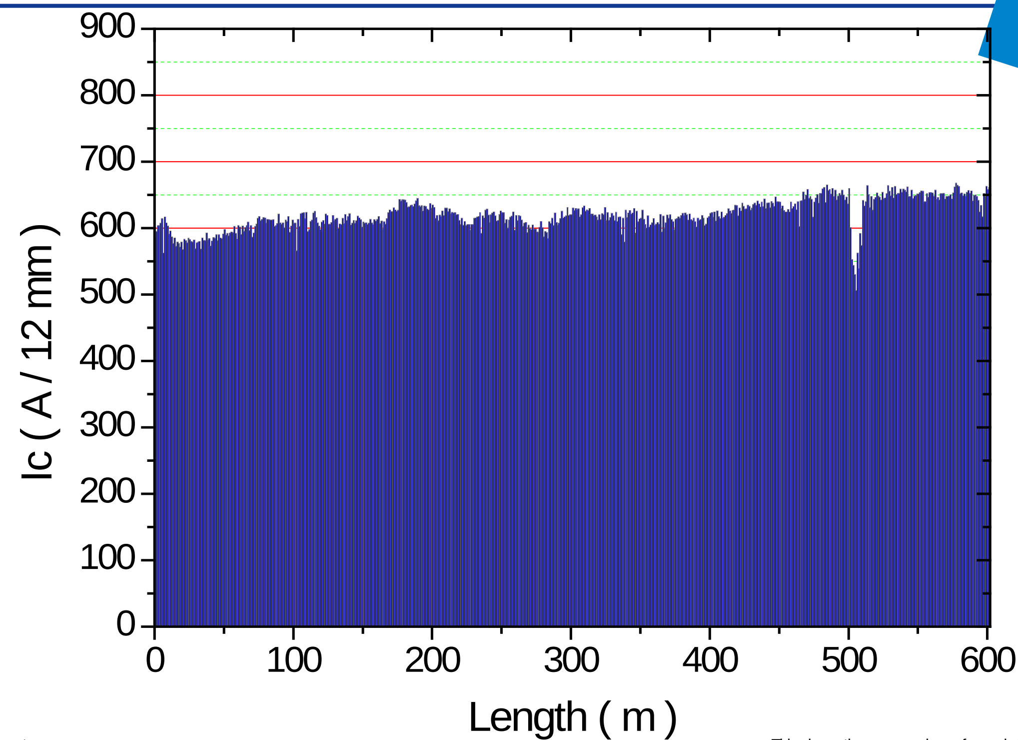
$$\mathrm{COV(coefficient\ of\ variation)} = \frac{\sigma}{\overline{\chi}} \times 100(\%)$$

IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), October 2013
Paper based on this presentation was published by Superconductor Science & Technology (SuST, IOP) 27, No. 4, 044018 (2014)

RCE – DR Results on Hastelloy substrate



This shows the average vlaues for each 1 meters.



This shows the average vlaues for each 1 me

	Mean	Standard Deviation	Minimum	Maximum
I_C (A)	594	22.7	519	640

Min-Max Uniformity(%)	COV (%)	$COV_{\vert min\text{-}max\vert}$ (%)
87.5	4.6	20.4

	Mean	Standard Deviation	Minimum	Maximum
I_C (A)	619	18.8	506	667

Min-Max Uniformity(%)	COV (%)	$COV_{\vert min\text{-}max\vert}$ (%)
81.8	3.6	26.0

$$\mathrm{COV}_{|\mathrm{min-max}|} = \frac{|I_{C,\max} - I_{C,\min}|}{\overline{\chi}} \times 100(\%)$$

$$\mathrm{COV(coefficient\ of\ variation)} = \frac{\sigma}{\overline{\chi}} \times 100(\%)$$

σ : Standard Deviation, $\overline{\chi}$: Mean I_C

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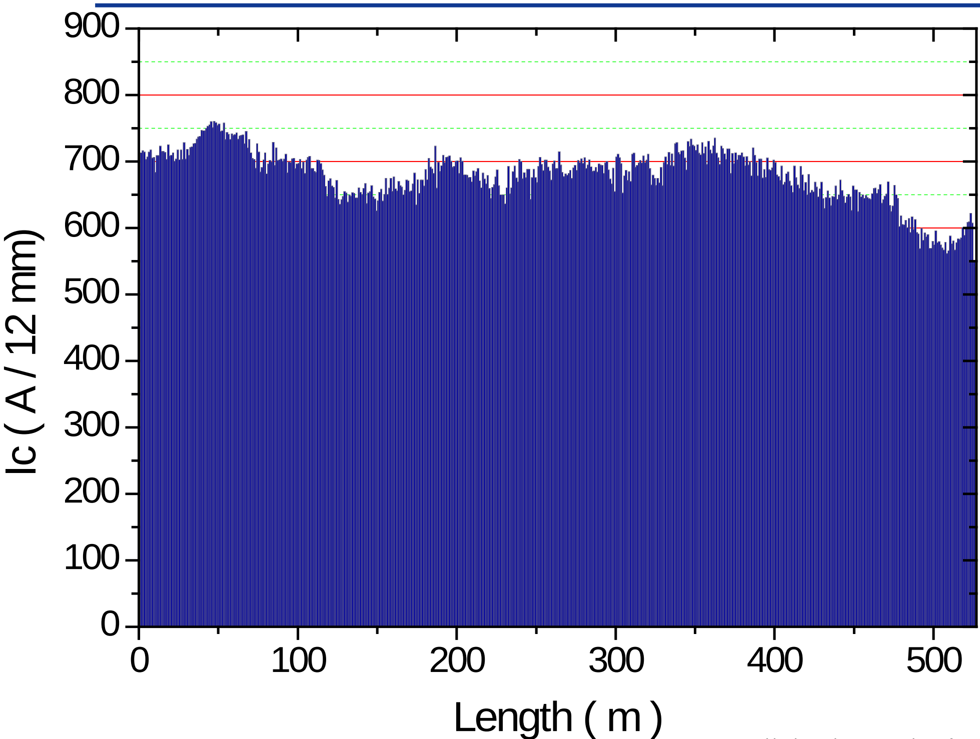
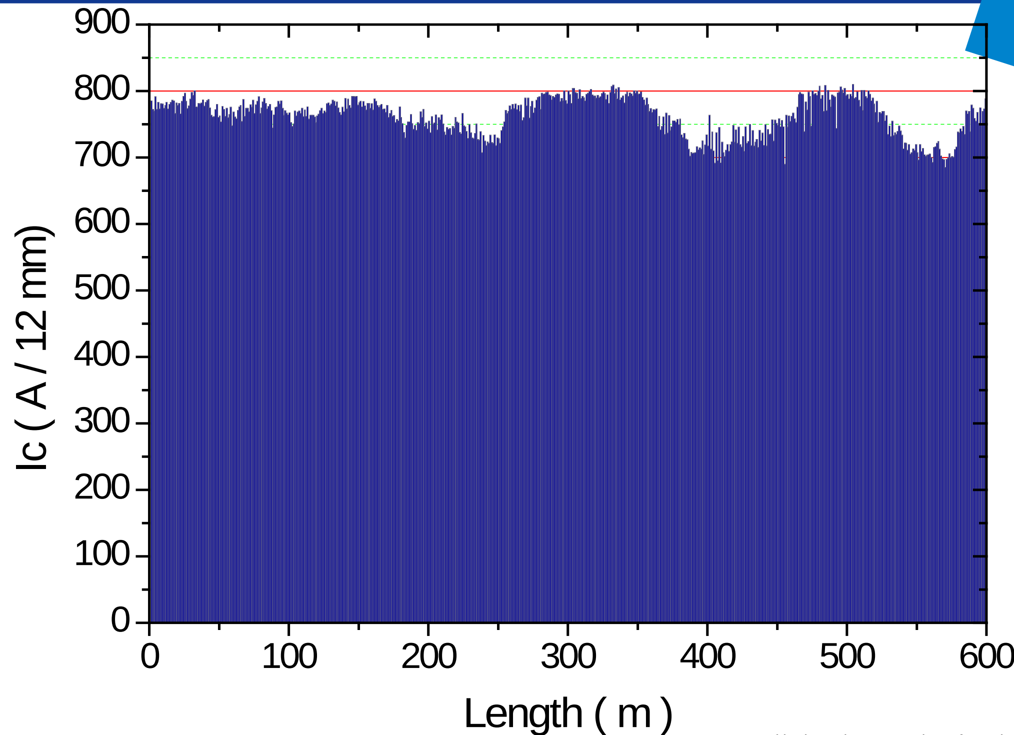
RCE – DR Results on Stainless steel substrate





	Mean	Standard Deviation	Minimum	Maximum
I_C (A)	678	40.3	542	761

Min-Max Uniformity(%)	COV (%)	$COV_{\|min-max\|}$ (%)
79.9	5.9	32.2

	Mean	Standard Deviation	Minimum	Maximum
I_C (A)	762	28.5	686	810

Min-Max Uniformity(%)	COV (%)	$COV_{\|min-max\|}$ (%)
90.0	3.7	16.4

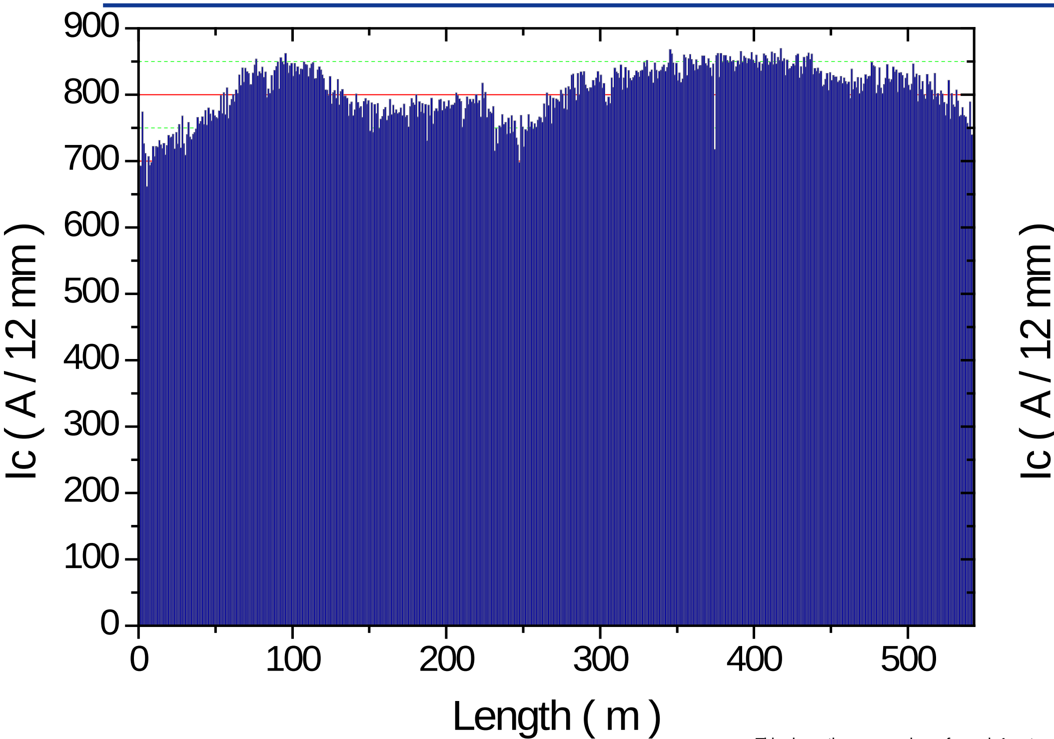
$$\mathrm{COV}_{|\text{min-max}|} = \frac{|I_{C,\max} - I_{C,\min}|}{\bar{\chi}} \times 100(\%)$$

$$\mathrm{COV}(\text{coefficient of variation}) = \frac{\sigma}{\bar{\chi}} \times 100(\%)$$

σ : Standard Deviation, $\bar{\chi}$: Mean I_C

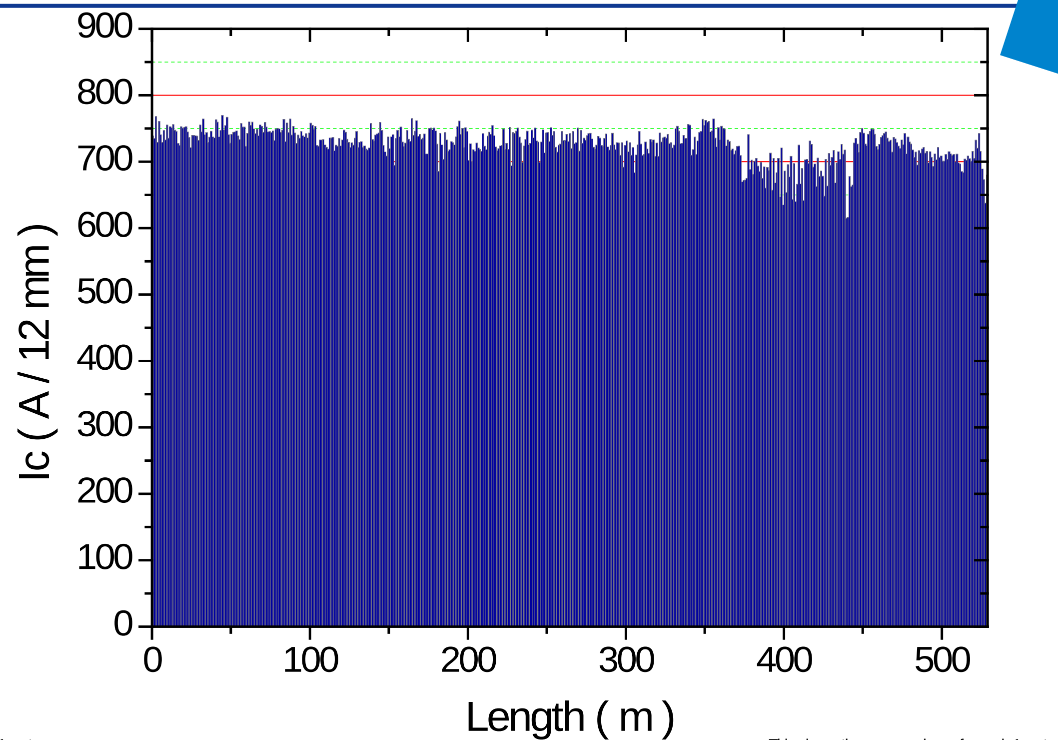
RCE – DR Results on Stainless steel substrate

Paper based on this presentation was published by Superconductor Science & Technology (SuST, IOP) 27, No. 4, 044018 (2014)



	Mean	Standard Deviation	Minimum	Maximum
I_C (A)	804	40.0	643	869

Min-Max Uniformity(%)	COV (%)	$COV_{\|min-max\|}$ (%)
80.0	5.0	28.1



	Mean	Standard Deviation	Minimum	Maximum
I_C (A)	726	24.6	614	770

Min-Max Uniformity(%)	COV (%)	$COV_{\|min-max\|}$ (%)
84.6	3.4	21.5

$$\mathrm{COV}_{|\text{min-max}|} = \frac{\left|I_{C,\max} - I_{C,\min}\right|}{\overline{\chi}} \times 100(\%)$$

$$\mathrm{COV(coefficient\ of\ variation)} = \frac{\sigma}{\overline{\chi}} \times 100(\%)$$

σ : Standard Deviation, $\overline{\chi}$: Mean I_C

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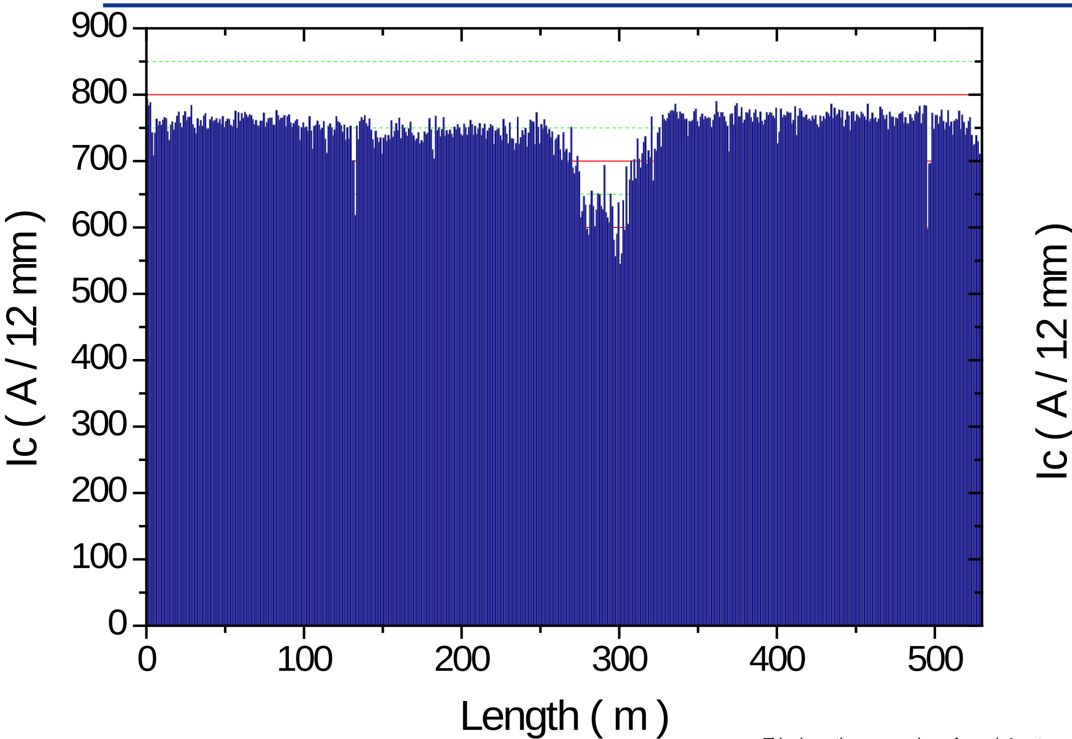
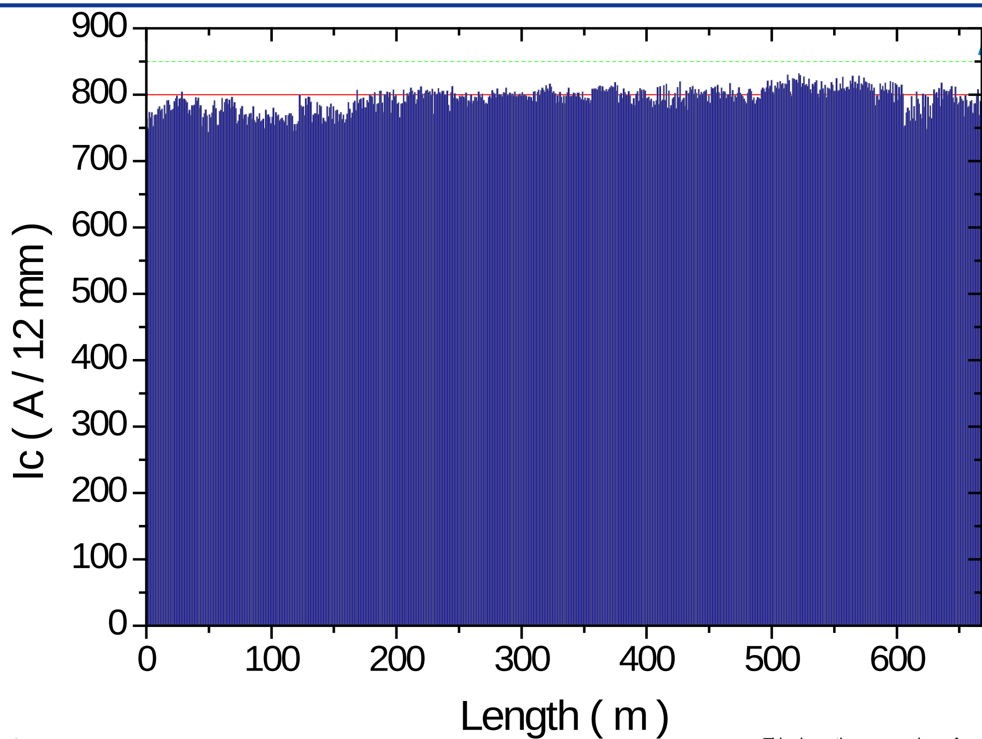
RCE – DR Results on Stainless steel substrate



This shows the average vlaues for each 1 meters.

	Mean	Standard Deviation	Minimum	Maximum
I_C (A)	745	38.9	545	793

Min-Max Uniformity(%)	COV (%)	$COV_{\|min\text{-}max\|}$ (%)
73.2	5.2	33.3



This shows the average vlaues for each 1 meters.

	Mean	Standard Deviation	Minimum	Maximum
I_C (A)	794	17.0	744	832

Min-Max Uniformity(%)	COV (%)	$COV_{\|min\text{-}max\|}$ (%)
93.7	2.1	11.1

$$\mathrm{COV}_{|\text{min-max}|} = \frac{\left| I_{C,\max} - I_{C,\min} \right|}{\overline{\chi}} \times 100(\%)$$

$$\mathrm{COV(coefficient\ of\ variation)} = \frac{\sigma}{\overline{\chi}} \times 100(\%)$$

σ : Standard Deviation, $\overline{\chi}$: Mean I_C

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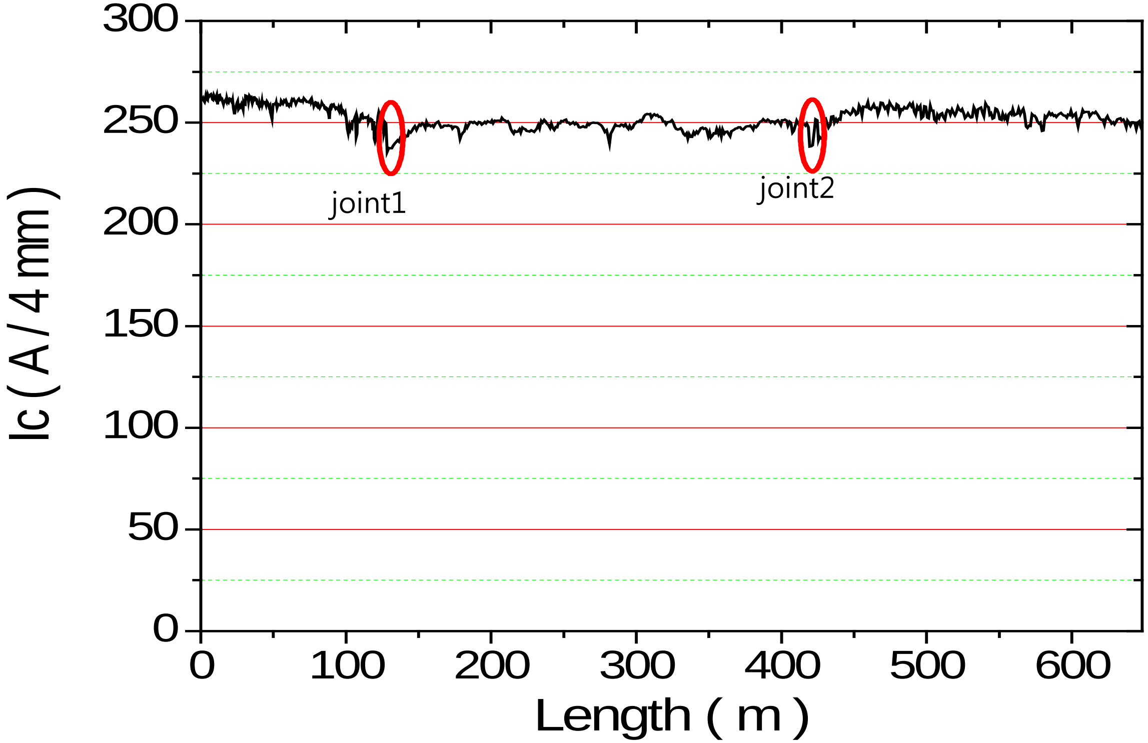
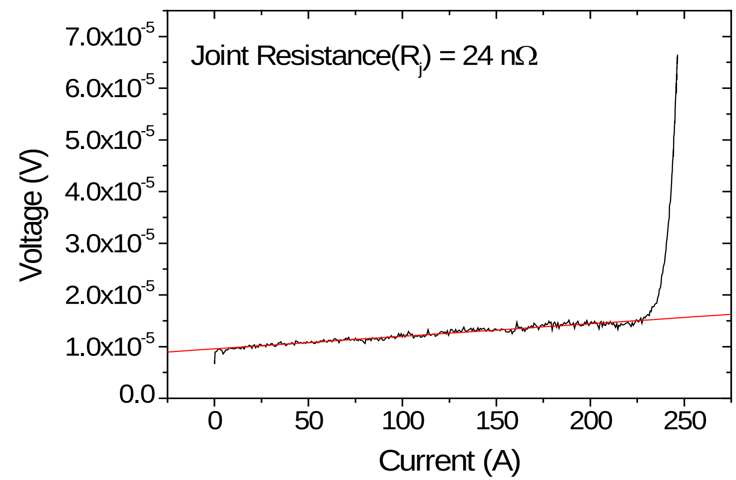
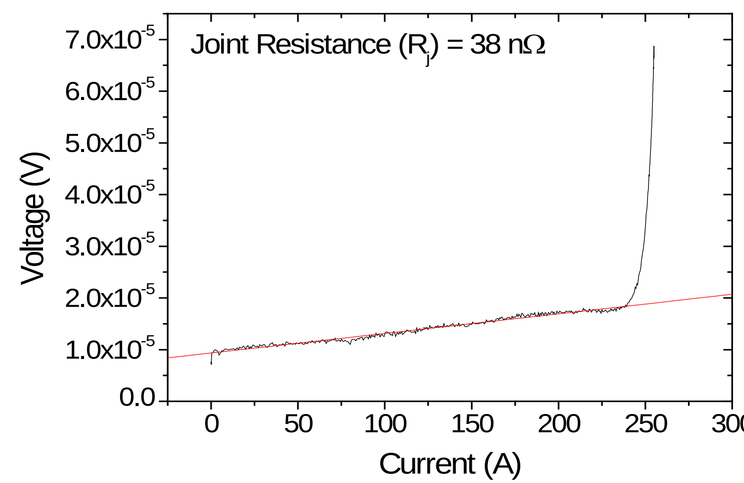
Ic / 4mm and joint resistance for brass laminated CC



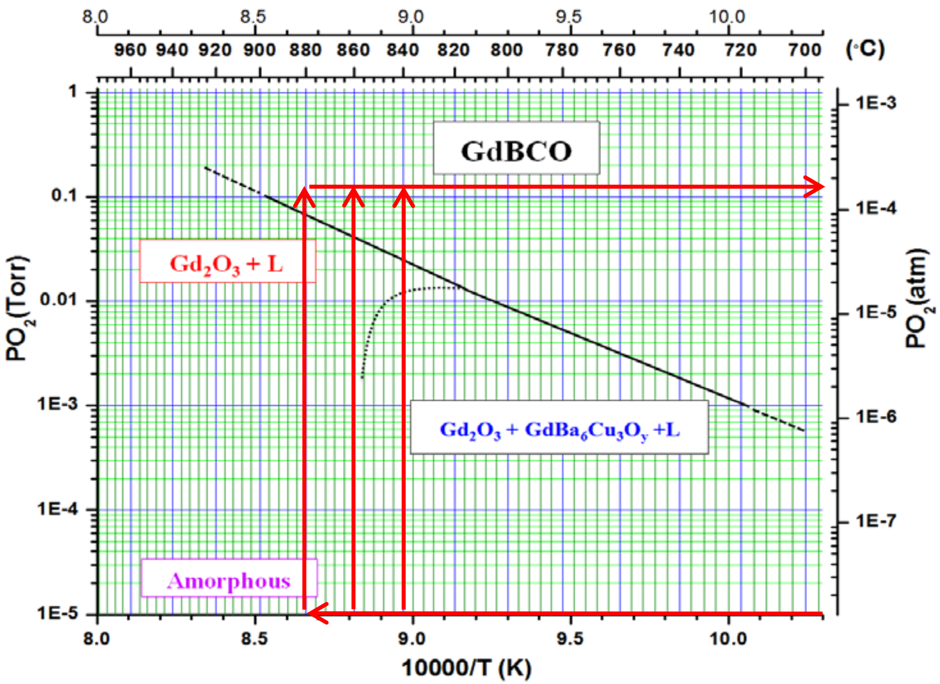


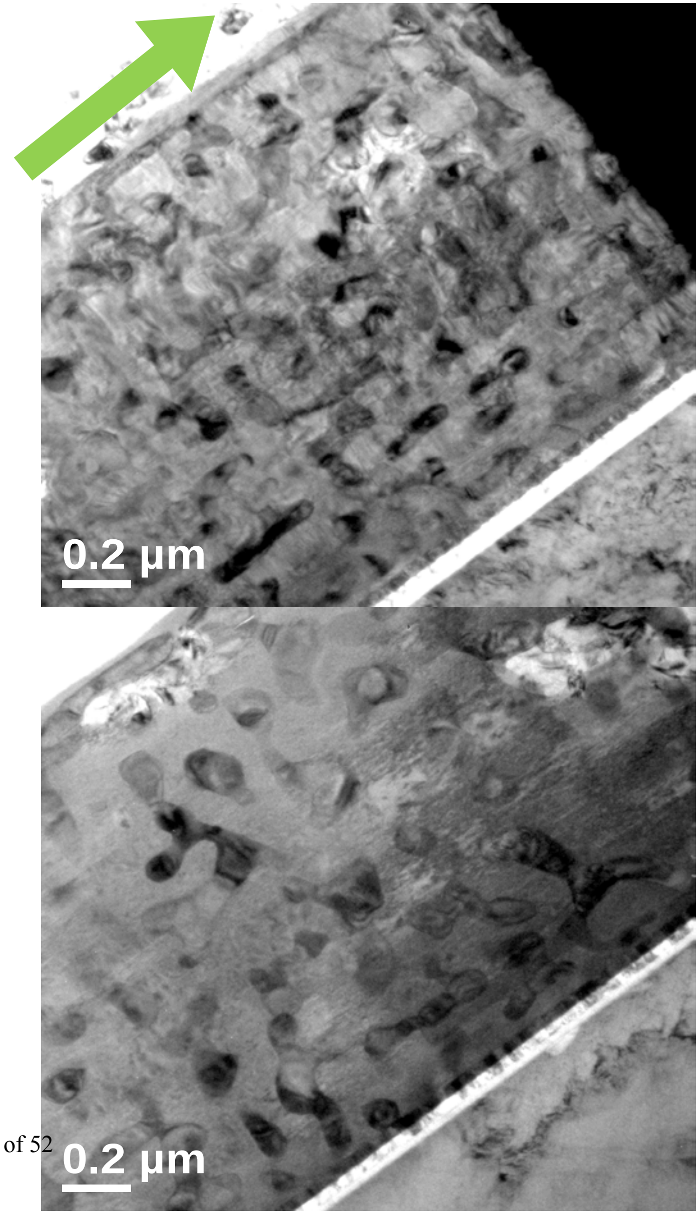


TOT	Mean	Standard Deviation	Minimum	Maximum
I_C(A)	253	5.6	236	264
$Unif_{\|min-max\|}$		COV	$COV_{\|min-max\|}$	
93.2		2.2	11.2	

Typical overlap joint length is 100 mm ~ 150 mm.

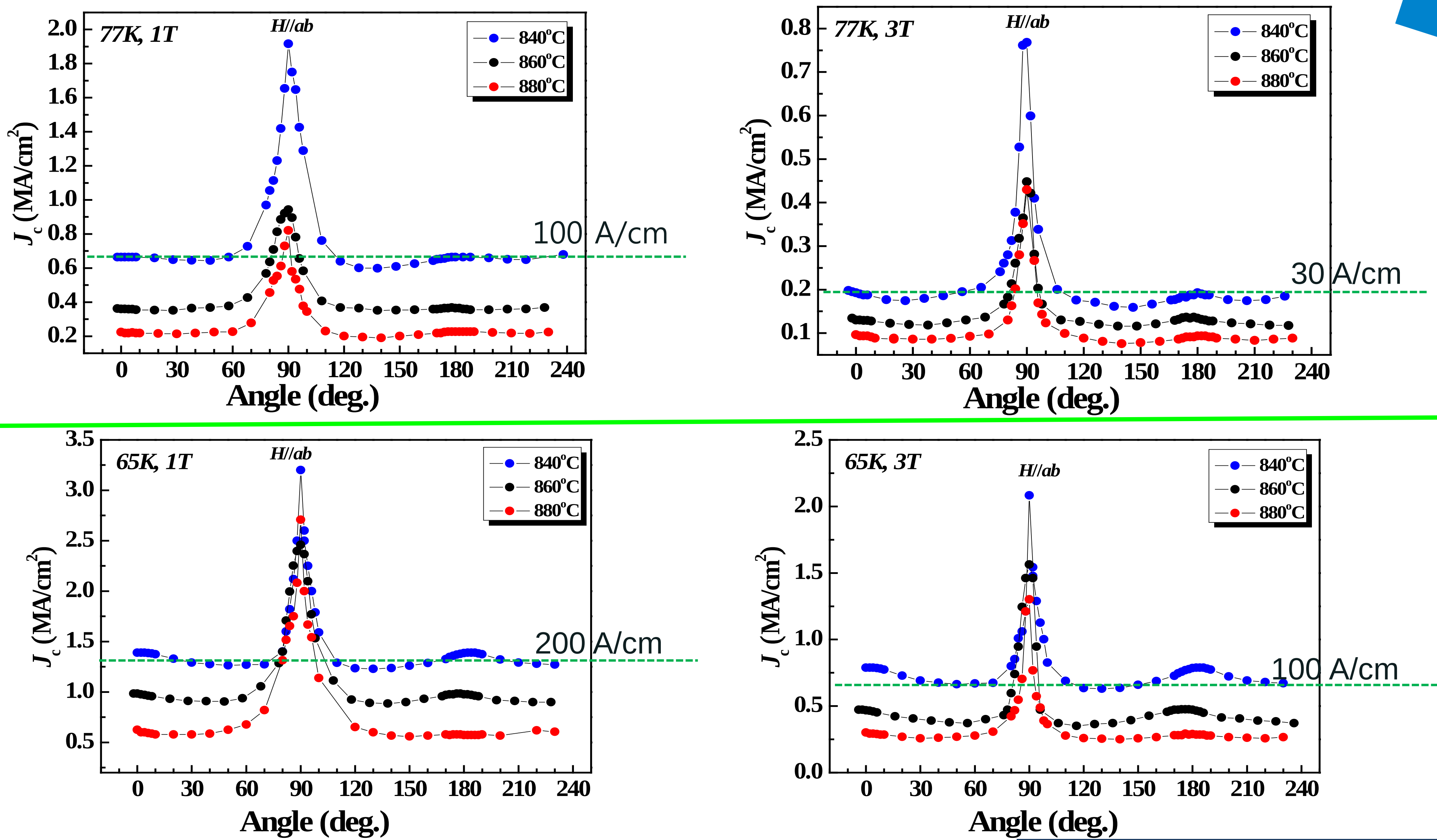
Flux pinning improvement by controlling Gd_2O_3 particles





- **840°C** sample : Particles are aligned with arrow direction.
- **880°C** sample : Particle size is bigger & randomly located.

Angular dependence of J_c at 77K & 65 K(840, 860, and 880°C)



Seoul National University
Department of Material Science & Engineering

RCE-DR : in B-field Properties add APC (Short sample)

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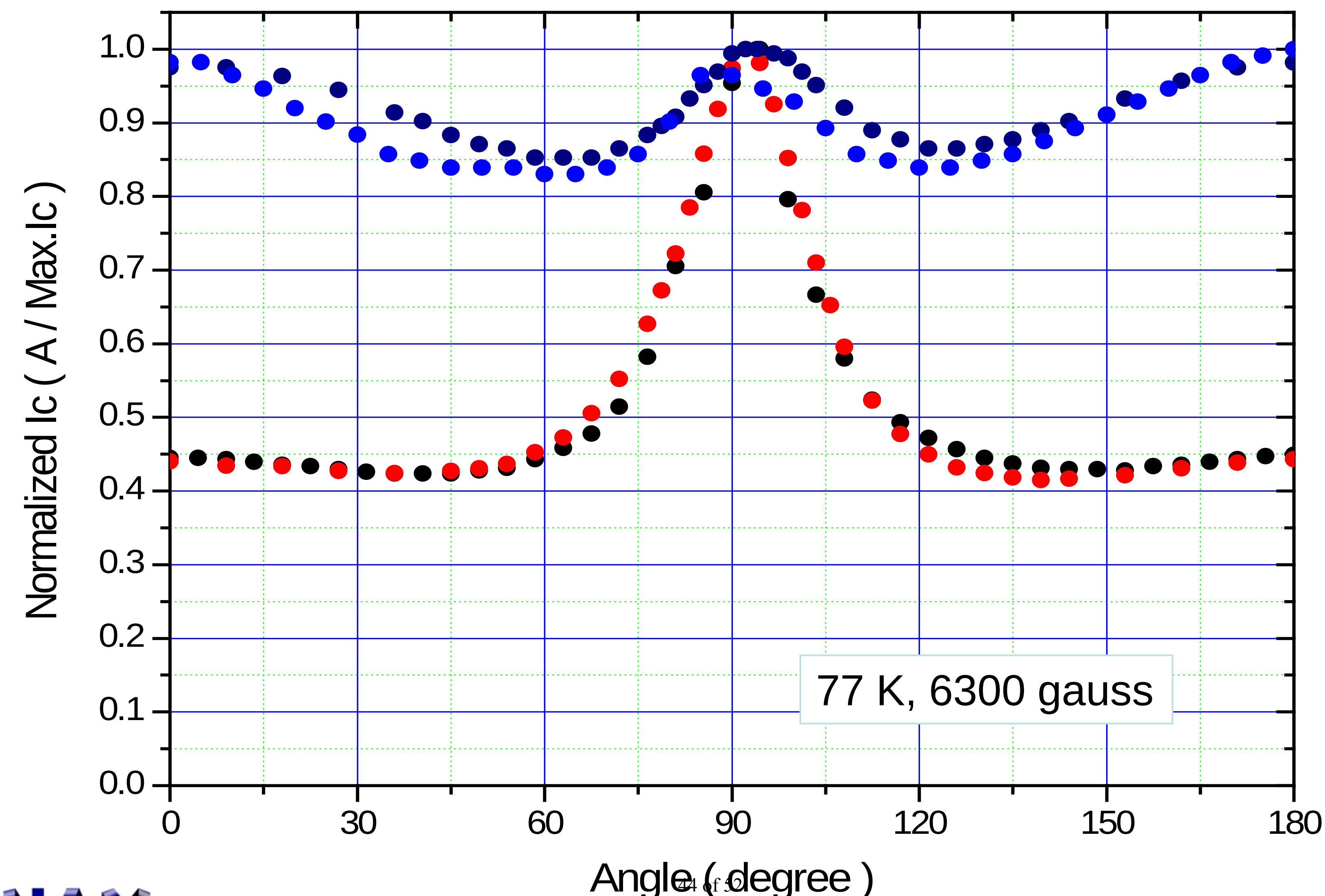

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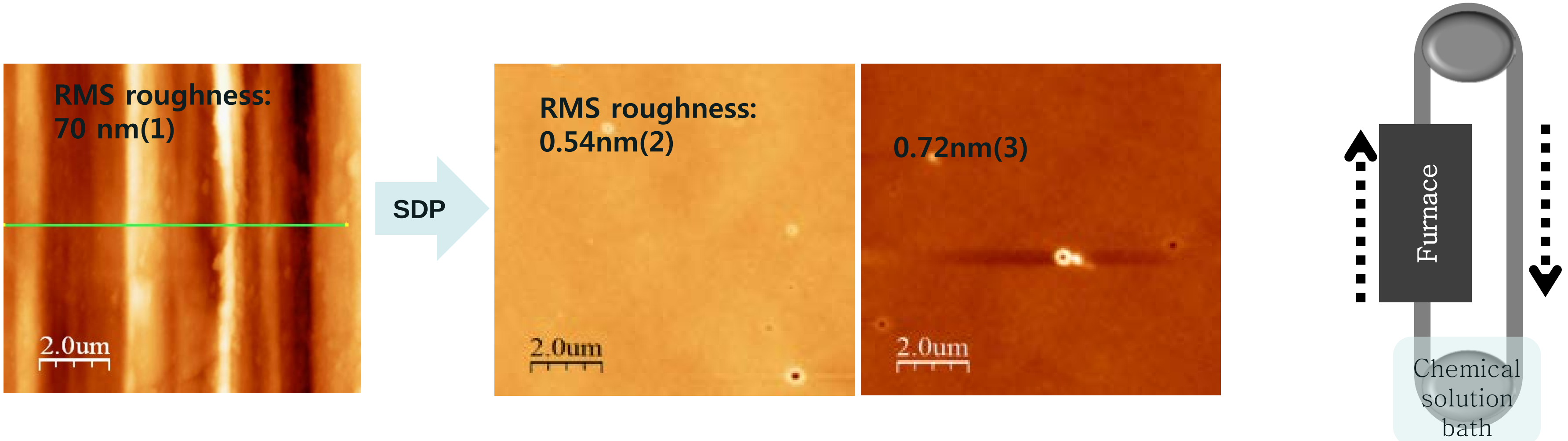
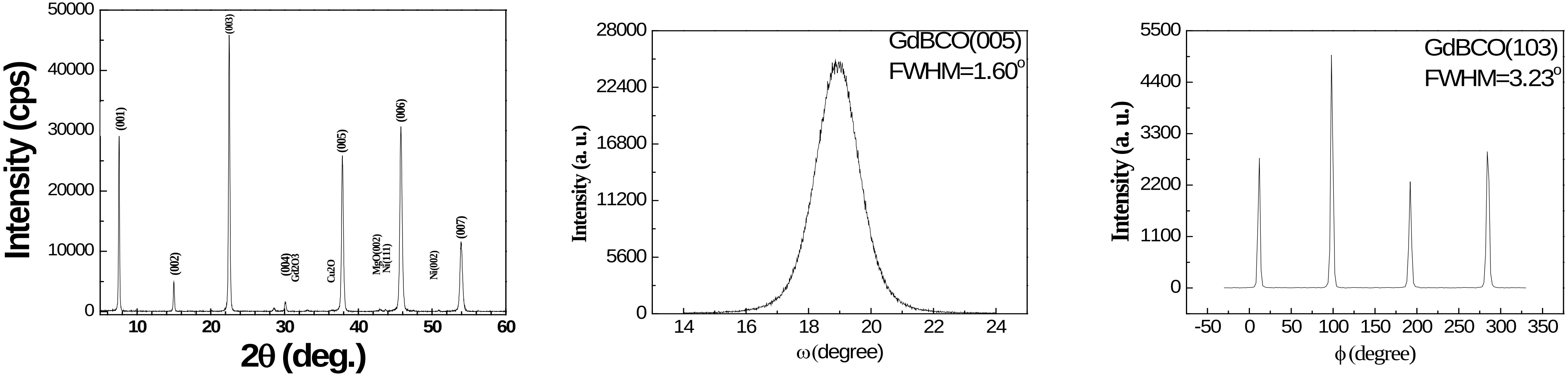
Simplified buffer layer – Solution Deposition Planarization (SDP)



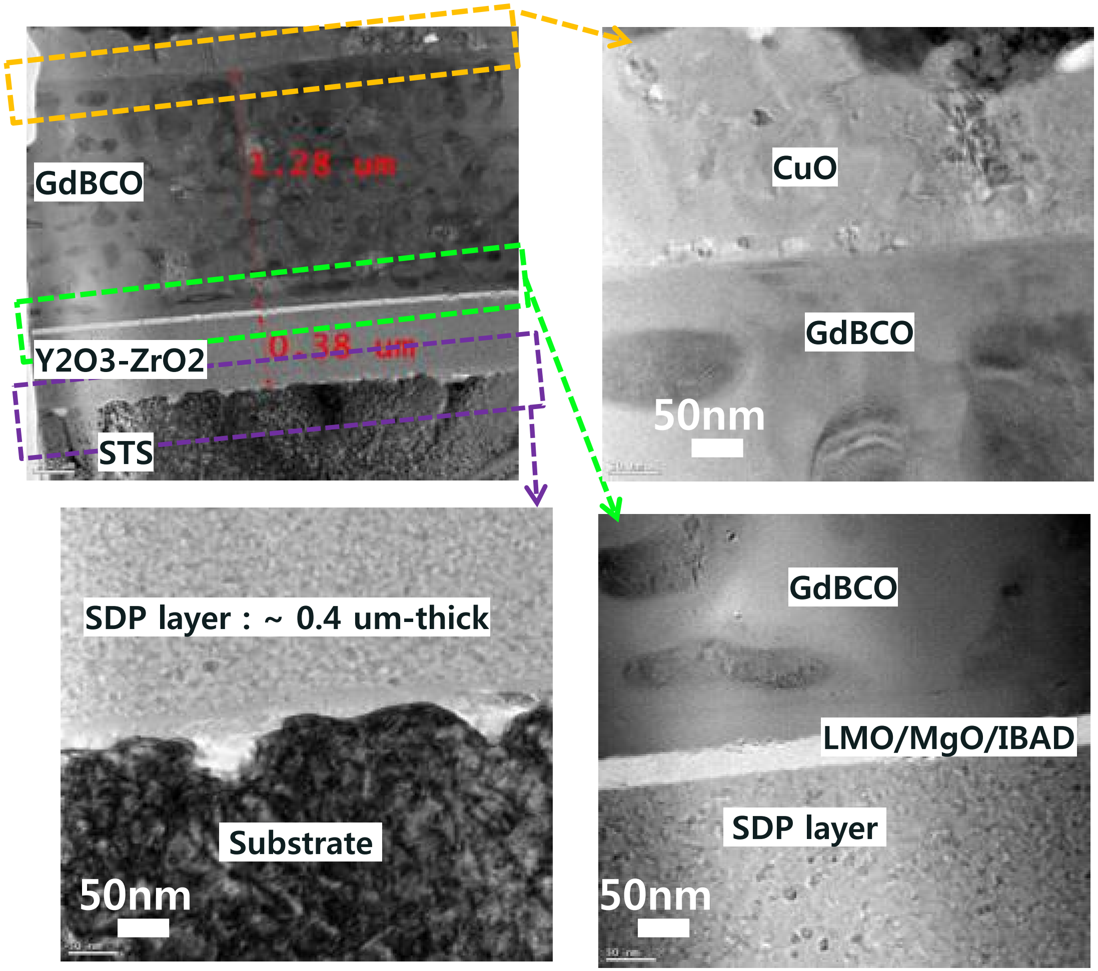
Dip coating Process

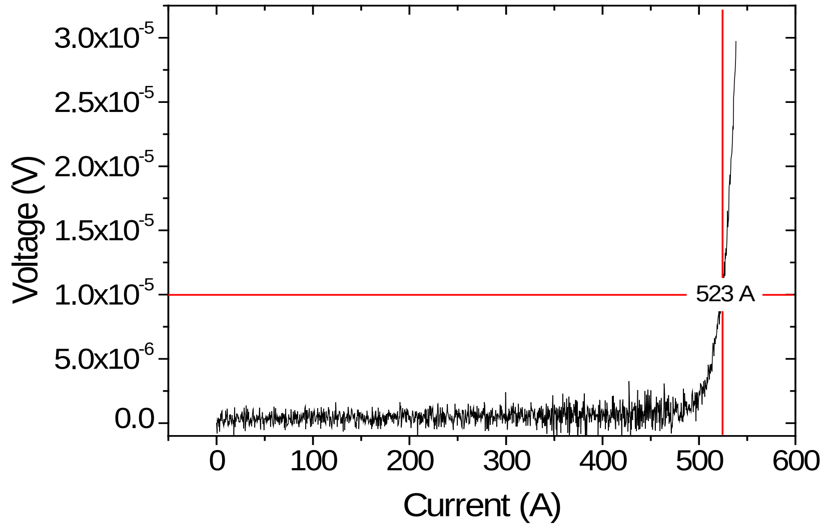


Structural properties of GdBCO on SDP substrate

Paper based on this presentation was published by Superconductor Science & Technology (SuST, IOP) 27, No. 4, 044018 (2014)

Simplified buffer layer – Solution Deposition Planarization (SDP)





I_c=523 A / 12mm

Jc ~ 3.4 MA/cm^2

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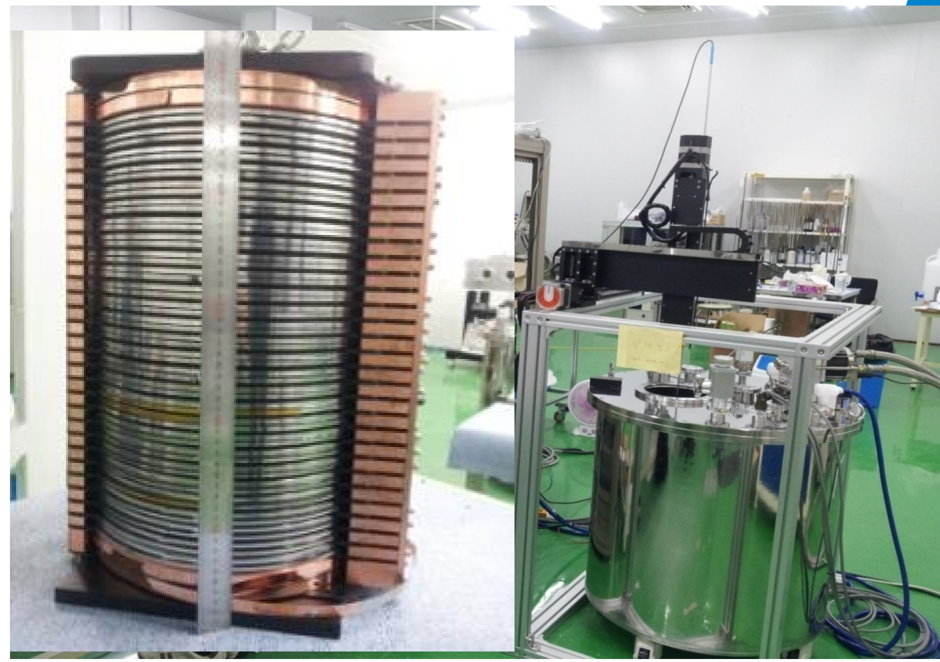
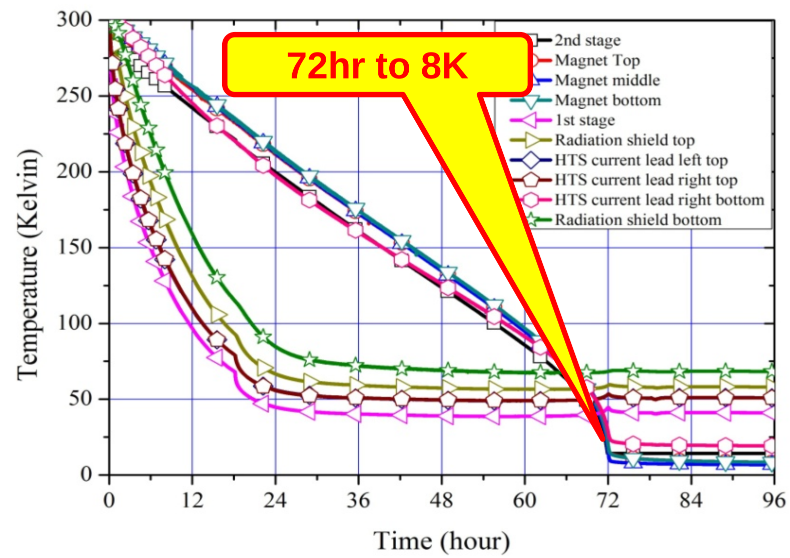
4T, 203 mm diameter RT bore cryogen free magnet

Superconducting magnet parameter			
Conductor	Width; Thickness	[mm]	4.1(12.1); 0.21(0.1)
	Ic @ 20 K, B⊥=1.5 T	[A]	> 180A
Coil	# of DP coils, (4mmW; 12mmW)		**28; 2**
	turn per pancake		133
	Winding i.d.; o.d.;	[mm]	245(274); 300.9
	Overall height	[mm]	452
	Conductor per DP (4mmW; 12mmW)	[m]	**232; 255**
	Total Conductor (4mmW; 12mW)	[m]	**6,496; 510**
Operation	B_c	[T]	4.0
	I_{op}	[A]	205
	T_{op}	[K]	8
Cryostat	Clear bore	[mm]	**203**
	Cold bore	[mm]	245





(1P- LS3-06, Mon. Afternoon)

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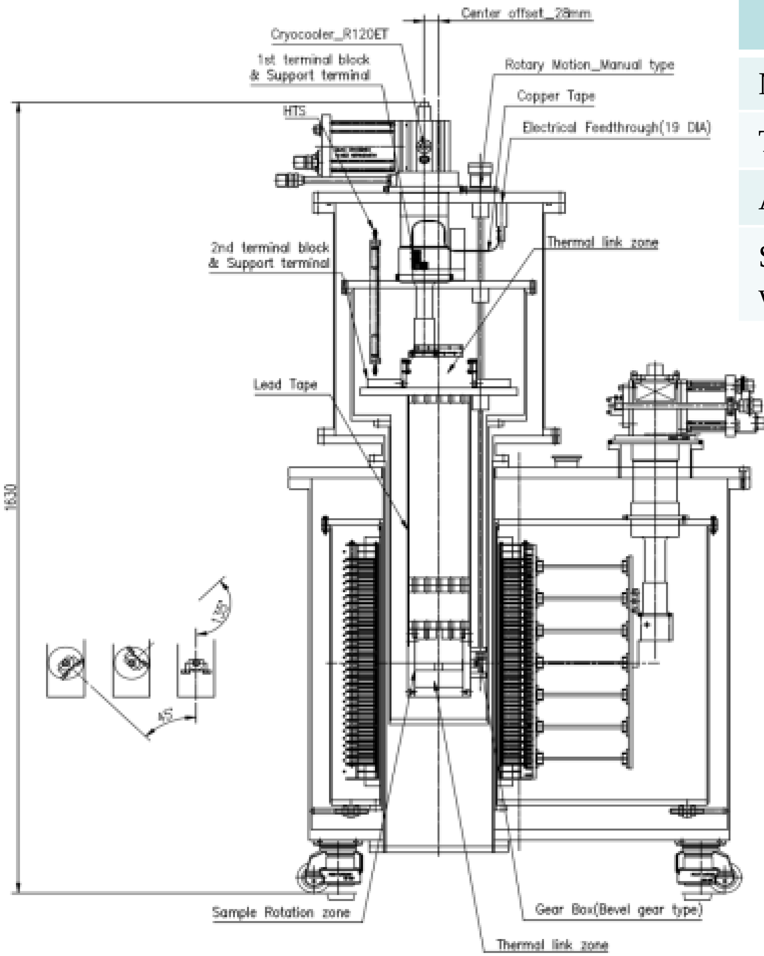
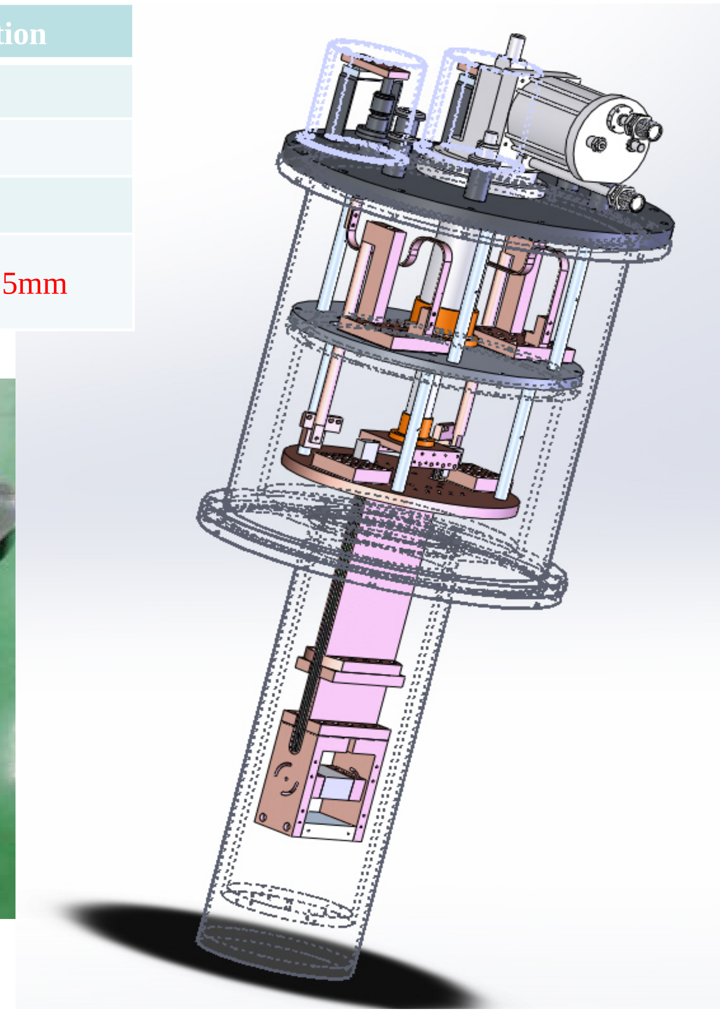
Development of Ic (B, T, θ) measurement system



Parameters	Specification
Maximum current	1000A
Temperature	12K ~ 70K
Angle	0~135º
Sample length, width	30 ~ 90mm, <15mm



Direction of Technology Development in the Future

"Increasing Demand for HTS 2G wire has surpassed the supply"

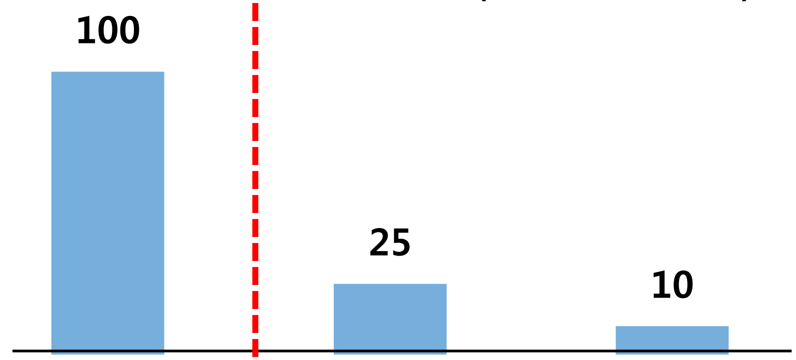
"For market entrance $ 50 / kAm is the threshold "

"Price Reduction will ignite an exponential growth of demand for HTS 2G wire"

"High throughput, low material cost, High yield is 3 Critical Success Factor"

Price Reduction

(Unit: USD / kAm)



Width :	12 mm	120 mm	360 mm
Capacity :	1,000 km/y	15,000 km/y	75,000 km/y
Max Revenue :	$ 20 Mil.	$ 75 Mil.	$ 150 Mil.
CAPEX* :	$ 7 Mil.	$ 20 Mil.	$ 30 Mil.
	Achievable with Existing Line of SuNAM		

* Capital Expense : Required Investment in Production Line

SuNAM

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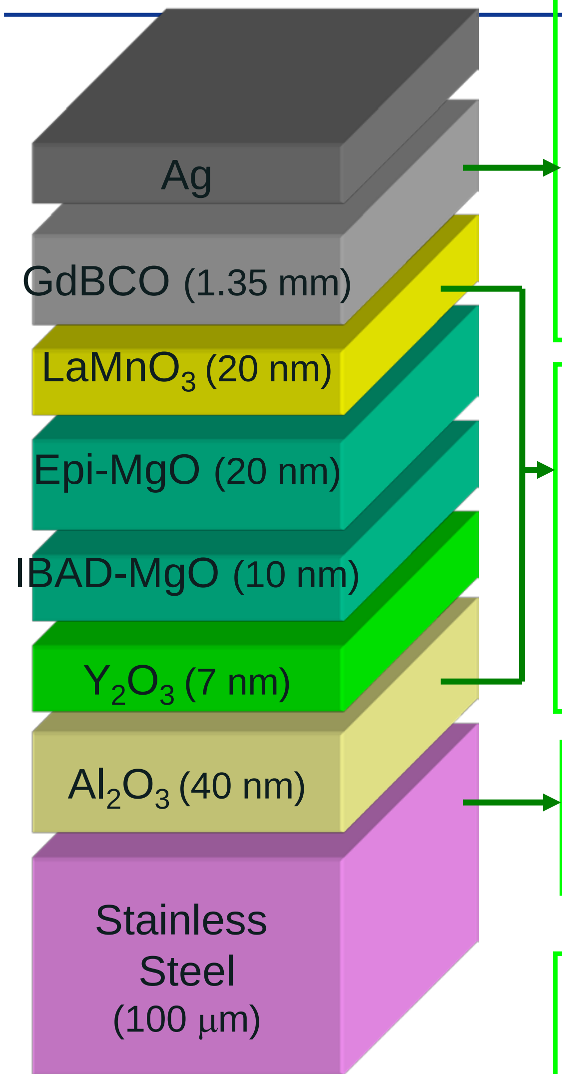

- Superconducting layer : RCE-DR
  - Low material cost, high throughput process
  - Easy to scale up
  - Typical Ic : ~ > 150A/4 mm width (t = 1.3 ㎛), & max. Ic ~ 318 A/4 mm width (t = 1.8 ㎛)

- Textured buffer based on IBAD-MgO
  - Fast & reproducible process
  - Because of small thickness(~ 100 nm total), process cost is relatively low
  - Possible to use various kind of substrates

- Low cost(~1/5 of Hastelloy), high performance non-magnetic STS substrate

- High Ic tape (for ac & dc cables) & good in B-field property tape with APC(for rot. machines & magnets) are available.

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- Korea Polytech. Univ. : G. W. Hong.
- Stanford University : R. H. Hammond.
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Thanks for Attention !