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Demonstration of a 1000-fold voltage multiplier using double-flux-quantum generation

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Abstract. We demonstrate operation of a 1000-fold voltage multiplier designed for single-flux-quantum (SFQ) digital-to-analog converters (DACs). The voltage multiplication is based on the double-flux-quantum amplifier (DFQA) that was originally proposed by Herr in 2005 for wide bandwidth signal transmission from Josephson circuits to semiconductor electronics. A DFQA is composed of stacked three-junction (3J) loops. Each 3J-loop includes two critically-damped Josephson junctions and one under-damped Josephson junction. In the first 3J-loop stage, one DFQ is generated at the under-damped junction for one input SFQ, resulting in one SFQ reflection. The reflected SFQ is transferred to the 2nd 3J-loop, and induces double-flux-quantum generation there. N-fold voltage multiplication is realized using an $(N-1)$-stage DFQA. Although the possibility of quantum amplification was noted in the original paper, the accuracy of voltage multiplication was not evaluated. We have designed and fabricated a 999-stage DFQA using a Nb/AlO_x/Nb integration technology. In experiments, we have used two methods for feeding the input SFQ pulse train. The one is an over-biasing method; the input SFQ pulse train is generated at an over-biased input junction. 1000-fold voltage multiplication with errors less than $\pm 1\%$ has been confirmed for the input voltages of up to 27 μV, of which the corresponding Josephson frequency is 13 GHz. In the other method, a dc/SFQ converter is used for feeding the input SFQ pulse train. 1000-fold voltage multiplication with an error of -0.03% has been obtained for the input frequency of 600 MHz, of which the corresponding Josephson voltage is 1.2 μV.

1. Introduction

Josephson voltage standards are being extended from dc to ac voltage [1] using programmable binary-weighted arrays [2] or a pulse-driven array of Josephson junctions [3]. Digital-to-analog conversion using single-flux-quantum (SFQ) digital technologies is another candidate for ac voltage standards [4, 5, 6, 7, 8]. Because of its ultrafast digital signal processing [9, 10], an SFQ-based digital-to-analog converter (DAC) is expected to synthesize a sinusoidal voltage waveform beyond 1 MHz.

There are two types of SFQ-based-DACs proposed so far. The first one is based on switching of the multiplication factor in a voltage multiplier (VM) stage. This type of DAC consists of three subsystems: a pulse-number multiplier (PNM), a pulse distributor (PD), and a VM [8]. Its analog output voltage $V_{\rm OUT}$ is expressed as $V_{\rm OUT} = \Phi_0 N(t) m f_{\rm RIN}$, where Φ_0, $N(t)$, m, and $f_{\rm RIN}$ are a flux quantum, the number of working VM cells, the multiplication factor in the PNM, and the repetition frequency of the reference SFQ train, respectively. Among these parameters, $N(t)$ is a variable to change $V_{\rm OUT}$, which is controlled by the PD with an external digital code.

The second one is based on frequency modulation of the output SFQ pulse train [5, 7], where the multiplication factor in the PNM, $m(t)$, is a variable. The analog output voltage $V_{\rm OUT}$ is expressed as $V_{\rm OUT} = \Phi_0 N m(t) f_{\rm RIN}$. Recently, the authors designed and operated a 5-bit quasi-sinusoidal voltage waveform generator comprising frequency-modulation-based DAC integrated with a code generator on the same chip [11]. A 16-step quasi-sinusoidal voltage waveform of 10 μV peak-to-valley was demonstrated using Nb/AlO$_x$/Nb integrated circuits. Its small output voltage was mainly due to the absence of a VM, i.e., $N = 1$.

In general, the maximum repetition frequencies in SFQ circuitry using Nb/AlO$_x$/Nb junctions are limited up to 10–50 GHz, depending on the fabrication technologies. (It was set at 10 GHz in our 5-bit quasi-sinusoidal voltage waveform generator [11].) Consequently, the product of $\Phi_0 f_{\rm RIN} m(t)$ becomes 20–100 μV at most, and thus, a 1000-fold VM is required for the output voltages of tens of mV. So far, operation of a 1023-fold VM comprising 1023 voltage mirrors has been demonstrated for DACs of the VM-switching type [12], where the voltage mirror is a combination of an input Josephson transmission line (JTL) and an output dc-superconducting quantum interference device (dc-SQUID). A drawback of the voltage-mirror-based VM is that its bias current is in proportion to its multiplication factor. Actually, the bias current of the 1023-fold voltage-mirror-based VM was as large as 0.9 A [12].

N is a fixed number in frequency-modulation-based DACs, which may allow us to employ a new type of VM devices in place of the voltage-mirror-based VM. We have focused on a double-flux-quantum amplifier (DFQA) that was proposed by Herr in 2005 [13] for a voltage driver from Josephson circuits to semiconductor electronics. It is a flux quantum multiplier, of which the stacked structure makes its bias current independent of the multiplication factor. Although Herr demonstrated its fast operation, its quantum characteristics were not fully presented in the literature.

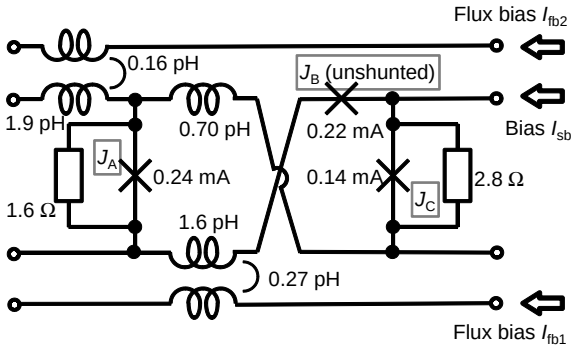

Figure 1. Equivalent circuit of a three-junction loop (3JL) working as a single-stage DFQA. An SFQ pulse is transferred from the shunted junction J_A to the shunted junction J_C via DFQ generation at the unshunted junction J_B.

To investigate its quantum voltage multiplication, we have examined the accuracies of voltage multiplication of a 20-fold, a 100-fold, and a 1000-fold VM using 19-, 99-, and 999-stage DFQA [14, 15, 16]. In this paper, we describe our recent results of a 1000-fold VM comprising a 999-stage DFQA. Its multiplication errors are evaluated for two feeding methods of the input SFQ pulse train. Uncertainties of the measured voltages are introduced to explain the spread of errors.

2. Design and fabrication of 1000-fold voltage multiplier comprising 999-stage double-flux-quantum amplifier

Figure 1 shows the equivalent circuit of a three-junction loop (3JL) working as a single-stage DFQA [13]. Three Josephson junctions, J_A, J_B, and J_C, are included in one superconducting loop. The junctions J_A and J_C are critically damped by external shunting resistors, whereas the junction J_B is under-damped with no external resistor. An input SFQ enters into the 3JL through J_A, and induces 4π phase-leap (DFQ generation) in J_B. (That is, the average input voltage across J_A is exactly doubled at J_B.) Then, the compensatory SFQ exits from the 3JL through J_C, and propagates to the next stage. Operation is tuned by three biases, one direct current bias I_{sb} and two flux biases (I_{fb1} and I_{fb2}). More detailed explanation can be found in the literature [13].

Assuming that the repetition frequency of the input SFQ pulse train is f_{IN}, the average input voltage V_{IN} is expressed as $\Phi_0 f_{IN}$. The average output voltage of a single-stage DFQA becomes $\Phi_0 f_{IN} + \Phi_0 f_{IN} = 2\Phi_0 f_{IN}$. It should be noted that the average output voltage of a two-stage DFQA is expressed as $2\Phi_0 f_{IN} + \Phi_0 f_{IN} = 3\Phi_0 f_{IN}$, not $2(2\Phi_0 f_{IN}) = 4\Phi_0 f_{IN}$. That is, the number of 3JLs for realizing N-fold multiplication is $N - 1$. We need to integrate 999 3JLs for a 1000-fold DFQA.

Figure 2(a) shows the configuration of the test circuit. We have prepared two methods for introducing SFQ pulse train into the circuit. One method uses a single Josephson junction (input junction) over-biased by an external dc current source. The

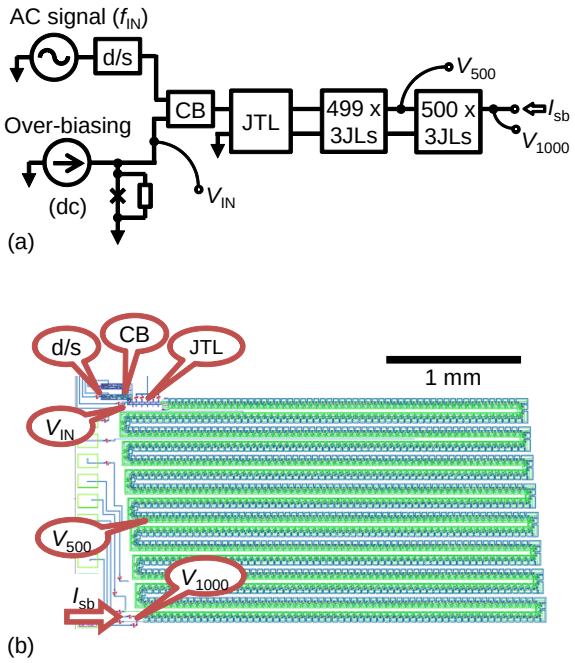

Figure 2. (a) Configuration of a 1000-fold voltage multiplier comprising 999 3JLs. Two methods are possible for introducing SFQ pulse train into the circuit; via a single junction over-biased by a dc current source, or via a dc/SFQ (d/s) converter driven by an ac current source. Two input paths are merged at a confluence buffer (CB). Nine JTL sections are inserted between the CB and the 1st 3JLs. The average voltages of the input ($V_{\rm IN}$), the output from the 499th 3JL (V_{500}), and the output from the 999th 3JL (V_{1000}) are measured. Two flux biases are also supplied although they are not shown. (b) CAD layout.

average input voltage $V_{\rm IN}$ is measured using a digital multimeter (DMM). The output voltages from the 499th (V_{500}) and the 999th 3JL (V_{1000}) are also measured using DMMs. The input SFQ pulse repetition frequency $f_{\rm IN}$ is calculated as $V_{\rm IN}/\Phi_0$. The other method uses a dc/SFQ (d/s) converter driven by an external ac current source. The input voltage is calculated as $\Phi_0 f_{\rm IN}$, while the output voltages from the 999th 3JL (V_{1000}) is measured using a DMM.

Test chips were fabricated using the National Institute of Advanced Industrial Science and Technology (AIST) Nb 2.5 kA/cm^2 standard process 2 (STP2). Four Nb layers are available in the AIST-STP2. Figure 2(b) shows the CAD layout. 999 3JLs are placed with eight clockwise and seven counterclockwise turns. To reduce stray capacitance, the bottom Nb layer beneath each 3JL is electrically isolated by grid moats [13].

In measurements, test circuits were cooled at 4.2 K in liquid helium. A two-layer magnetic shield of μ-metal cans reduced the residual magnetic field on the chip to less than 10^{-7} T.

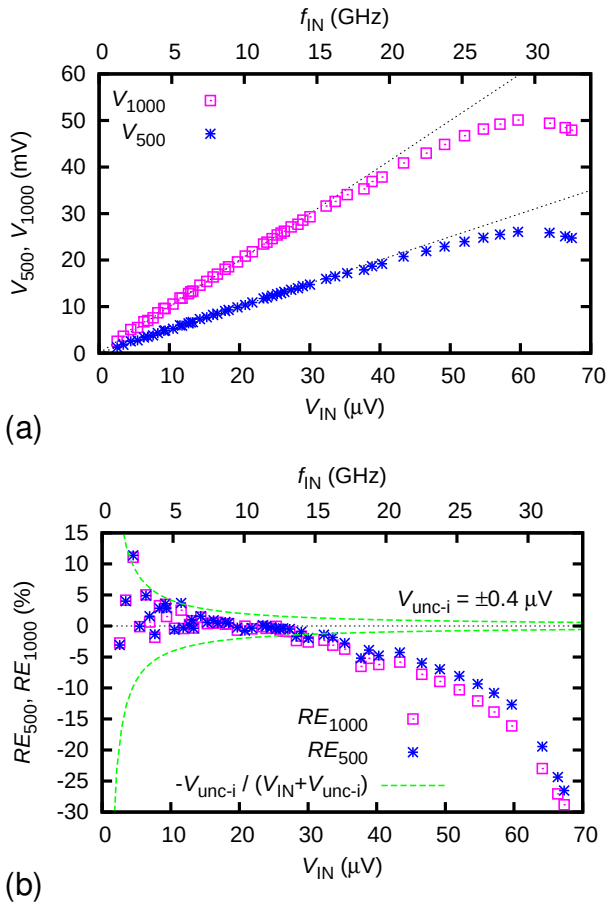

Figure 3. (a) Input-output characteristics obtained using the over-biasing method. The lower and upper horizontal axis mean the input average voltage $V_{\rm IN}$ and the calculated repetition frequency $f_{\rm IN}$ of the input SFQ pulse train. Both V_{500} and V_{1000} are plotted. The dotted lines represent the ideal relationships for 500-fold and 1000-fold voltage multiplication. (b) Relative errors plotted as functions of $V_{\rm IN}$. The relative errors are defined as $RE_{500} = \{(V_{500} - 500V_{\rm IN})/500V_{\rm IN}\} \times 100\%$ and $RE_{1000} = \{(V_{1000} - 1000V_{\rm IN})/1000V_{\rm IN}\} \times 100\%$. The dashed curves represent the relative errors given by $-V_{\rm unc\text{-}i}/(V_{\rm IN} + V_{\rm unc\text{-}i})$, where $V_{\rm unc\text{-}i}$ is the uncertainty of the measured input voltage $V_{\rm IN}$. The uncertainty of the measured output voltages is neglected.

3. Results and Discussion

3.1. Input-output characteristics measured using the over-biasing method for feeding the input SFQ pulse train

We first adopted the over-biasing method to feed the input SFQ pulse train. The input-output characteristics are shown in Fig. 3(a). The output voltages V_{500} and V_{1000} follow the ideal lines of $500V_{\rm IN}$ and $1000V_{\rm IN}$ for $V_{\rm IN}$ below 27 μV. (That is, 1000-fold voltage multiplication is seen below 27 μV.) Above 27 μV, both V_{500} and V_{1000} become smaller than the ideal values.

To investigate multiplication errors, the relative errors RE_{500} and RE_{1000} are plotted in Fig. 3(b) as functions of $V_{\rm IN}$, where RE_{500} and RE_{1000} are defined as $\{(V_{500}-500V_{\rm IN})/500V_{\rm IN}\}\times 100\%$ and $\{(V_{1000}-1000V_{\rm IN})/1000V_{\rm IN}\}\times 100\%$, respectively.

In the $V_{\rm IN}$ range from 15 to 27 μV, RE_{500} and RE_{1000} are both within the $\pm 1\%$ range, where the multiplication factors are confirmed to be $495 < V_{500}/V_{\rm IN} < 505$ and $990 < V_{1000}/V_{\rm IN} < 1010$.

When $V_{\rm IN}$ is below 15 μV, RE_{500} and RE_{1000} deviate to the outside of the $\pm 1\%$ range. We attribute these large errors mainly to uncertainties of the measured $V_{\rm IN}$ values. Assuming that the 1000-fold multiplication is perfect ($V_{1000} = 1000V_{\rm IN}$) and that uncertainties of the measured V_{500} and V_{1000} values are neglected, the relative errors caused by the uncertainty of the measured input voltage ($V_{\rm unc\text{-}i}$) is expressed as $\{V_{1000} - 1000(V_{\rm IN} + V_{\rm unc\text{-}i})\}/\{1000(V_{\rm IN} + V_{\rm unc\text{-}i})\} = -V_{\rm unc\text{-}i}/(V_{\rm IN} + V_{\rm unc\text{-}i})$. Two dashed curves in Fig. 3(b) show the relative errors for $V_{\rm unc\text{-}i}$ of ± 0.4 μV, between which the RE_{500} and RE_{1000} data fall.

For $V_{\rm IN} > 27$ μV, RE_{500} and RE_{1000} go below the -1% line with increasing $V_{\rm IN}$. Furthermore, it is clearly seen that the RE_{1000} values are worse than the RE_{500} values at the same $V_{\rm IN}$. The difference between RE_{1000} and RE_{500} at the same $V_{\rm IN}$ is increased as $V_{\rm IN}$ increases up to 65 μV. This difference indicates that the operation errors occur between the 499th and 999th 3JL, while RE_{500} is attributed to the errors between the 1st and the 499th 3JL. Two curves of RE_{500} and RE_{1000} suggest that the operation errors between the 1st and 499th 3JL is dominant for $27 < V_{\rm IN} < 65$ μV. For $V_{\rm IN} > 65$ μV, both RE_{500} and RE_{1000} deteriorate more rapidly, while the difference between them shrinks.

From the results shown in Figs. 3(a) and (b), we may conclude that the 999-stage DFQA works as a 1000-fold VM for $V_{\rm IN}$ of up to 27 μV. The corresponding $f_{\rm IN}$ is 13 GHz. On the other hand, our numerical simulation suggests that the maximum $f_{\rm IN}$ value lies between 34 and 36 GHz. The difference between the numerical and experimental maximum $f_{\rm IN}$ value is attributed mainly to the imperfect inductance layout at the counterclockwise turns. We have checked the maximum $f_{\rm IN}$ values of 19-stage DFQA including either three clockwise turns or three counterclockwise turns, of which the results are 34 and 14 GHz, respectively. It is necessary to redesign the layout of the 3JL cell for the counterclockwise turn to improve the maximum operation frequency.

3.2. Input-output characteristics measured using a dc/SFQ converter for feeding the input SFQ pulse train

In the measurements using the over-biasing method, the uncertainties of the measured input voltage $V_{\rm unc\text{-}i}$ are likely to limit the accuracy of the measured multiplication factor. To avoid the uncertainties of $V_{\rm IN}$, we have tried to feed the input SFQ pulse train using a dc/SFQ converter.

Figure 4 shows the $f_{\rm IN}$-V_{1000} and $f_{\rm IN}$-RE_{1000} characteristics obtained using a dc/SFQ converter for feeding the input SFQ pulse train. The input voltage $V_{\rm IN}$ and

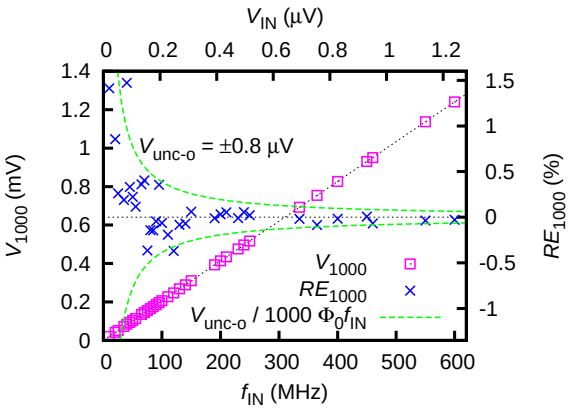

Figure 4. f_{IN}-V_{1000} and f_{IN}-RE_{1000} characteristics obtained using a dc/SFQ converter. The lower and upper horizontal axis mean the frequency f_{IN} of the ac current source and the calculated average voltage V_{IN}. 1000-fold voltage multiplication is obtained for f_{IN} from 10 to 600 MHz. The dashed curves represent the relative errors given by $V_{\mathrm{unc\text{-}o}}/1000\Phi_0 f_{\mathrm{IN}}$, where $V_{\mathrm{unc\text{-}o}}$ is the uncertainty of the measured output voltage V_{1000}.

the relative error RE_{1000} are calculated as $V_{\mathrm{IN}} = \Phi_0 f_{\mathrm{IN}}$ and $RE_{1000} = \{(V_{1000} - 1000\Phi_0 f_{\mathrm{IN}})/1000\Phi_0 f_{\mathrm{IN}}\} \times 100\%$, respectively.

In measurement, the maximum input frequency for 1000-fold voltage multiplication was 600 MHz, where the RE_{1000} value as small as -0.03% was obtained. Beyond 600 MHz, it was not possible to confirm stable operation, because the multiplication factor was strongly dependent on the amplitude of the ac signal source. The bandwidth of our experimental setup seemed to be insufficient for the input frequencies beyond 600 MHz.

For $130 \leq f_{\mathrm{IN}} \leq 600$ MHz, the RE_{1000} values fall within $\pm 0.1\%$, where the multiplication factor is confirmed to be $999 < V_{1000}/V_{\mathrm{IN}} < 1001$. When f_{IN} is below 130 MHz ($V_{\mathrm{IN}} < 0.27$ μV), the RE_{1000} data deviate to the outside of the $\pm 0.1\%$ range. We attribute these errors to the uncertainty of the measured V_{1000} values. Assuming that the 1000-fold multiplication is perfect and that the dc/SFQ converter works with no errors, the relative errors caused by the uncertainty of the output voltage ($V_{\mathrm{unc\text{-}o}}$) is expressed as $\{(1000\Phi_0 f_{\mathrm{IN}} + V_{\mathrm{unc\text{-}o}}) - 1000\Phi_0 f_{\mathrm{IN}}\}/1000\Phi_0 f_{\mathrm{IN}} = V_{\mathrm{unc\text{-}o}}/1000\Phi_0 f_{\mathrm{IN}}$. Two dashed curves in Fig. 4 show the relative errors for $V_{\mathrm{unc\text{-}o}}$ of ± 0.8 μV, between which the RE_{1000} data fall.

We also evaluated the margin of the direct bias I_{sb} using the dc/SFQ converter. After adjusting the two flux biases, we swept I_{sb} and measured V_{1000} for f_{IN} of 50, 100, and 600 MHz. The results are shown in Fig. 5. For f_{IN} of 50 and 100 MHz, 1000-fold multiplication with errors less than $\pm 0.1\%$ are confirmed at $0.348 \leq I_{\mathrm{sb}} \leq 0.382$ mA and $0.356 \leq I_{\mathrm{sb}} \leq 0.378$ mA, respectively. Their margins are calculated as $\pm 4.7\%$ and $\pm 3.0\%$ for their center values. For $f_{\mathrm{IN}} = 600$ MHz, on the other hand, the 1000-fold multiplication with errors less than $\pm 1\%$ is confirmed at $0.378 \leq I_{\mathrm{sb}} \leq 0.380$ mA, of which the margin is $\pm 0.3\%$. The inaccurate multiplication with the small bias margin

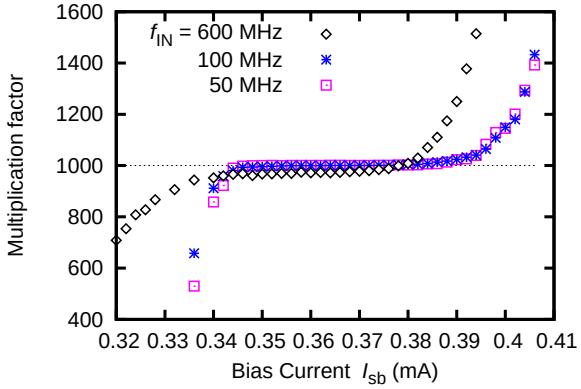

Figure 5. Dependence of the multiplication factor on $I_{\rm sb}$ for $f_{\rm IN}$ of 50, 100, and 600 MHz. $I_{\rm fb1}$ and $I_{\rm fb2}$ for the flux biases are set at 1.45 and 1.26 mA, respectively.

for $f_{\rm IN}$ = 600 MHz is probably due to poor adjustments of the flux biases in this measurement, because the RE_{1000} value of -0.03% has been confirmed for $f_{\rm IN}$ = 600 MHz as shown in Fig. 4. Crosstalk coupling in the experimental setup could reduce operation margins.

For DAC applications, precise evaluation of a 1000-fold VM is necessary for $f_{\rm IN}$ of 10 GHz. Since it is difficult to feed a 10-GHz SFQ input pulse train directly via a dc/SFQ converter, a PNM should be introduced for such high-frequency evaluation. We have evaluated the output voltage of a 6-bit triangle voltage waveform generator including a 64-fold PNM and a 9-stage (10-fold) DFQA [17], in which the relative error less than 0.03% is confirmed for the nominal SFQ repetition frequency of 10 GHz. The accuracy of a 1000-fold VM will be checked in a similar way.

4. Conclusion

We demonstrated 1000-fold voltage multiplication using a 999-stage DFQA. DFQ generation at under-damped Josephson junctions realizes the quantum voltage multiplication. The input-output characteristics were evaluated using Nb/AlO$_x$/Nb Josephson integrated circuits. Two methods were employed for feeding the input SFQ pulse train. The first one was the over-biasing method. 1000-fold voltage multiplication with relative errors less than $\pm 1\%$ was confirmed for the input voltages of up to 27 μV. It was shown that the multiplication accuracies for the input voltage smaller than 15 μV were limited by the uncertainty of the measured input voltages. In the second method, a dc/SFQ converter was used for feeding the input SFQ pulse train. 1000-fold voltage multiplication with relative errors less than $\pm 0.1\%$ was confirmed for the input frequencies of up to 600 MHz. The total bias current supplied to the 999-stage DFQA was approximately 3 mA, which was two orders of magnitude less than that of the voltage-mirror-based 1023-fold VM. Although further evaluation is still required, the results demonstrate potential performance for frequency-modulation-based SFQ DACs.

Acknowledgments

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