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Design and Evaluation of Flash ADC

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***Abstract*— We have designed single-bit comparators and multi-bit flash ADCs using three flavors of periodic comparators; one flavor uses a differential "quasi-one-junction" SQUID (DQOS) comparator, the second use a differential SQUID wheel comparator and the third uses a symmetric differential SQUID wheel comparator with time-interleaved clocks. We have also developed a new performance analysis scheme that enables full reconstruction of input signal using a single-bit comparator. The signal is reconstructed based on multiple beat frequency measurements that track the position of the comparator thresholds in response to a DC offset to the input signal. In addition, to eliminate the frequency dependent distortions resulting from impedance mismatches over wide bandwidths, the signal and clock distribution network have been optimized using EM simulations. For distributing the clock signal to the multi-bit comparators, a 50 ohm coplanar transmission line has been designed. Test results for a 1-bit comparator using a differential SQUID wheel comparator demonstrates a performance of 4.5 bits of resolution in Gray code for a beat frequency test using a 20 GHz input signal and 5.3 bits for 10 GHz input. 4-bit and 8-bit versions of the flash ADC with a DQOS comparator and a 3-bit time-interleaved ADC using the SDSW comparator have also been designed. The DQOS ADC has been tested up to 25 GHz input signal frequency with performance of 4.3 bits of resolution in Gray code for 19.7 GHz input signal. The time-interleaved ADC performance is 4.3 bits for a 15 GHz beat frequency test with an effective sampling rate of 30 GHz.**

***Index Terms*— Flash ADCs, periodic comparators, Analog-to-Digital Converter, SQUID Wheel.**

I. Introduction

THE RECENT YEARS have seen an unprecedented increase in the demand for the spectrum resulting in opening up of higher frequency bands, both for commercial and military applications. An array of applications will benefit from extremely wideband analog-to-digital converters (ADCs) supporting an instantaneous bandwidth from HF to well over Ka band. Dynamic band bandwidth allocation, spectrum monitoring, sensor readout, digital oscilloscope, and transient digitizers are some of the example applications.

Very high sampling speed superconductor ADCs, utilizing periodic comparators that reduce hardware complexity [1-6], have a discriminating advantage for high instantaneous bandwidth applications. Towards this goal, we have been developing and evaluating three flavors of the periodic flash comparators that are differential quasi-one-junction (DQOS) SQUID comparator, differential SQUID wheel comparator (DSW), and the symmetric differential SQUID wheel comparator (SDSW) comparator.

The following section describes a performance evaluation technique for 1-bit flash comparator using beat frequency measurements. Section III describes optimization and measurement results for the signal and clock distribution network for flash ADCs. Section IV reports design and experimental measurement results for the three flavors of the comparator and multi-bit ADCs.

II. Evaluation of 1-bit Comparator using Signal Reconstruction from Beat Frequency Measurement

Performance of superconductor flash comparators has been traditionally evaluated using beat frequency measurements. While beat frequency measurements are useful for preliminary study of comparator distortions and performance, it is hard to quantify the distortions or to study their correlation with the applied input signal. A more powerful technique including full signal reconstruction for a 1-bit comparator using beat frequency simulation was reported in [6]. A similar scheme can be followed to analyze the test results for the comparator. One starts with a single periodic comparator running a conventional beat-frequency test using a sinusoidal input data signal, with an independent dc offset, and observes its output. The output toggles in response to linearly changing clock-to-data phase difference (from the frequency offset), but also depends on the dc offset applied to the signal. Thus, for a selected clock-to-data phase difference, one can capture multiple beat frequency measurements by slowly sweeping the DC offset applied to the signal and tracking the position of the thresholds (0-to-1 and 1-to-0 transitions). When a Φ_0-periodic comparator is used in this experiment, it yields multiple reconstructed traces that repeat Φ_0-periodically along the Y axis. Each full period corresponds to 2π change of the comparator input phase and contains two different traces, one for 0/1 and another for 1/0 threshold respectively. Fig. 1 marks one vertical 2π period of such family of wrapped traces obtained using multiple beat frequency measurements at 20 GHz. The amplitude of signal in this experiment was not optimized for maximum performance and resulted in only eight transitions in a beat frequency period.

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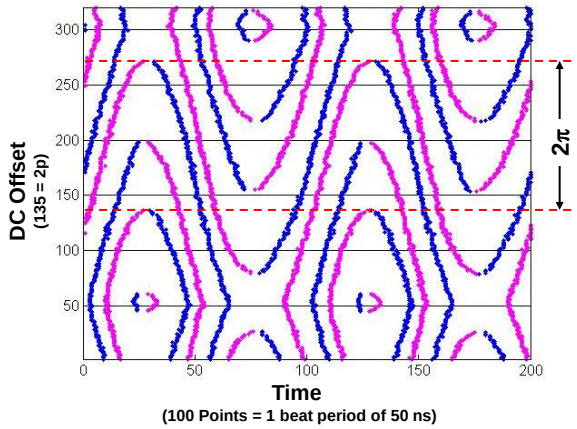

Fig. 1. Wrapped reconstruction of a sinusoidal input signal obtained using multiple beat frequency measurements by sweeping the DC offset applied to the signal and plotting the threshold positions for each measurement. The DC offset is Φ_0 periodic, with 2π corresponding to 135 units of DC offset.

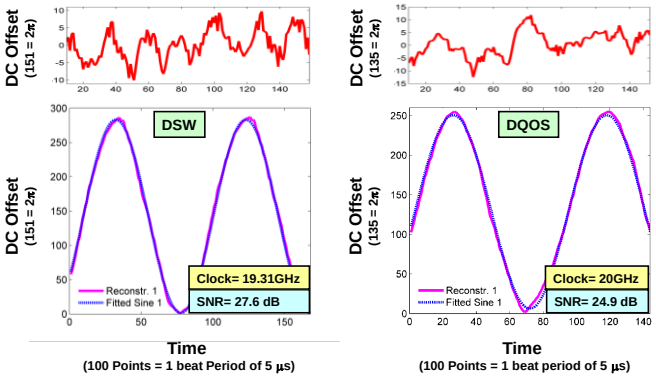

Fig. 2. Unwrapped signal reconstruction of a sinusoidal input signal for (a) the DSW and (b) the DQOS comparator.

When the traces are unwrapped, they yield the full reconstruction of the input waveform. Fig. 2 shows performance comparison of two such reconstructions for the DSW and DQOS comparators [6]. The SNR measured using sine-fit shows a 2.7 dB improved performance using a DSW comparator. The top trace plots the comparator distortions obtained from subtracting the reconstructed waveform from the sine fit.

III. Multi-bit Flash ADC

In order to design the multi-bit flash ADC, the signal and clock need to be distributed to the multiple comparators. The section below describes the design and evaluation of the signal and clock distribution networks.

A. Resistive Divider (R-2R Network)

In every fabrication process the resistive metal layer provides a certain resistance per square depending on the resistive material and the thickness of the layer. At low frequencies, the desired resistance can be realized simply by creating a rectangle with the proper number of squares. However the resistance value varies considerably over a wide frequency range as a result of the inductance of the line and parasitic capacitances to ground. Fig. 3**Error! Reference source not found.** shows the 3-D model and the EM simulation results for a 1-port, 50 Ω load (load A) from DC to 40 GHz. Simulation results show the input impedance and the imaginary part of the load over a wide frequency range. For design A, the impedance varies from 50 Ω at DC to more than 100 Ω at 40 GHz.

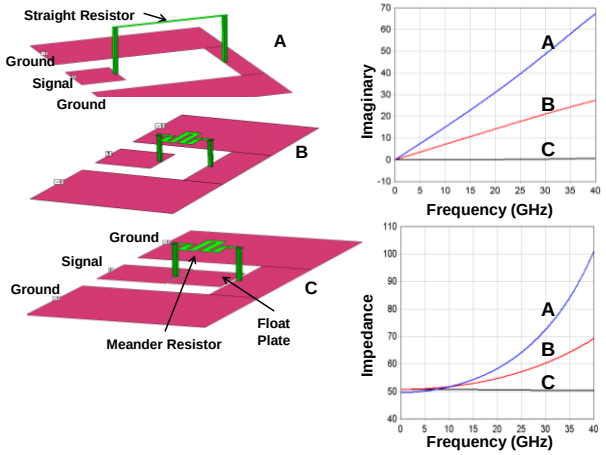

Fig. 3. The 3-D model and EM simulation for three flavors of resistor design are shown. A meander shaped resistor with a floating plate is designed to cancel out the imaginary component of the impedance.

In order to realize a frequency independent resistive power divider, the first step is to design the individual resistors to have almost constant resistance over the desired frequency range. To address this matter, a meander shaped resistive line is designed [7]. The magnetic field generated by each leg of the meander line can be cancelled out to a great extent by the magnetic field in the opposite direction from the adjacent leg provided that the gap between the legs is small enough. A 50 Ω load using this technique is designed and simulated (design B). To minimize the remaining inductance of the line a float metal plate can be added on top or beneath the resistive line (design C). Note that over the same frequency range, design C shows less than 1 Ω variation in the input impedance which is a significant improvement compared to design A.

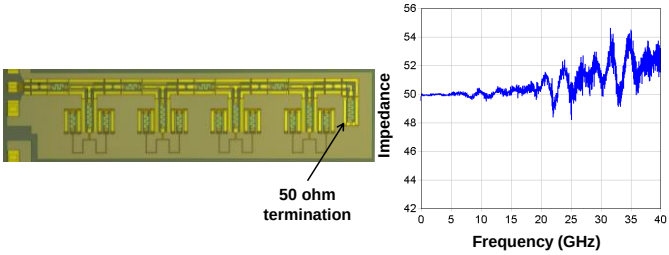

Fig. 4. Layout of a 1-port resistive ladder network with four branches (left). Measured results for the impedance of the resistive network (right).

For characterizing resistive ladder networks to be used with multi-bit ADCs, R-2R ladder with four legs were designed, fabricated, and measured based on the meander resistor with the floating plate. Fig. 4 shows the layout of a 1-port design which is terminated in 50 Ω. The resistive network is measured over a frequency range of 40 GHz in the lakeshore probe station at 4K. The resistance of the network is almost constant up to 20 GHz and shows small variation (about 6%) up to 40GHz as shown in the measured results.

B. Signal Distribution Network

The signal from each branch of the resistive ladder is coupled to the comparator using a multi turn transformer in order to improve the comparator sensitivity. A four turn

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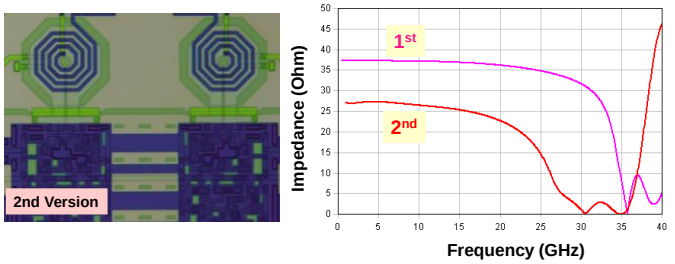

Fig. 5. 3-D model for the input signal transformer (left). EM simulation results for two flavors of the transformer.

transformer is used for current amplification and to feed differential signal to the complementary quantizers. A ~ 1.25 pH shunt inductor is used to shunt both ends of the secondary inductance of the transformer that effectively reduces the β_L of the circuit. A DC bias current injected at the center of the transformer secondary is used as a common mode phase bias. The primary of the transformer (Fig. 5, left) is designed as a stripline with 25 ohm impedance. Fig. 5, right shows EM simulation result for two versions of the transformer. The first version has a higher bandwidth, but is not matched to the desired impedance. In the second flavor, the bandwidth is sacrificed to achieve the desired impedance. The input signal sensitivity is 0.48 mA to couple a Φ_0 to the comparator.

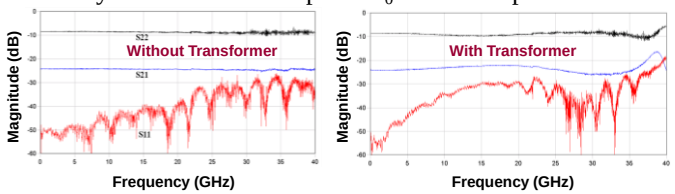

Fig. 6. S-parameter measurement results from a two-port signal distribution network without the transformer (left) and with the transformer (right).

To characterize the transmitted signal through the resistive ladder network and the transformer, we designed two variants of the signal distribution network, one without the transformer and the other including the transformer. Each design is a 2-port network including four branches of the R-2R ladder. Fig. 6 shows the measured results. As expected, for a 4-branch resistive ladder network, an insertion loss of 24 dB is measured at the output of the 2-port network. The optimized design of each resistor in the network provides a constant insertion loss from DC to 40GHz. With the transformers included, variation of the measured insertion loss seen at higher frequencies is due to the inductance of the transformers.

C. *Clock Distribution Network*

The clock distribution network consists of a coplanar transmission line that couples the clock signal to individual DC-to-SFQ converters that clock the individual comparators. EM simulation was used to design a two-turn coil matched to 50 ohm impedance.

IV. Design and Test Results for Flash ADC

We laid out three flavors of the flash comparator: a) differential quasi-one-junction SQUID comparator (DQOS), b) differential SQUID wheel comparator (DSW), and c) symmetric differential SQUID wheel comparator (SDSW) [6].

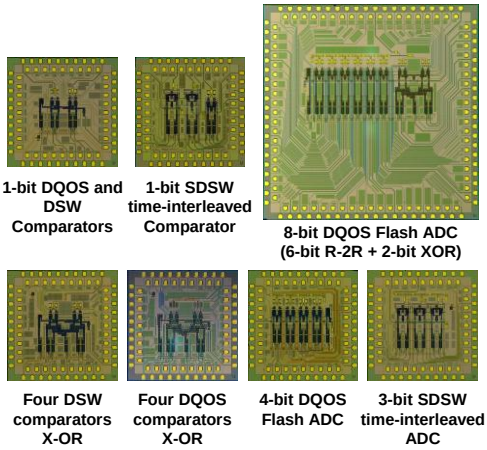

Fig. 7. Flash ADC chipset showing test circuits for different flavors of the comparator and multi-bit ADCs.

Each design incorporates the improved signal and clock distribution networks. Fig. 7 shows several 5mm x 5mm chips including test circuits for three flavors of 1-bit comparators, threshold interleaving of four comparators using the DQOS and DSW comparators, and multi-bit ADC chips using the DQOS comparator and the time-interleaved ADC using the SDSW comparator. Also shown is a 1cm x 1cm chip incorporating an 8-bit flash ADC using the DQOS comparator. The 8-bit ADC is constructed using a 6-bit section with an R-2R ladder and additional 2-bits of least significance coming from threshold interleaving four comparators. The DQOS and DSW comparators use a single transformer to inject the differential signals, whereas the SDSW comparator using time interleaved clocks uses two transformers with reversed polarity to inject the differential signals. The test circuits for each comparator are designed with two comparators per bit with an independent bias to phase shift threshold of one comparator with respect to another. The chip has been fabricated using the standard HYPRES Nb process with critical current density (J_c) equal to 4.5 kA/cm^2 [9] and was tested in liquid helium.

We performed a beat frequency measurement for each of the comparators [6]. The goal of the beat frequency test is to evaluate the comparator performance by determining the number of bits of resolution based on the number of transitions that can be achieved on the comparator outputs.

Fig. 8 shows the test result for the DSW comparator for different signal frequencies. The first version of the transformer was used for this measurement. At 20 GHz the comparator demonstrates 24 transitions in full period of the sine wave corresponding to 3.58 effective bits in binary code. For a Gray coded output, 24 transitions correspond to 4.58 effective bits of resolution if each threshold for every higher significant bit aligns with the center of the two thresholds of the preceding bit. In this revised design, we got a 0.5 bit improvement compared to that reported in [6]. The performance of the SDW comparator is 1.5 bit better than that reported for other superconductor flash comparators [2, 4]. The flash comparator digitizes the polarity of the quantized current from the differential QOS quantizers. 24 transitions at 20 GHz demonstrate digitization of a 240 GHz quantized current from the QOS quantizer. Further performance

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improvement is limited by the ability of the comparator to digitize higher frequency quantized current.

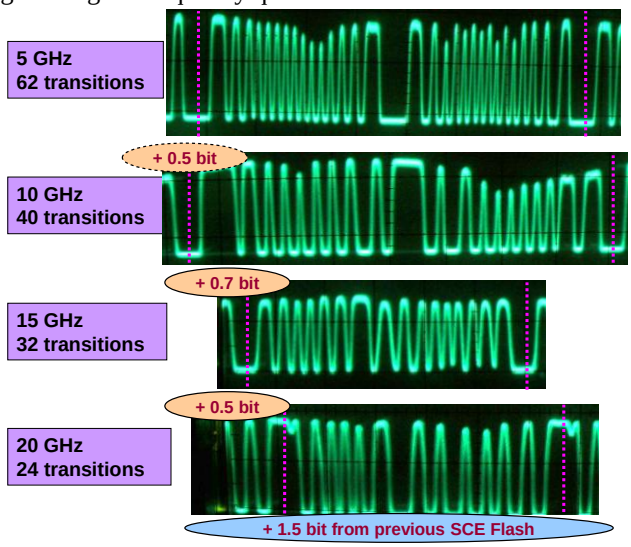

Fig. 8. Beat frequency test results for the DSW comparator for different signal frequencies biased with CMPB equal to π.

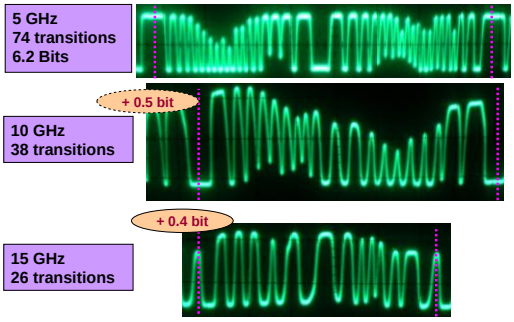

Fig. 9. Beat frequency test results for the SDSW comparator for different signal frequencies.

Fig. 9 shows the test result for the SDSW comparator at 5, 10, and 15 GHz signal frequencies. At 15 GHz the comparator demonstrates 26 transitions in full period of the sine wave corresponding to 4.7 effective bits of resolution in Gray code. The performance is 0.4 bit better than that reported in [6].

Fig. 10 shows the test results for the SDSW comparator at 15 GHz signal frequency. The comparator demonstrates 20 transitions on the LSB in full period of the sine wave. Since time interleaved clocks are used the effective sampling frequency is 30 GHz.

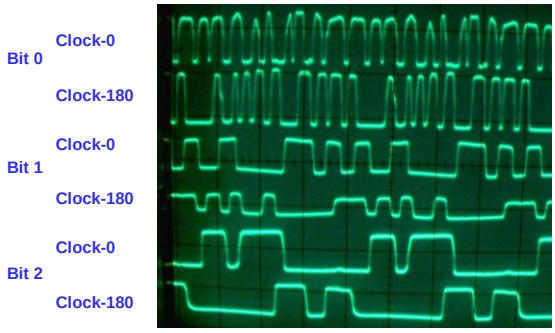

Fig. 10. Beat frequency test for a 3-bit time interleaved ADC using SDSW comparator. ADC performance at an effective sampling frequency of 30 GHz using 15 GHz time interleaved clocks has been demonstrated.

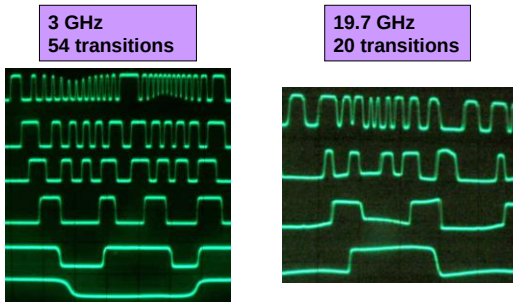

Fig. 11. Beat frequency test results for a 8-bit flash ADC using DQOS comparator have been tested up to 19.7 GHz and demonstrate 4.3 bits of resolution in Gray code.

Fig. 11 shows the test results for the 8-bit flash ADC using the DQOS comparator. At 19.7 GHz clock frequency, the comparator demonstrates 20 transitions on the LSB in full period of the sine wave corresponding to 4.3 bits of resolution in Gray code.

V. Conclusion

We have developed a powerful comparator evaluation technique that enables full signal reconstruction using a 1-bit periodic comparator beat frequency measurement. This evaluation technique enables to quantify the comparator SNR, duty cycle distortion, and sensitivity to duty DC bias, in addition to comparison with simulated reconstruction using a similar scheme. For multi-bit ADC design, the signal and clock distribution networks have been optimized using EM simulations and comparing measured test circuits with simulated results. Fig. 12 summarizes the test result for different flavors of 1-bit flash comparators and multi-bit flash ADC using the DQOS comparator. Measurement results for 1-bit DSW comparator at 20 GHz signal frequency shows 4.5 bits of resolution, an improvement of 1.5-bits over that of previously demonstrated result in superconductor technology. Time interleaved comparator and ADC that enable doubling the bandwidth have been demonstrated up to 15 GHz (effectively 30 GHz) sampling frequency. Also, an 8-bit flash ADC using DQOS comparator has demonstrated 4.3 bits of resolution at 19.7 GHz.

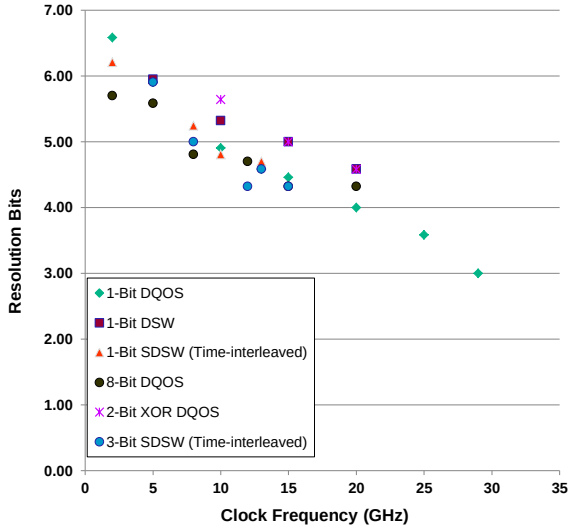

Fig. 12. Summary of test results for different flavors of flash comparator and multi-bit ADCs using beat frequency test.

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