Multi-input Synchronous Analog-to-Digital Converter

Deepnarayan Gupta, *Senior Member, IEEE*, Timur V. Filippov, Andrei Talalaevskii, Vladimir V. Dotsenko, Alf E. Lehmann, Saad Sarwana, Son Dinh, Osama Nayfeh, and Anna Leese de Escobar

***Abstract*— Integration of multiple synchronous identical superconductor analog-to-digital converters (ADCs) on a single chip or a multi-chip module is attractive for numerous applications, including Magnetic Resonance Imaging (MRI) systems. Several dual-ADC chips comprising two phase modulation-demodulation (PMD) ADCs with a common sampling clock, each connected to a digital decimation filter, have been designed. One variant with a single-junction quantizer with two-channel synchronizer and a decimation ratio of 256 has been installed in a modular cryocooled digital-RF receiver system (called ADR), operated with a common clock frequency of 20.48 GHz, and extensively tested with single and multiple input signals. Other variants have reduced decimation ratio for higher RF bands to digitize signals from higher-field MRI systems. Another variant of multi-input ADC integrated circuit chips have no on-chip filtering. We have designed and tested 2 (dual), 3 (tri), and 4 (quad) input versions of such a chip, where each ADC is followed by a deserializer circuit. A proof-of-concept multi-chip module (MCM) with 8 (octo) synchronous ADCs, consisting of four flipped dual-ADC chips on a carrier, has been designed to demonstrate scalability.**

***Index Terms*— MRI, RSFQ, ADC, MCM, Digital Receiver.**

I. Introduction

THE current trend in MRI imaging is to use an array of coils instead of a single coil covering the same area. Such parallel imaging improves sensitivity and speeds up the MRI encoding process, making even a single-echo acquisition possible. Recently, experimental systems with up to 128-channel receivers and 64-channel parallel transmitters were reported [1, 2].

The multi-channel approach combined with high sensitivity of SQUID-based sensors led to the first 7-channel system for ultralow field MRI [3]. For higher fields where the radio frequency (RF) signal is proportionately higher (the gyromagnetic constant for proton is 42.6 MHz/T), direct digitation of an *N*-element array by means of superconductor ADCs sampled at tens of GHz, followed by immediate on-chip digital processing of data streams by RSFQ-based circuitry, may have advantages over traditional systems. Such a multi-input digital receiver may provide better frequency and spatial resolutions.

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D. Gupta, T. V. Filippov, A. Talalaevskii, V. V. Dotsenko, A. E. Lehmann, and S. Sarwana are with HYPRES, Inc., Elmsford, NY 10523, USA (phone: 914-592-1190, fax: 914-347-2239, email: gupta@hypres.com)

S. Dinh, O. Nayfeh, and A. Leese de Escobar are with the Space and Naval Warfare Systems Center Pacific (SSC-Pac), San Diego, CA, USA (anna.leese@navy.mil)

The prospective system should enable discrimination of frequencies from adjacent slices and provide high spatial localization (see Fig.1). It implies that such a receiver should be capable of processing images from different slices in parallel and properly treat the phase differences (time delays) between a voxel and the spatially distributed elements of the receiver array.

On-chip (or on-MCM) digital processing may include but is not limited to copying the signal from each element into many streams and delaying of individual streams to reflect spatial distribution of coils in an array before combining data streams together. Better image reconstruction may require multiplying data streams to compensate for calibrated inequalities in array elements. This can be achieved by adding a multiplier after each delay element. Notably, by using a massively oversampled ADC with a few bits of quantization, the complexity of this multiplier can be kept relatively low. Depending on the complexity, this function can be realized using the same circuitry employed for digital mixers [4-6], look-up tables [7] and RSFQ-based digital signal processors [8-11].

Multi-input digitization assumes synchronous behavior of multiple ADCs and data processing units. In this paper, we focus on the principles of a scalable multi-input ADC design and report experimental results.

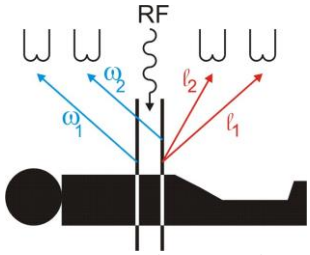


Fig. 1. Multi-input synchronous front-ends followed by RSFQ-based circuitry can improve both frequency and spatial resolutions of parallel MRI detector arrays.

II. Multi-input ADC Design

A. Design Considerations

There are various constraints on the design of a multi-input ADC with *N* identical ADCs. First, the total size of integrated circuitry is governed by the availability of the number of superconductor layers and lithographic dimensions of a fabrication process. Second, the total digital data output is limited by the digital data link rate per line (*R*). Third, the use of a standard pad layout to facilitate testing using standard apparatus limits the total number of output lines for a given chip size. For the current design, we have chosen the HYPRES 4.5 kA/cm^2 4-layer standard fabrication process

[12], 10 mm × 10 mm chip size with the standard 80-pad layout, and a maximum output data link rate of R = 2 Gbps per line.

Our first design is a dual-ADC single chip (N = 2), comprising two lowpass phase modulator-demodulator (LP-PMD) front-ends [13] and two digital decimation filter (DDF) back-ends [14]. The use of LP-PMD ADCs is appropriate in the lower range of the RF spectrum because its dynamic range is slew rate limited. This design naturally extends to N = 4, 8, and 16 through the MCM approach, each having a common front-end chip with N signal inputs and a set of N/2 dual-DDF back-end chips.

On-chip digital decimation filters reduce the total data throughput to room temperature by rejecting unwanted noise. For low field (0.1–0.4 T) MRI, a high decimation ratio (e.g. 256) can be used for typical sampling frequency of 20 GHz. Since a DDF, employing the cascaded integrator comb (CIC) architecture, naturally accepts a multi-bit binary word at the sampling clock rate from the LP-PMD ADC, its complexity does not increase sharply as the number of synchronizer channels (m) grows. For a second-order CIC DDF, the number of bits (or slices) in the filter is given by $S = \{1+\log_2(m)\}+2\log_2(f_{clk}/f_d)$, where f_{clk} is the ADC sampling clock frequency and the f_d is the output (decimated) clock frequency. Out of these, the number of significant bits (B) is given by $B \geq \{1+\log_2(m)\}+1.5\log_2(f_{clk}/f_d)$.

B. Multi-input ADC Single-chip Design

Several flavors of dual-ADC chips have been designed (Fig. 2, Fig. 3). In its most common form, the ADC front-end is a single-junction quantizer with m = 2 synchronizer channels. Two such front-ends are clocked from a common clock source, which is derived from an external source using a DC/SFQ converter. A common decimated (or Nyquist) clock is derived using a frequency divider. A pulse distribution network distributes the two data bits from each ADC to the corresponding DDF along with a common master (f_{clk}) and decimated (f_d) clocks. The output digital words from the two DDFs are applied to SQUID-stack output drivers [15] and read out in parallel. The decimation ratio (f_{clk}/f_d) for this chip is fixed at 256. Each DDF has S = 18 bits out of which B = 15 are read out through SQUID-stack output drivers.

This basic design can be extended by incorporating higher slew-rate (half-rate and quarter-rate) quantizers [16] with more synchronizer channels and an adder circuit to convert the synchronizer output to binary format. A variant of this design uses an on-chip clock source using a long Josephson junction (LJJ). Since the output data rate is fairly low (f_d = 110 MHz for f_{clk} = 28.16 GHz which is the highest sampling rate obtained to date), serialization of the digital output word [15] would simplify the chip packaging by making optimum use of data links at the expense of a slight increase in complexity.

Another variant of the dual ADC chip does not use any superconductor filters but transports all the digitized data to room temperature for further processing. To bridge the gap between ADC sampling rate and the digital data link rate, deserialization by an appropriate factor (k) is necessary. The chip shown in Fig. 3 has a 1:16 deserializer attached to each of the two LP-PMD ADC front-ends that are limited to a single synchronizer channel. The chip operates up to a clock frequency of 32 GHz with 2 Gbps data link rates. Due to the limitation of the number of pads (80) on a 10 mm × 10 mm, a 2-channel synchronizer front-end would have to work with a smaller k or at lower f_{clk} until the data link rate is improved. Passive transmission lines [17,18] are used to connect the front-ends to the deserializers.

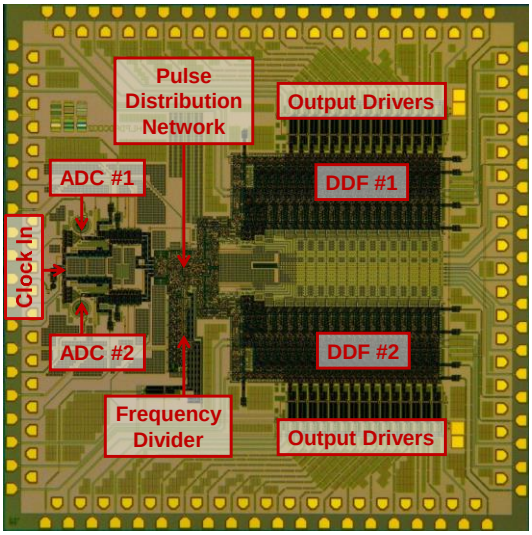


Fig. 2. Photograph of a 10 mm ×10 mm dual-ADC chip, comprising two identical LP-PMD front-ends that are clocked with a common clock derived from an external clock source and two 18-slice digital decimation filters (DDFs). The outputs are 15-bit digital words. This chip has more than 11,000 Josephson junctions.

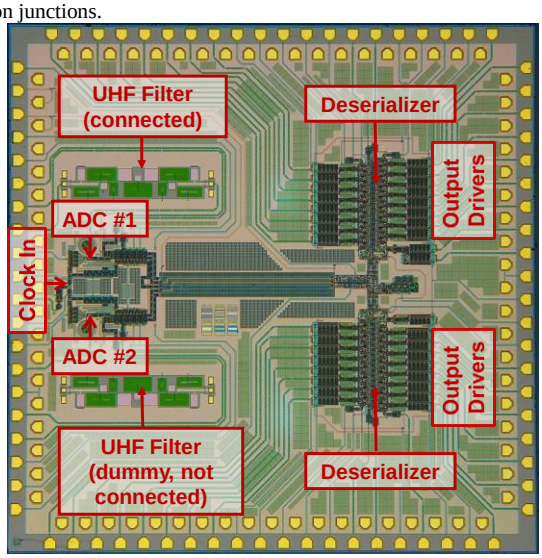


Fig. 3. Photograph of a 10 mm ×10 mm dual-ADC chip, comprising two identical LP-PMD front-ends that are clocked with a common clock derived from an external clock source and two 1:16 deserializers. This variant includes a UHF-band (225-525 MHz) analog filter connected in front of one ADC (#1); the other filter structure is placed to preserve layout symmetry [19].

The quad-ADC with 4 synchronous LP-PMD front-ends with a symmetric clock distribution tree has been designed (Fig. 4). Each front-end is connected to a 1:8 deserializer by passive transmission lines. The tri-ADC design was derived from this quad-ADC by abandoning one front-end and increasing the deserialization ratio of the three outputs from 1:8 to 1:12 enabling higher sampling frequency. A

programmable frequency divider [4] was used to obtain the non-binary division factor of 12. The case for N=3 is an important one for spatial localization and merits discussion. Both tri- and quad-ADCs reach the level of maximum complexity allowed by the selected fabrication process [12] and pad layout for a single chip design.

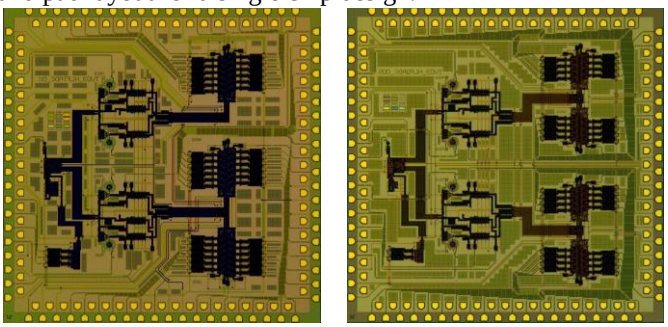


Fig. 4. Photographs of a 10 mm ×10 mm triple-ADC chip (left) and quad-ADC chip (right), comprising three and four identical LP-PMD front-ends and deserializers with 1:12 and 1:8 deserialization ratios correspondingly. Note that one of front-ends seen in triple-ADC chip (left) is not accompanied by deserializer and left on chip to preserve symmetry.

C. Octo-ADC Multi-chip Module (MCM) Design

Scaling to large *N*, especially with substantial on-chip digital circuitry, is best done by dividing the circuit into independently testable modular blocks and assembling as an MCM. Using the dual-ADC chip design (the DDF flavor) as a foundation, an MCM with 8 analog inputs and 8 digital outputs was designed (Fig. 5). The circuit architecture has a central section with 8 ADC front-ends and four identical dual-DDF circuit blocks, preserving common centralized SFQ clocking of all the ADC front-ends. This scalable architecture ensures distribution of multiple RF signals in the synchronized digital domain. In the current implementation, we laid out the central section on the carrier and used 4 identical flipped chips (Fig. 5). Alternatively, one can use a passive carrier and a separate flipped chip for the central section.

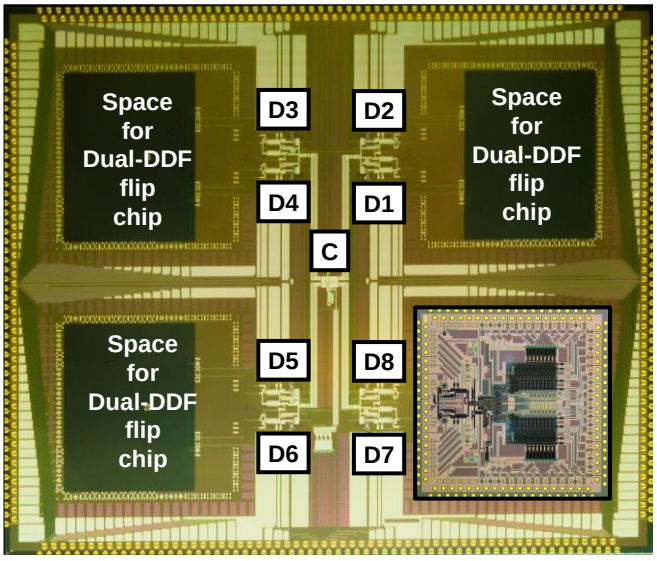


Fig. 5. Layout of a 25 mm ×30 mm octo-ADC carrier. The carrier has 8 LP-PMD ADC front-ends (D1 – D8) and a clock controller (C) and space for four 10 mm ×10 mm dual-ADC flip chips. A dual-ADC flip chip layout is placed face up in the bottom-right quadrant for clarity.

The dual-DDF circuit block was derived from the dual-ADC chip (Fig. 2). In addition to designated inputs for SFQ clock and data arriving from the carrier, these chips have an on-chip front-end section for independent testing and die selection (Fig. 6). Therefore, the dual-DDF flip-chip is essentially a dual-ADC chip with additional interchip connections (Fig. 7). Four SFQ signals are passed from the carrier to a dual-ADC flip chip: a master clock (MC), a decimated or "Nyquist" clock (NC), and two data streams from two LP-PMD front-ends. The carrier is designed so that a selected die can go into any of the four possible locations.

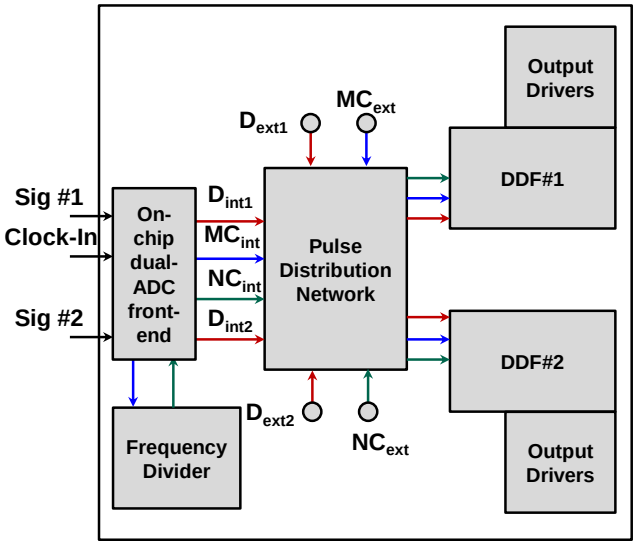


Fig. 6. Block diagram of the dual-ADC flip chip which has two sources of data and clock inputs: external from MCM carrier and internal from an on-chip front-end.

The version of the dual-ADC flip-chip shown in Fig. 7 has a decimation ratio of 32 and a single-channel synchronizer (m=1). There are two sets of pads on this chip. The outer pad-ring corresponds to the standard pad layout for testing in a liquid He immersion probe or a cryocooled testbed. The inner pad-ring corresponds to the matching pads on the MCM carrier. In addition, the chip has a set of MCM interface pads inside the chip for passing SFQ signals from the carrier.

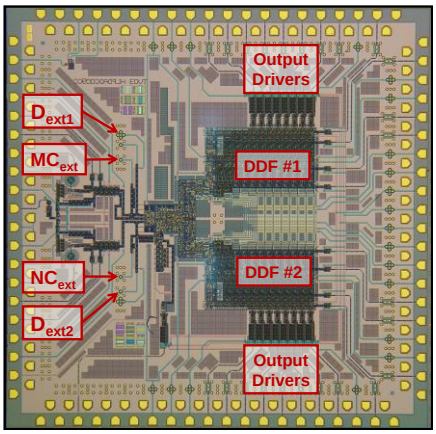


Fig. 7. Photograph of a 10 mm ×10 mm dual-DDF chip, designed to be flipped on the carrier shown in Fig. 4. The chip includes two LP-PMD front-ends for independent testing of the DDFs at high clock frequency.

The interchip interface consists of matching pad structures on the carrier and the flip-chips and driver-receiver pairs to send SFQ pulses from the carrier to the flipped chips [17],[18].

III. Operation of Dual-ADC Chip in a Cryocooled Digital-RF Receiver Testbed

Modular digital-RF receiver systems provide a convenient platform for operating various superconductor chips and MCMs. One of the third-generation [20] digital-RF receivers (ADRs) was used to host a dual-ADC chip module. Such a rack-mounted ADR system is capable of hosting two chip modules. The configuration shown in Fig. 8 corresponds to a single chip module mounted in an ADR.

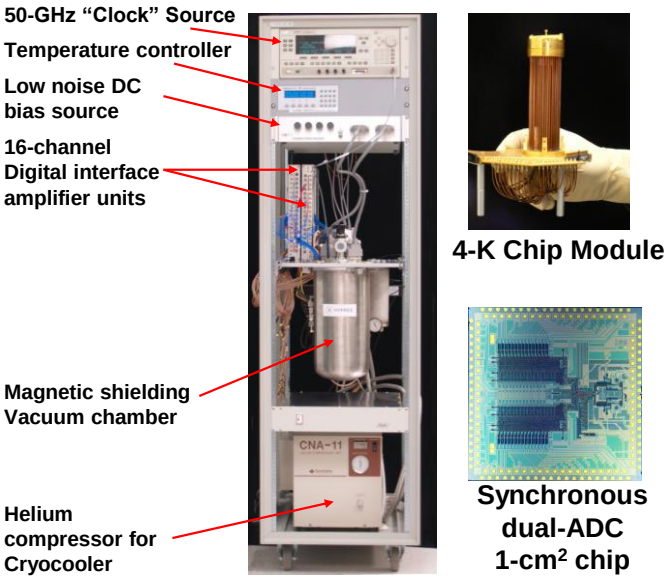


Fig. 8. The dual-ADC chip shown in Fig. 2 was mounted in a cryocooled digital-RF receiver testbed, equipped with an external clock source, interface amplifiers, FPGA-based data acquisition and other monitoring devices. Photographs of the chip and its module are also shown.

A. Performance of Dual-ADC chip in ADR

The chip performed consistently over many measurements at HYPRES and SSC-Pacific laboratories. To illustrate representative performances of the two ADCs and channel isolation, we describe a measurement where two closely spaced signals around 10 MHz were applied to the two ADCs through a pair of bandpass filters (BPFs) and attenuators (Fig. 9 and Fig. 10). The least significant output bit of the second DDF was defective and lowered the performance of the second ADC by 2-3 dB compared to the first.

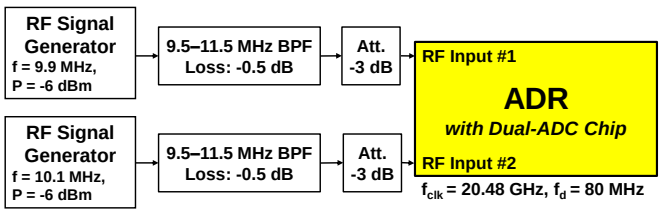
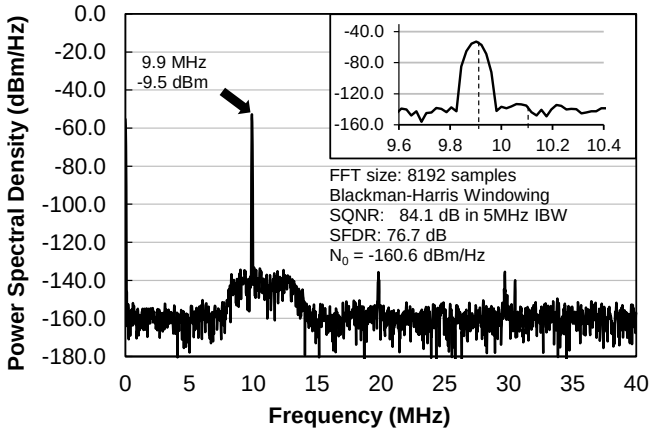


Fig. 9. A test set-up at SSC-Pacific laboratory for channel isolation measurement of the dual-ADC chip shown in Fig. 2 in the ADR digital-RF receiver testbed. The digitized outputs were acquired through a Virtex-4 FPGA after passing through a pair of interface amplifier units.



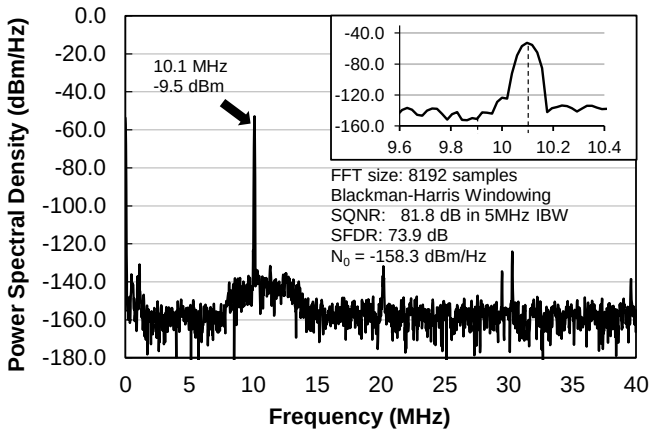


Fig. 10. Digitized spectra for the two ADCs on the same chip, obtained by applying two sinusoidal signals at 9.9 and 10.1 MHz to them respectively, from a pair of Agilent 8257D RF signal generators, are shown. The common master clock frequency was 20.48 GHz. The first ADC (top spectrum) has better performance than the second (bottom spectrum). The noise pedestal around the peak signal represents the generator's noise upon bandpass filtering. The insets zoom in on the 9.6-10.4 MHz range to illustrate the fact that no measurable inter-channel interference was observed.

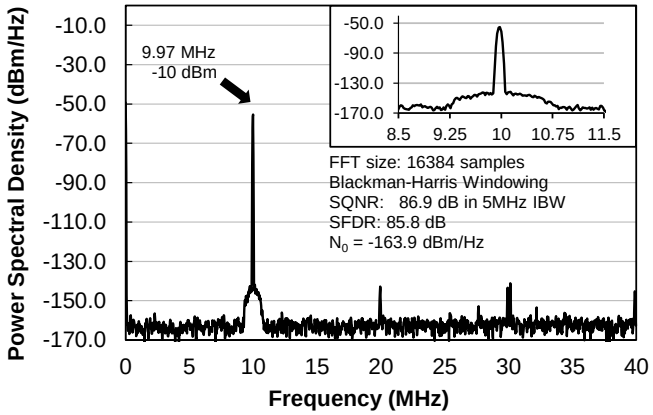


Fig. 11. Digitized spectrum obtained from the first ADC, clocked at 20.48 GHz, for a single-tone analog input with -10 dBm input power at 9.973 MHz, which is close to the slew-rate limit. The average signal-to-quantization-noise-ratio for a set of 10 consecutive acquisitions was about 87 dB for a 5 MHz noise bandwidth.

B. Time delay measurement with Dual-ADC chip

A simple experiment (Fig. 12) was performed with the dual-

ADC chip to illustrate the principle of time delay measurement with a set of synchronous ADCs. A sinusoidal signal (f_s) from a single generator was split and applied to the two ADC inputs on a dual-ADC chip through varying cable lengths. For this experiment, we chose a set of 6-ft coaxial cables and a set of 1-inch connectors. After capturing the digitized data at the output (decimated) clock rate through a logic analyzer, a sine-fit analysis was performed (Fig. 13) to measure the phase difference ($\Delta\phi$) between the two channels. For this experiment, f_{clk} = 15.36 GHz, f_d = 60 MHz, and f_s = 5 MHz.

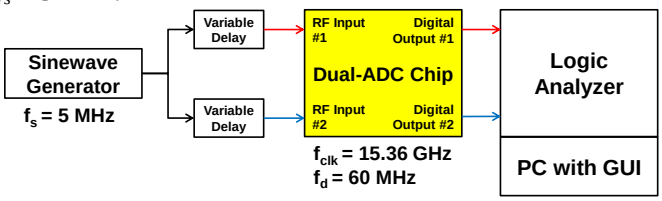


Fig. 12. A test set-up to measure time delay using the dual-ADC chip.

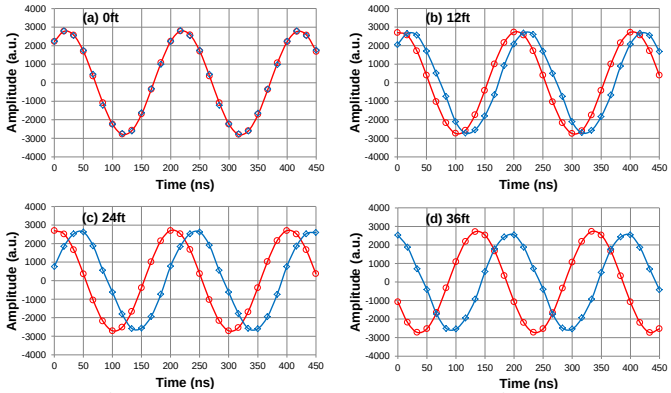


Fig. 13. A few representative reconstructed sinewaves from the two ADC outputs are shown for various cable length differences.

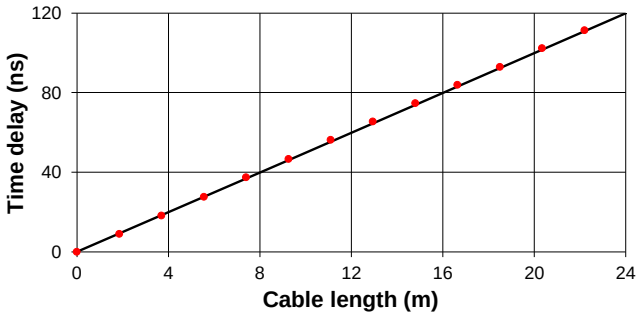


Fig. 14. Time delays measured by the dual-ADC chip shown in 2 are plotted against a theoretical linear function.

No inter-channel delay was observed with equal lengths of cable. Next, the delay of the first ADC was fixed and thirteen coaxial cables were added one by one before the second ADC input. The time delay was calculated as $\tau = \Delta\phi/(2\pi f_s)$ and plotted as a function of cable length difference between two inputs (Fig.14). The measured time delays matched well with theory. To explain experimental data we have taken into account the length of each connector. That gives us a rough estimation of spatial resolution to be about 1 inch.

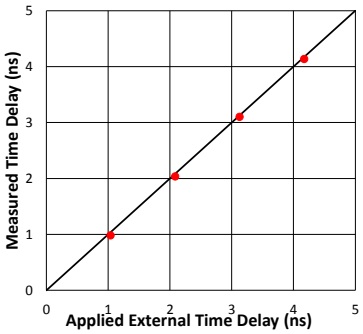


Fig. 15. Time delays measured by the dual-ADC chip shown in Fig. 3 are plotted against independently measured delays.

In the next experiment, we used the dual ADC chip with deserializers (Fig. 3). First, we measured the difference in the delay between the two inputs to the ADCs introduced primarily by the analog UHF filter, which was estimated to be about 640 ps and compensated by adding an extra cable. As in the previous experiment, the external delay was applied by connecting a set of cables. These cable delays were characterized using a time-domain reflectometer (TDR) and plotted as the x-coordinate (Fig. 15). The time delays measured by the dual-ADC match the TDR predicted values.

IV. Conclusion

We have designed and demonstrated synchronous operation of two lowpass ADCs, not only at the chip level but through the complete data acquisition system comprising interface amplifiers. This proves that coherence can be maintained for the entire system and paves the way for scaling the system to multi-input ADCs. Current data link and fabrication technology limitations permit up to four such ADCs to be integrated on a single 10mm x 10mm chip. Further scaling requires a multi-chip module approach with interchip transport of SFQ clock and data. The dual-input ADC chip has been operating reliably as part of an ADR for three years. Cryocooled digital-RF receiver systems provide a convenient, stable platform for using superconductor ADCs at MRI facilities.

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