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Demonstration of 10k gate-scale adiabatic-quantum-flux-parametron circuits

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***Abstract*— Adiabatic quantum flux parametron (AQFP) is a very energy-efficient superconductor logic. In AQFP logic, dynamic energy dissipation can be drastically reduced due to adiabatic switching operations using ac excitation currents. In the present study, we evaluated circuit yields using a large-scale AQFP circuit composed of as many as 10,000 AQFP gates with approximately 20,000 Josephson junctions. We measured eleven chips from four wafers and obtained circuit yields of 48% for 1,000-gate circuits and 22% for 10,000-gate circuits, respectively. In all the circuits, which worked correctly, the margins of excitation currents were as wide as approximately ±20%.**

Keywords—AQFP, flux biasing, adiabatic operation, circuit yield

I. Introduction

Complementary metal–oxide–semiconductor (CMOS) logic has been widely used in most digital circuits over last two decades because of the continuing improvement in energy efficiency, which was accomplished by huge effort in miniaturization of device size. However, the improvement in energy efficiency is getting more and more difficult, for example, due to static power consumption caused by a large amount of leakage currents. Therefore, rapid-single-flux-quantum (RSFQ) logic [1] has been attracting much attention thanks to high operation frequencies and low energy dissipation compared to CMOS logic. In order to achieve even lower energy dissipation per operation, energy-efficient superconductor logics, including reciprocal quantum logic (RQL) [2], energy efficient SFQ (eSFQ) logic [3], low voltage RSFQ (LV-RSFQ) logic [4], are being studied. In those logics, static power consumption is much smaller than that of RSFQ logic, because the resistances in bias networks are removed or reduced.

Adiabatic quantum flux parametron (AQFP) logic [5,6] is one of the energy-efficient superconductor logics. In AQFP logic, static energy dissipation is zero because of the flux biasing using ac excitation currents, and dynamic energy dissipation in switching events can be reduced by adiabatically changing potential energy. Moreover, the bit energy of an AQFP gate with underdamped Josephson junctions can be reduced below the Landauer bound [7] given by $k_B T \ln 2$ [8], where k_B is the Boltzmann constant, and T is temperature. We demonstrated reversible computing using logically and physically reversible AQFP gates with underdamped Josephson junctions [9,10], where the energy dissipation per logic operation can be below the Landauer bound.

Recently, we built an AQFP cell library [11,12] and successfully demonstrated an 8-bit carry look-ahead adder (CLA) [12]. The CLA includes 1,152 junctions and the largest AQFP circuit ever demonstrated. In the present study, we demonstrate a much larger AQFP circuit composed of as many as 10,000 AQFP gates with approximately 20,000 junctions, so as to evaluate circuit yields in AQFP logic. Through the measurement of eleven chips, we obtain the circuit yields for 1,000-gate circuits and 10,000-gate circuits, respectively.

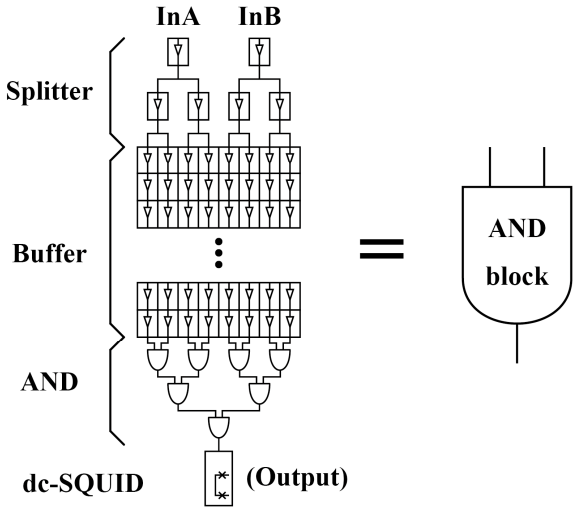

Fig. 1. Schematic of an AND block with 1,000 gates.

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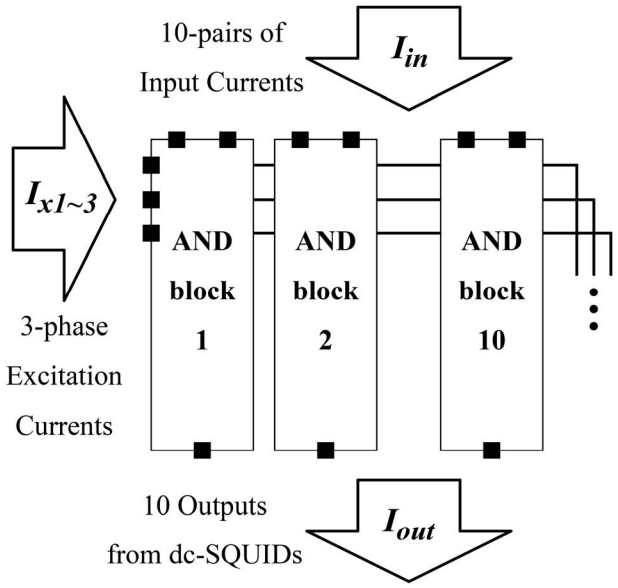

Fig. 2. Schematic of 10,000-gate circuits with 20,000 junctions.

II. Design of 10,000-Gate Circuits

The 10,000-gate circuit is composed of ten AND blocks, where an AND block includes 1,000 AQFP gates with approximately 2,000 junctions. Fig. 1 shows the schematic of the AND block. The two inputs (InA and InB) are divided to 8-bit data using splitter (SPL) gates, and the 8-bit data go through eight AQFP buffer trains, where one train includes 86 AQFP buffer gates in series. Finally, the data are merged by seven AND gates and the output is observed using a dc superconducting quantum interference device (SQUID). Only when all the gates in the block operate correctly, the correct output is obtained as the logical AND of InA and InB. Fig. 2 shows the schematic of the 10,000-gate circuit composed of 10 AND blocks, in which approximately 20,000 junctions are included in total. Since each output from an AND block can be observed individually, we can obtain circuit yields for both 1,000-gate circuits and 10,000-gate circuits. It should be noted that the 10 AND blocks are serially excited using the same excitation lines. Therefore, the 10,000-gate circuit can operate with three-phase excitation currents of only 4.8 mA in total.

III. Measurement of 10,000-Gate Circuits

Figure 3 shows the microphotograph of the 10,000-gate circuits fabricated using the AIST 2.5 kA/cm2 Nb standard process 2 (STP2) [13]. We measured eleven chips from four wafers, where one chip includes one 10,000-gate circuit. The measurement was implemented using three-phase trapezoidal excitation currents at 100-kHz in the liquid He. Figure 4 shows an example of measurement waveforms, where I_{x1} through I_{x3} are excitation currents, I_{sq} is a bias current for dc-SQUIDs, I_{inA} and I_{inB} are input currents, and V_{out} is the output voltage. In the example, "110011000100" and "101010100100" are input to InA and InB, respectively, and the correct output of "100010000100" is obtained after 31 excitation cycles after the inputs are applied. Table 1 shows the obtained circuit yields for

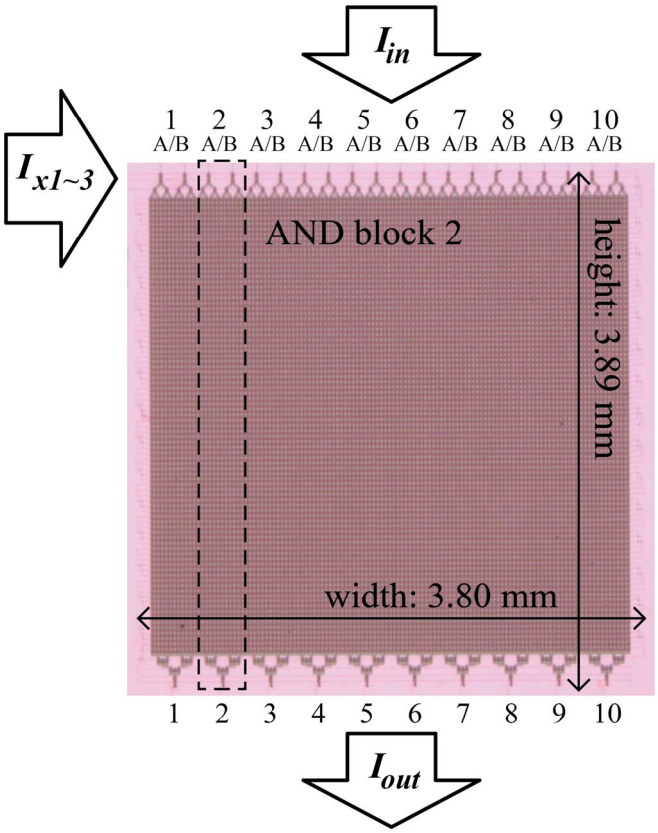

Fig. 3. Microphotograph of the 10,000-gate circuit

both 1,000-gate circuits (AND blocks) and 10,000-gate circuits. Apparently, the circuit yields in the wafer #1 is lower than the other wafers, which could be because of fabrication problems. In total, the yields of 1,000-gate circuits was 48% and that of 10,000-gate circuits was 22%. We also confirmed that in all circuits, which worked correctly, had excitation margins of approximately ±20%.

IV. Conclusion

We designed 10,000-gate AQFP circuits to evaluate circuit yields. The 10,000-gate circuit is composed of ten 1,000-gate circuits (AND blocks). We measured eleven chips from four wafers, and the obtained yields were 48% for 1,000-gate circuits and 22% for 10,000-gate circuits.

Acknowledgment

The circuits were fabricated in the Clean Room for Analog-digital superconductiVITY (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with standard process 2 (STP2).

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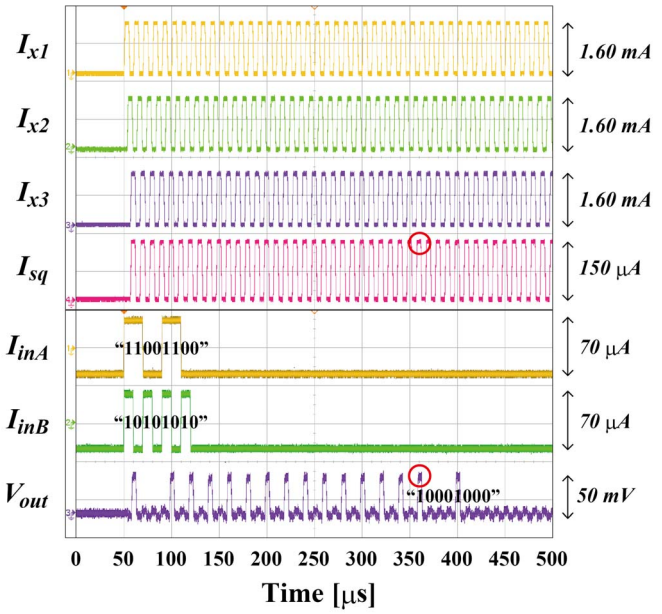

Fig. 4. Observed waveform of the 10,000-gate circuit.

TABLE I. MEASUREMENT RESULTS

Wafer	# of chips	Yields of 1,000-gate circuits	Yields of 10,000-gate circuits
#1	3	3% (1/30)	0% (0/3)
#2	3	53% (16/30)	33% (1/3)
#3	3	63% (19/30)	0% (0/3)
#4	2	85% (17/20)	50% (1/2)
Total	11	48% (53/110)	22% (2/11)

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