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(Version without animation)

12th European Conference on Applied Superconductivity,
EUCAS 2015 6 - 10 September 2015, Lyon, France

Advanced Fabrication Processes for Superconducting Very Large Scale Integrated Circuits

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This work was sponsored by the IARPA under Air Force Contract FA872105C0002.

Opinions, interpretations, conclusions, and recommendations are those of the author, and not necessarily endorsed by the United States Government.

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- **Introduction**
  - **MIT-LL Fab description**
  - **SFQ fabrication process nodes and the roadmap**
- **SFQ4ee process characterization and highlights**
  - **Photolithography and junctions**
  - **Circuit inductors**
  - **Process benchmarking circuits: AC-biased shift registers**
- **SFQ5ee process highlights: linewidth reduction to 0.35 μm**
  - **High sheet resistance layer**
  - **Second resistive layer: sandwich-type interlayer resistors**
  - **High-kinetic inductance layer (9th superconducting layer)**
- **Conclusion**

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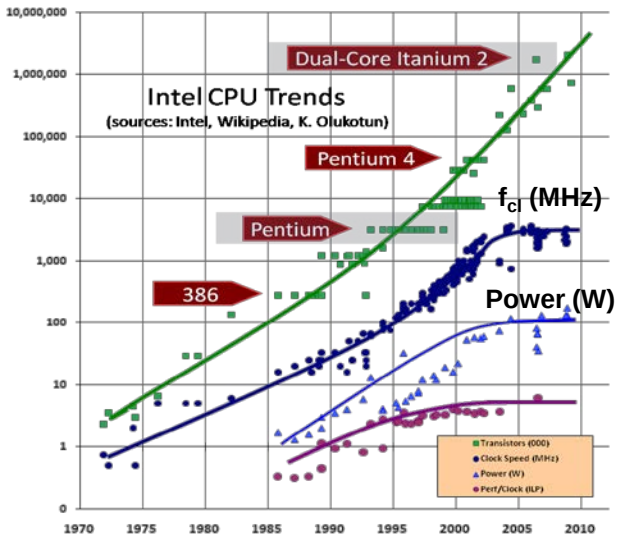
Introduction

- 55 years since the invention of semiconductor integrated circuits
- 30 years since RSFQ logic proposal for superconducting circuits

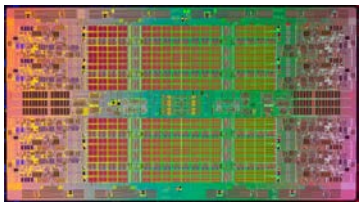


- Exponential growth of CMOS circuits (Moore's law) to ~ 50B transistors per chip (VLSI and ULSI)
- Medium-to-Large scale SFQ circuits, <~ 10^5 JJs
- Moore's law is not a law of physics – rather a reflection of capital growth in a market-driven economy
- There has been no market for superconducting circuits
- Government-funded programs are a substitute for the market
- Old rules of the game: Circuit speed (SFQ beats CMOS)

Nothing can grow exponentially forever

P ~ 0.1 W/cm^2

P ~ 10 W/cm^2



P ~ 100 W/cm^2

- New rules of the game: Energy efficiency instead of clock speed
- RSFQ was eliminated from the competition by this new market trend
- New SFQ branches have emerged: RQL, ERSFQ, eSFQ, adiabatic QFP, reversible…

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IARPA Cryogenic Computing Complexity (C3) Program

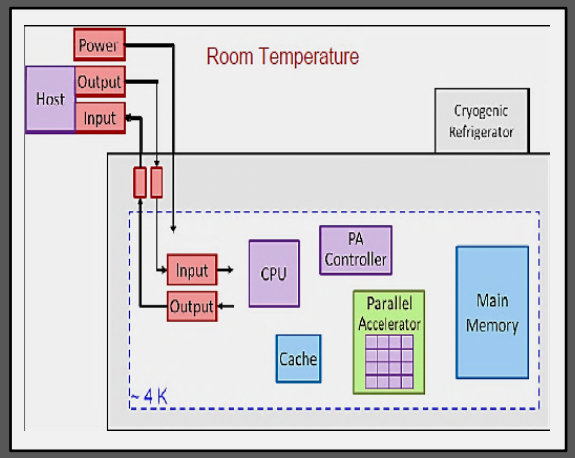
IARPA
BE THE FUTURE

Cryogenic Complexity (C3) Program

Office of Safe and Secure Operations

- **MIT Lincoln Laboratory (MIT-LL) was selected to serve as a Government Furnished Foundry for superconductor electronics for IARPA C3 Program**
- **MIT-LL is developing and maintaining several fabrication processes for SFQ-based superconducting circuits**
- **Circuits are designed by selected teams (IBM, NG, etc.) and fabricated at MIT-LL**

Superconducting computer to be developed by Y5 of the program



Notional Superconducting Computer System Diagram

Metric	Goal
Clock rate for superconducting logic	10 GHz
Throughput (bit-op/s)	10^{13}
Efficiency @ 4 K (bit-op/J)	10^{15}
CPU count	1
Word size (bit)	64
Parallel Accelerator count	2
Main Memory (B)	2^{28}
Input/Output (bit/s)	10^{9}

Superconducting Computer Metrics and Goals

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MIT-LL Microelectronics Laboratory

- **Classification**
  - **Total: 6400 m^2 (Class-10: 740 m^2; Class-100: 910 m^2)**
- **Production-class 90-nm CMOS, 200-mm tool set**
  - **Cluster metallization (sputter, MBE, CVD), etch, CMP, …**
  - **Advanced lithography: i-line, 248-nm, 193-nm, e-beam**
  - **Full SPC, electronic traveler, area engineers, technicians**
  - **Three-shift operation (24x5) from 01/2015**
  - **~10,000 wafer starts per year**
- **Superconductor electronics (SFQ) fabrication**
  - **200-mm tool set**
  - **Deep submicron junctions and wiring features**
  - **Dedicated metal and dielectric deposition tools**
  - **Dedicated metal and dielectric etch tools**
  - **Dedicated CMP tool**
  - **248-nm and 193-nm photolithography tools (shared)**
  - **Metrology and defect inspection tools (shared)**
  - **Superconducting multichip module fabrication**

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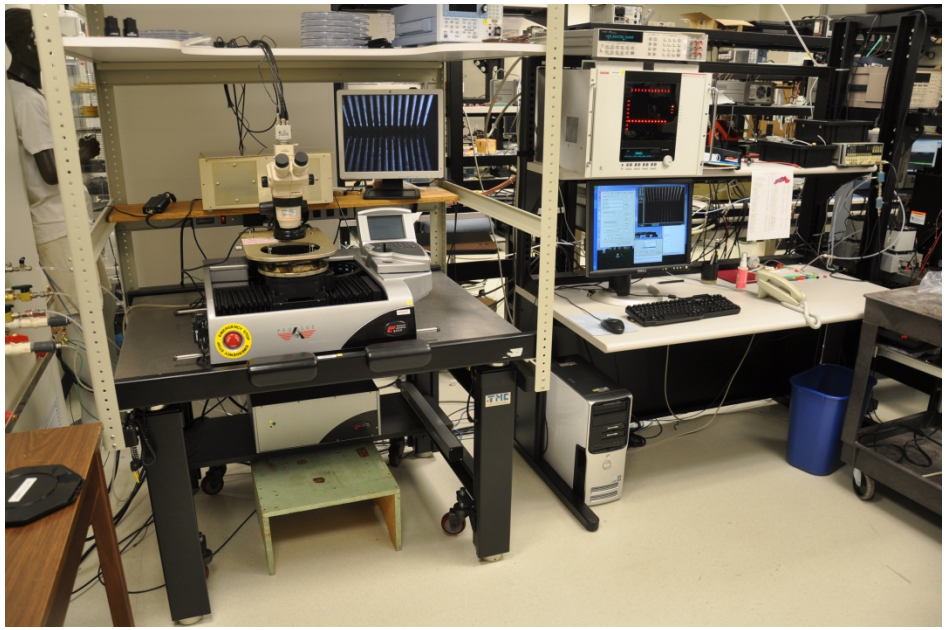
Room Temperature and 4K Process-Yield Testing

- **Room-temperature testing**
  - Three semi-automatic wafer probers
  - Switch matrix and test equipment
  - Automation software
  - 3,000 test structures per PCM
  - 9 PCM chips per wafer
- **Cryogenic testing**
  - 14-chip He immersion probes
  - 5-mm die attached to PCB and wired with automatic wirebonder
  - Switch matrix and test equipment
  - Automation software
  - Dilution refrigerator with 40-cm samples space for mK testing
- **CryoCMOS-enabled cryogenic switching**

Room Temperature Automatic Prober



^{4}He 14-chip Immersion Probe

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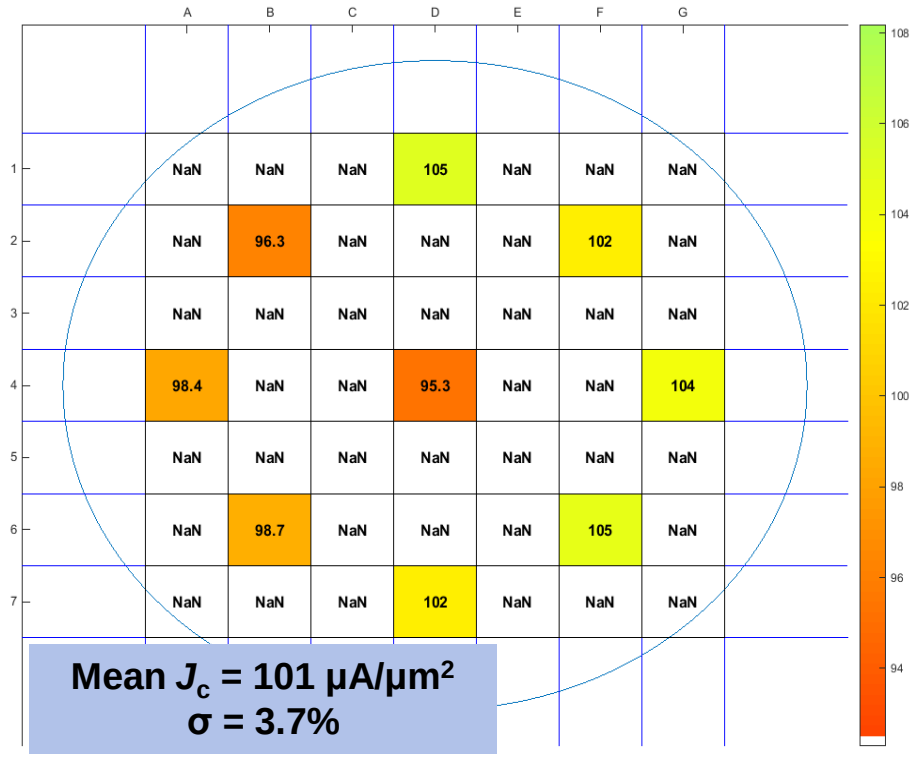
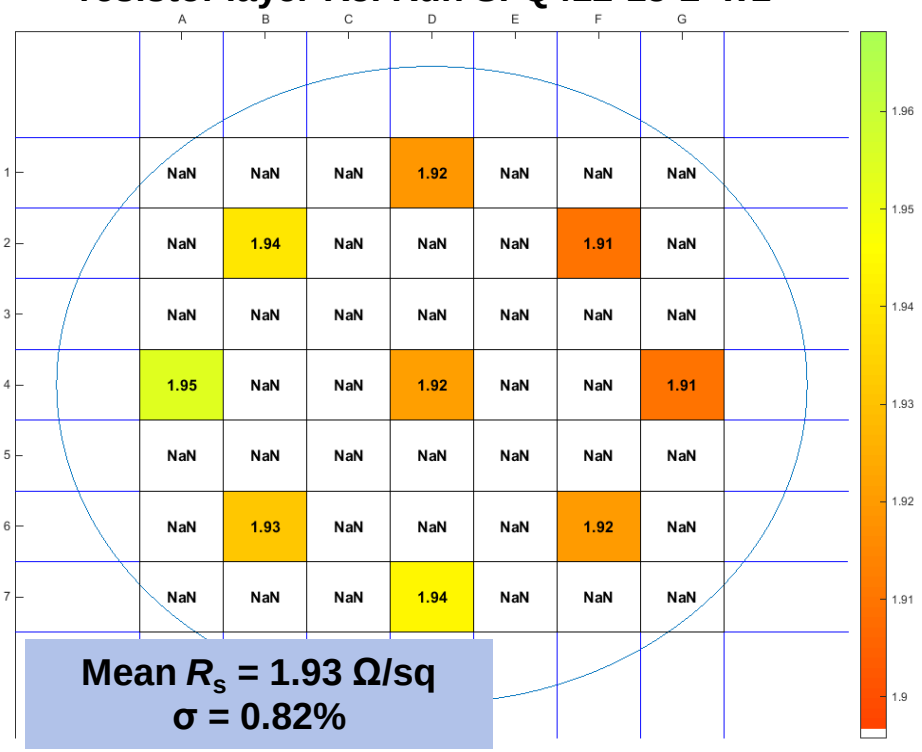
Wafermaps from 4.2 K and 300 K Measurements

Wafermap of J_c (μA/μm²)
Run SFO412-15-2 w1



Mean J_c = 101 μA/μm²
σ = 3.7%

Wafermap of the sheet resistance of resistor layer R5. Run SFQ412-15-2 w1



Mean R_s = 1.93 Ω/sq
σ = 0.82%

- 22 mm x 22 mm reticle size (exposure field)
- 45 full exposure fields per wafer
- 9 Process Control Monitor (PCM) sites per wafer

- 16 PCM chips (5 mm x 5 mm) per location
- 3,000 test structures on 16 chips
- 540 "customer" chips per wafer
- 8 wafers per lot (fab run)

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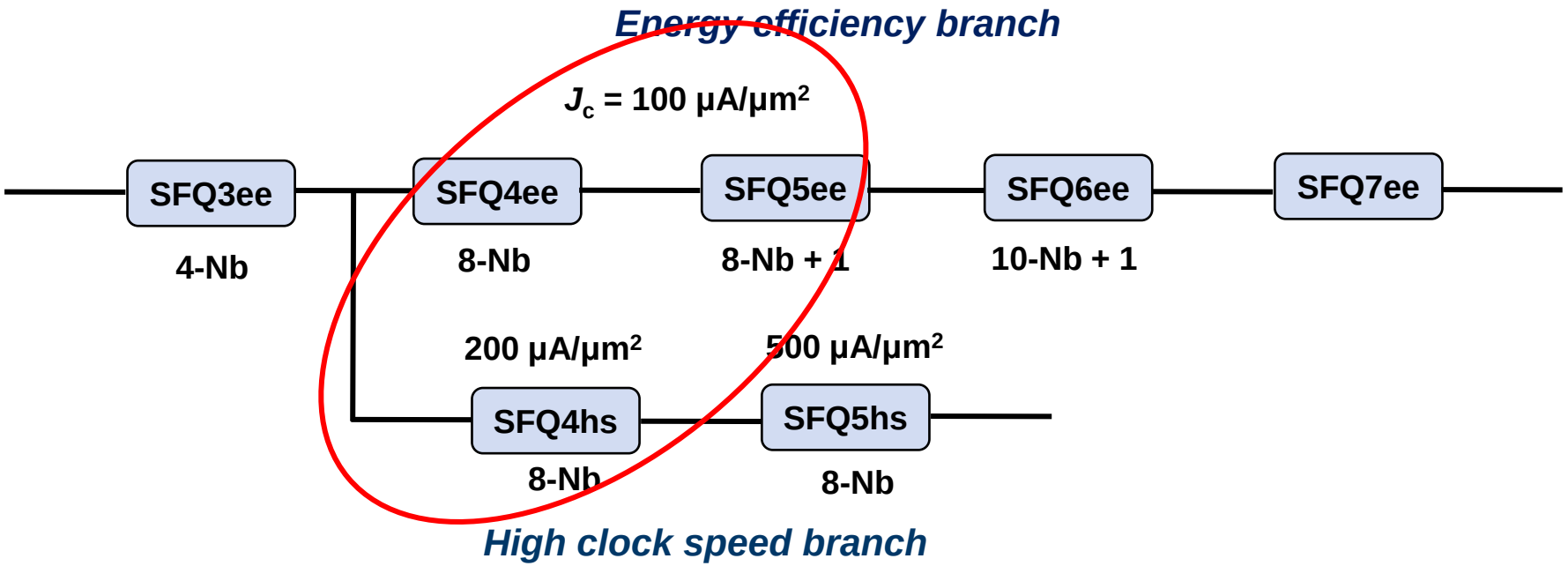
MIT-LL SFQ Process Nodes



- "ee" denotes that the process is tuned for energy efficient circuits
- "hs" denotes the processes for high-speed circuits
- "8-Nb" denotes process nodes with 8 niobium superconducting layers
- "8-Nb + 1" denotes nodes with 9 superconducting layers: 8 Nb + 1 High Kinetic Inductance Layer (HKIL)

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MIT-LL SFQ Technology Roadmap

Fabrication Process Attribute		Units	✓ ✓ Process Node					
			SFQ3ee	SFQ4ee	SFQ5ee	SFQ6ee	SFQ7ee	SFQ8ee
Junction critical current density		$\mu A/\mu m^2$	100	100	100	100	100	100
JJ diameter (surround)		nm	700 (500)	700 (500)	700 (300)	700 (300)	500 (200)	500 (200)
Nb metal layers		-	4	8	8	10	10	10
Line width (space)	Critical layers	nm	500 (1000)	500 (700)	350 (500)	350 (500)	250 (300)	180 (220)
	Other layers	nm			500 (700)	500 (700)	350 (500)	250 (300)
Metal thickness		nm	200	200	200	200	200	150
Dielectric thickness		nm	200	200	200	200	200	180
Resistor width (space)		nm	1000 (2000)	500 (700)	500 (700)	500 (700)	500 (500)	350 (350)
Shunt resistor value		Ω/sq	2	2	2 or 6	2 or 6	2 or 6	2 or 6
mΩ resistor		mΩ	-	-	3 - 10	3 - 10	3 - 10	3 - 10
High kinetic inductance layer		pH/sq	-	-	8	8	8	8
Via diameter (surround)		nm	700 (500)	700 (350)	500 (350)	500 (350)	350 (250)	350 (200)
Via type, stacking		-	Etched, Staggered	Etched, Stacked \2/	Etched, Stacked \2/	Etched, Stacked \2/	Stud, Stacked	Stud, Stacked
Access availability		-	2013-01	2014-01	2015-09	2016-03	2016-09	2017-09

Color change indicates changes from the previous process node

Future ⇨

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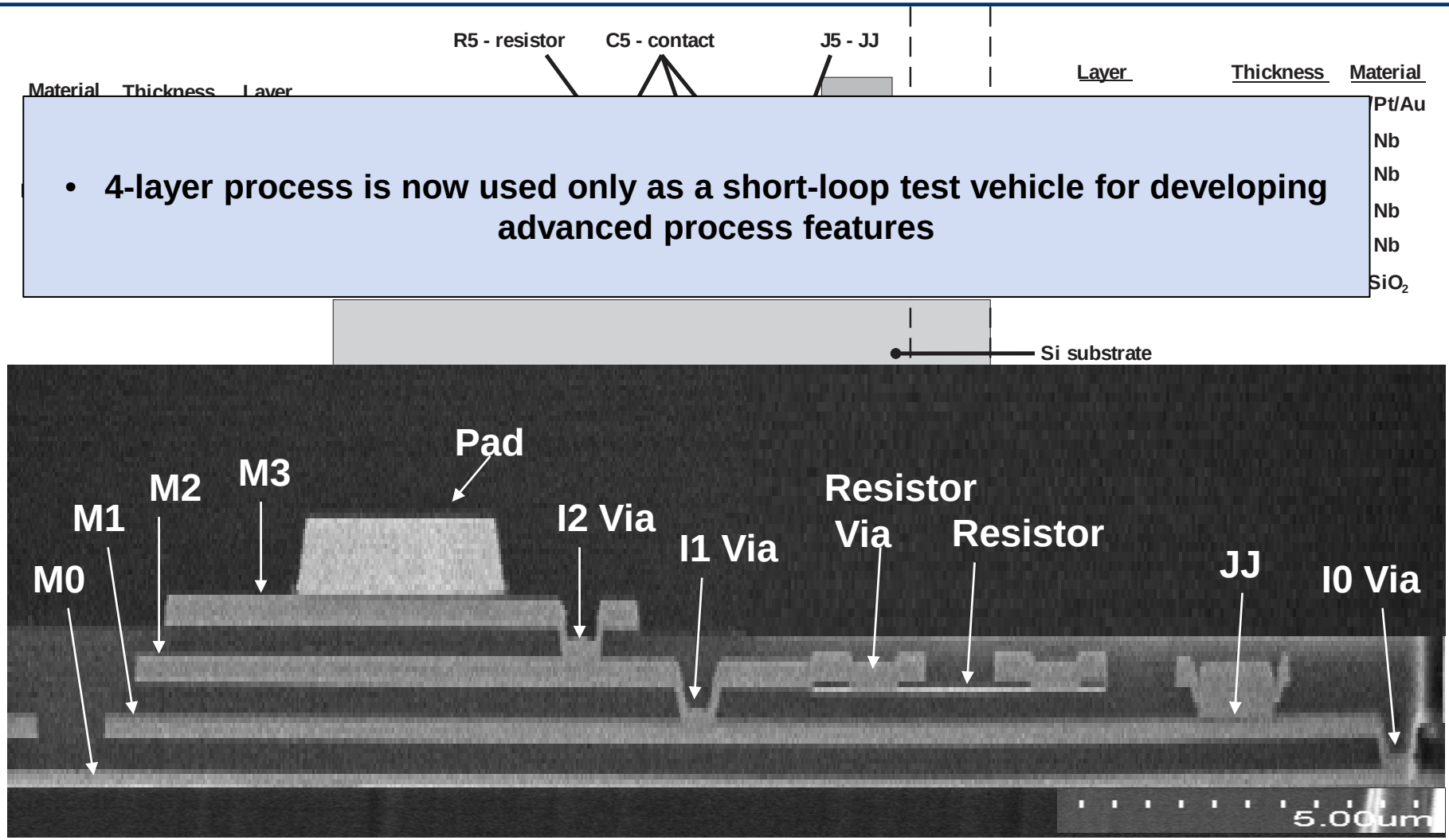
4-Layer Process Node: SFQ3ee
Cross Section



- 4-layer process is now used only as a short-loop test vehicle for developing advanced process features

- 4 Nb layers
- 700 nm Josephson junctions
- Wiring: 500 nm width, 700 nm spacing

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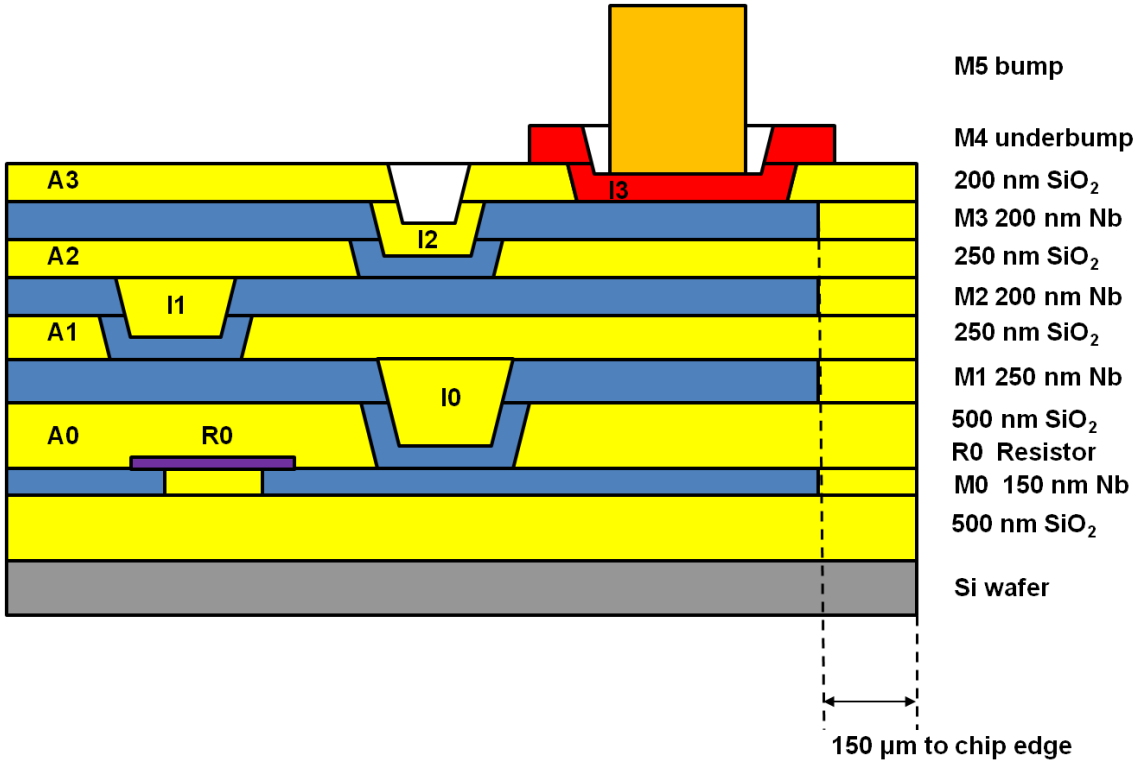
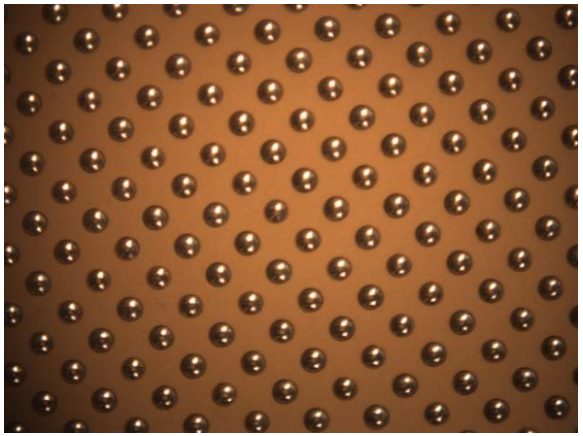
Process for 4-Metal-Layer Superconducting MCM





Reflowed indium bumps (optical Image)
15 µm bump diameter on 35 µm pitch

- **Dielectric thicknesses chosen to facilitate impedance targets:**
  - **50 Ω for 'clock' lines**
  - **15 – 20 Ω for 'data' lines**
- **Indium bumps: 8-15 µm diameter on 35 µm pitch**
- **Up to $6 \cdot 10^4$ bumps per chip in flip-chip MCMs demonstrated**
- **32 mm x 32 mm MCM size (up to 5 cm by 5 cm possible), i-line photolithography**

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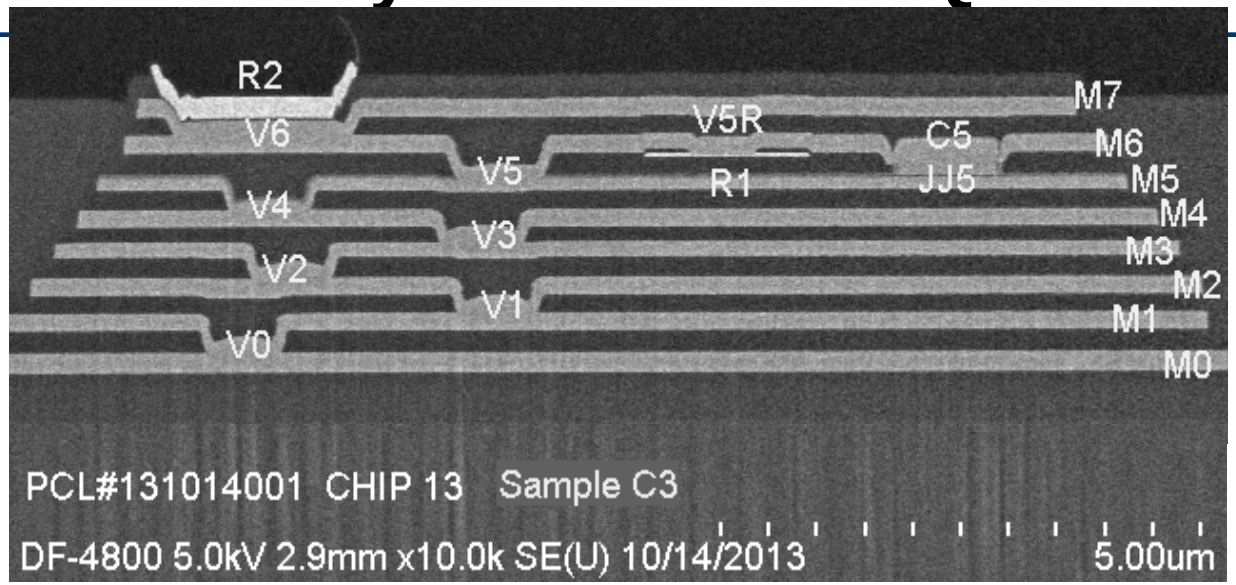
MIT-LL Fully Planarized SFQ4ee Process



Process Features

- Wafer size: 200 mm
- JJ technology: Nb/Al-AlO_x/Nb
- J_c: 10 kA/cm^2 (100 μA/μm^2) baseline
- Number of Nb layers: 8
- Min JJ size: 700 nm
- Min wiring size: 350 nm
- Min spacing: 500 nm
- Full planarization of all layers by CMP
- Fab cycle time: 2.5 months, 8 wafers

- Mask releases 2014: 3
- Mask releases 2015: 4 + 4 more planned

- Integration scale demonstrated:
  - RQL shift registers with 72,300+ JJs per chip (with Northrop Grumman)
  - AC-biased SFQ shift registers with 65,000+ JJs per circuit (with V. Semenov, SBU)
  - AC-biased SFQ shift registers with 144,000+ JJs per circuit fabricated and under test

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Wiring Processing Module

Processing step

1. Deposition (sputtering) of Nb layer M0
2. Photolithography
3. Metal dry etching
4. ILD SiO_2 deposition and CMP
5. ILD Photolithography
6. Contact hole (Dielectric) etch
7. Deposition of Nb layer M1

- AMAT etch cluster

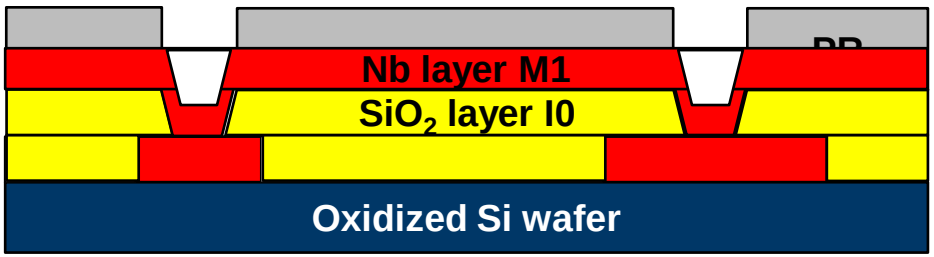
- Novellus, PECVD of SiO_2
- AMAT CMP tool

- Mattson
- Wet

- AMAT etch cluster

- TEL-ACT12
- Canon FPA-3000 EX4

- AMAT PVD cluster



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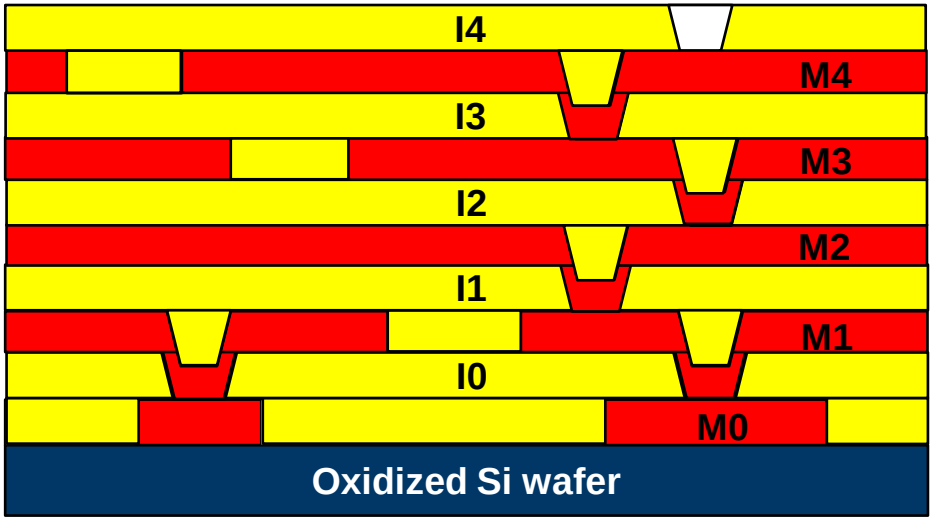
Building Bottom Wiring Layers

Now we are ready to proceed to creating active devices - Josephson junctions



Processing step

1. Deposition (sputtering) of Nb layer M0
2. Photolithography
3. Metal dry etching
4. ILD SiO_2 deposition and CMP
5. ILD Photolithography
6. Contact hole (Dielectric) etch
7. Deposition of Nb layer M1
8. Patterning of layer M1
9. SiO_2 deposition and CMP, layer I1
10. Patterning layer I1
11. Deposition and pattering of Nb layer M2
12. Deposition and planarization of layer I2
13. Patterning layer I2
14. Deposition and patterning of Nb layer M3
15. Deposition, planarization, and pattering of SiO_2 layer I3
16. Deposition and pattering of Nb layer M4
17. Deposition, planarization, and pattering of SiO_2 layer I4

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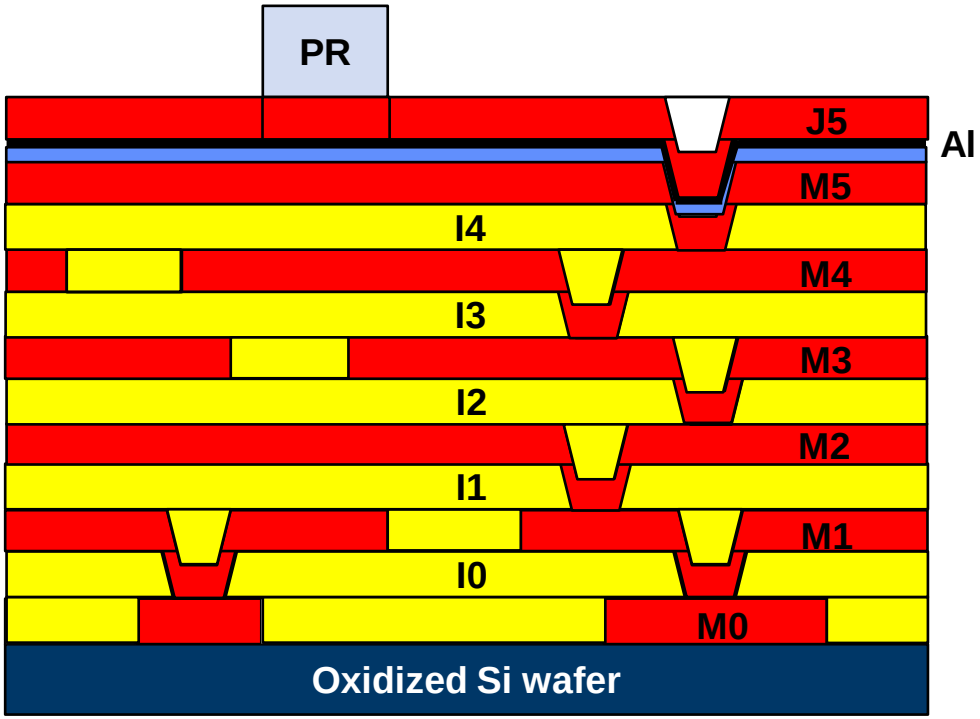
"Front-end Processing:" Josephson Junctions

Josephson junctions have been defined;
Base electrode, layer M5, serves as bottom wire



Processing step

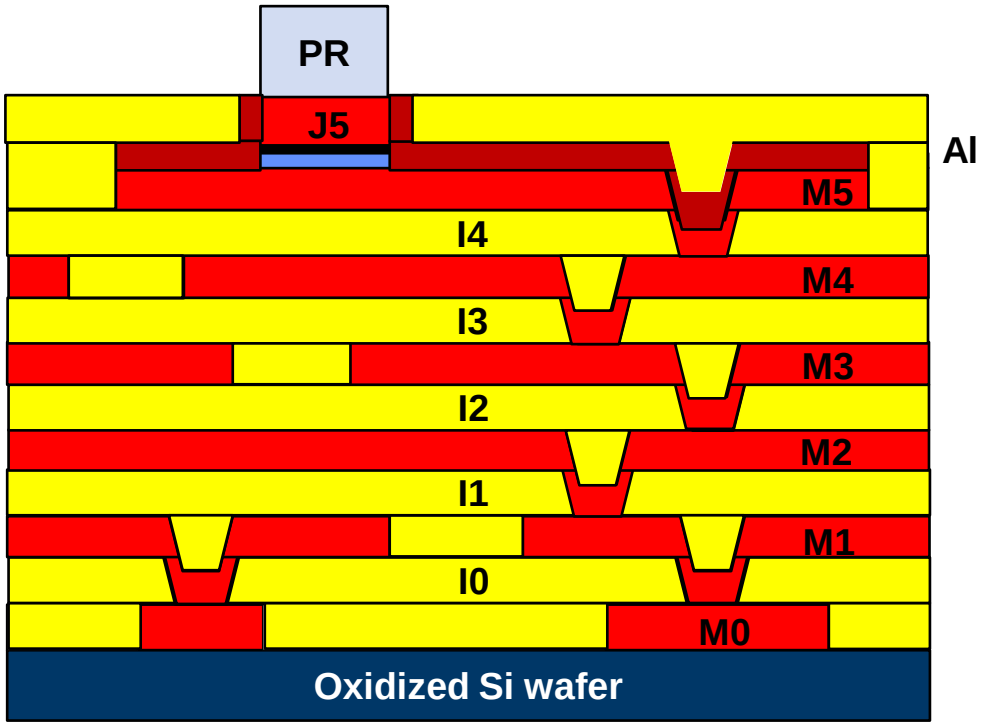
18. Deposition of JJ base electrode, Nb layer M5
19. *In-situ* deposition of Al barrier layer
20. *In-situ* thermal oxidation of Al to form ~ 1-nm layer of AlOx
21. *In-situ* deposition of Nb counter electrode. JJ trilayer Nb/Al-AlOx/Nb is formed
22. JJ photolithography
23. Etching counter electrode of JJs. This defines JJ area.

Processing step

25. **Passivation using anodic oxidation**

26. **Patterning JJ's base electrode, M5**

27. **SiO_2 deposition and CMP to the JJ level**



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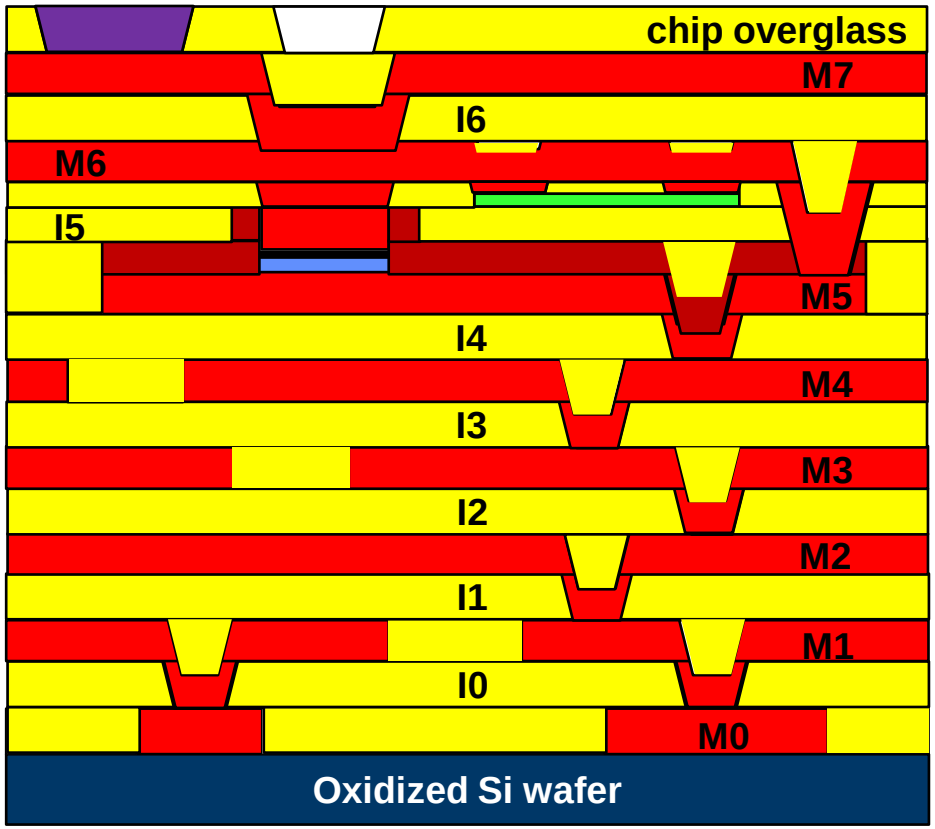
"Back-end Processing:" Resistive Shunt and Top Wiring Layers

And after ~ 430 opsets and ~ 2.5 months of work, our wafer processing is done



Processing step

28. Deposition and pattering of molybdenum resistor layer, R5
29. SiO_2 dielectric deposition
30. Etching contacts to resistors and JJs
31. Deposition and pattering of top Nb wiring layer M6
32. Deposition, planarization, and pattering SiO_2 layer I6
33. Deposition and pattering of Nb sky plane, layer M7
34. Deposition, and pattering of chip passivation SiO_2 layer
35. Deposition and pattering of chips contact pads (Ti/Pt/Au)

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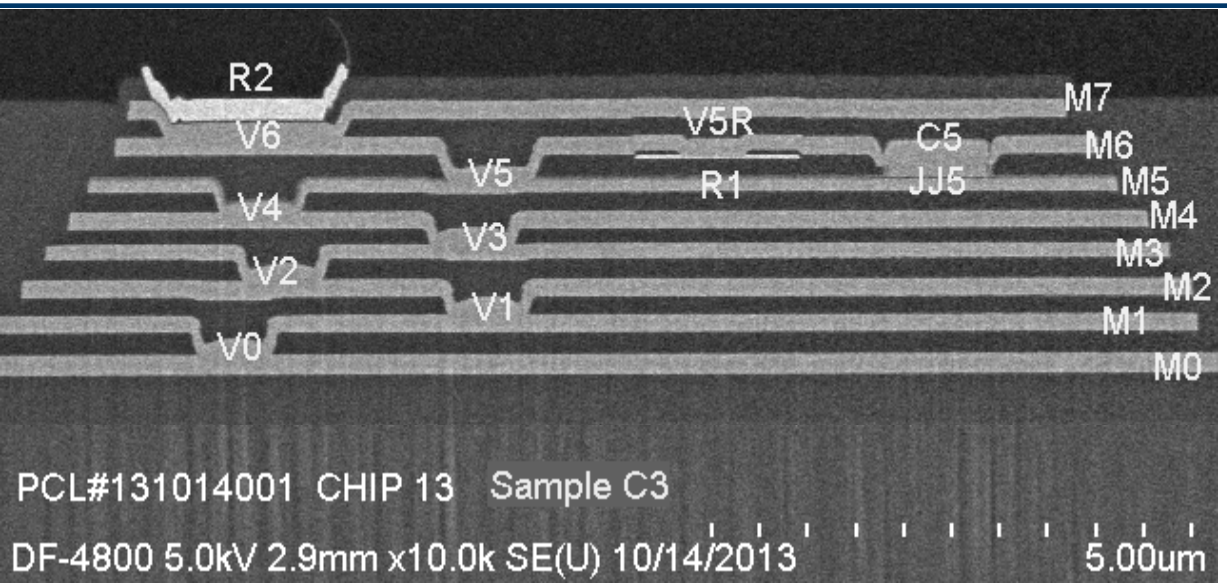
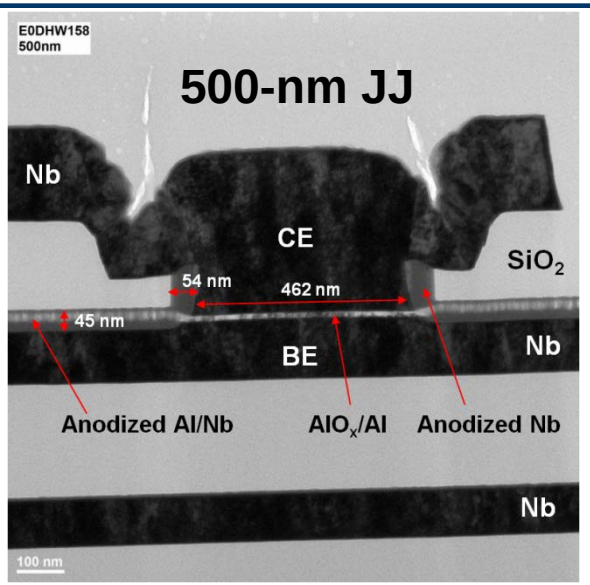
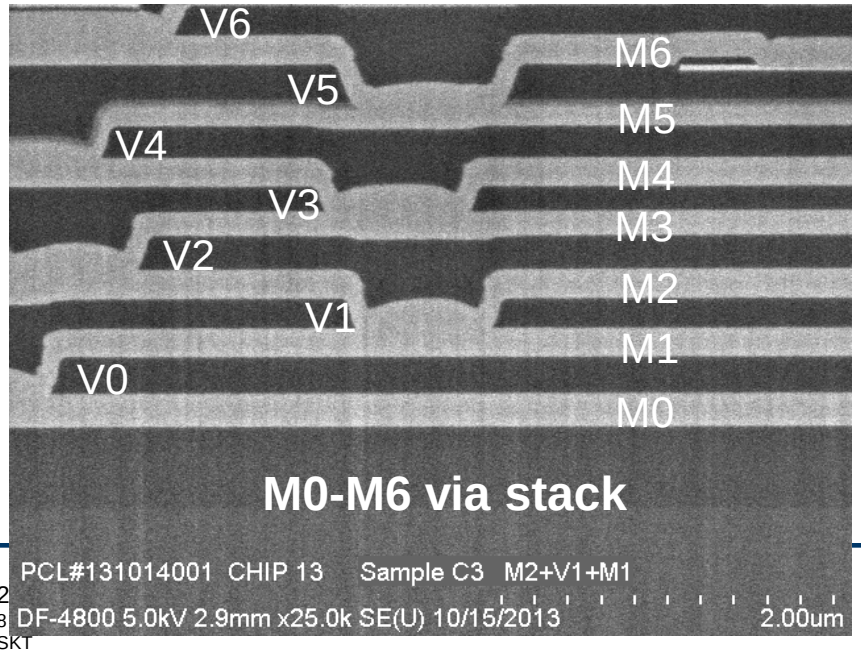
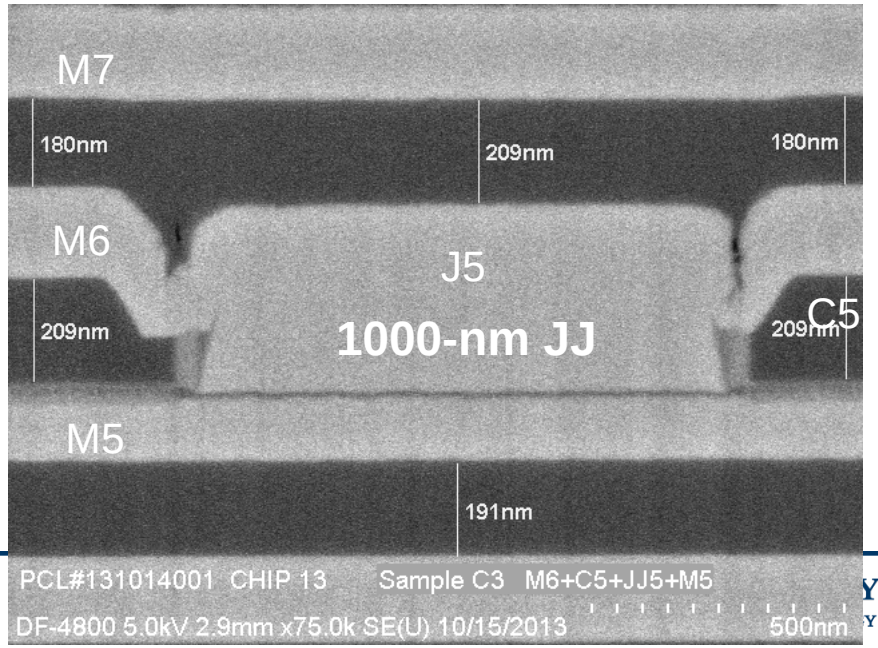
8-Metal-Layer Process Cross Sections









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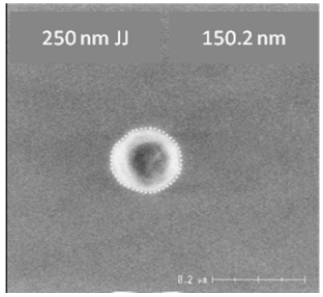
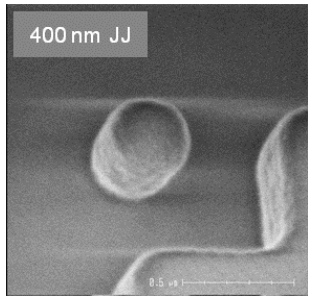
Photolithoraphy

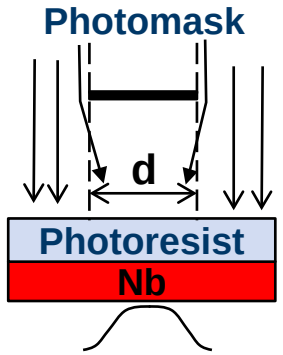
- **Key to VLSI and low parameter spreads, and high yield is photolithography**
- **Main challenge: accurate area definition of JJs of very different sizes (CD) in a manner preserving the proper relation between their I_cs**
- **For a single circular object (JJ), there is no theoretical resolution limit**
- **The practical resolution limit, d_c is set by the photoresist and the need to print correctly all different sizes**

$$d_c = \frac{2\lambda}{\pi NA}(1-\sqrt{I_{th}})^{1/2}$$

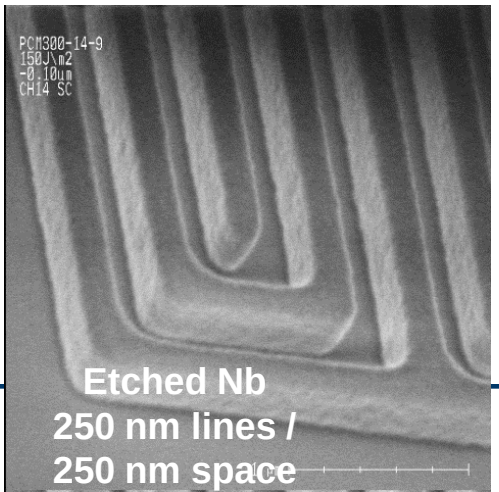
λ – exposure wavelength (248 nm or 193 nm), *NA* – numerical aperture, I_{th} – photoresist exposure threshold intensity

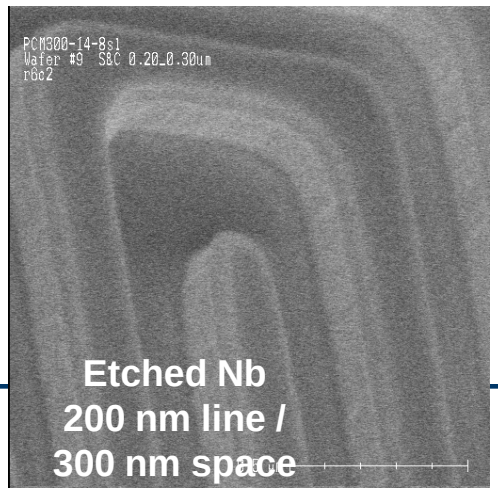






- **Photolithography cut-off d_c ~ 180 nm (248-nm tool) and ~ 110 nm (193-nm tool)**



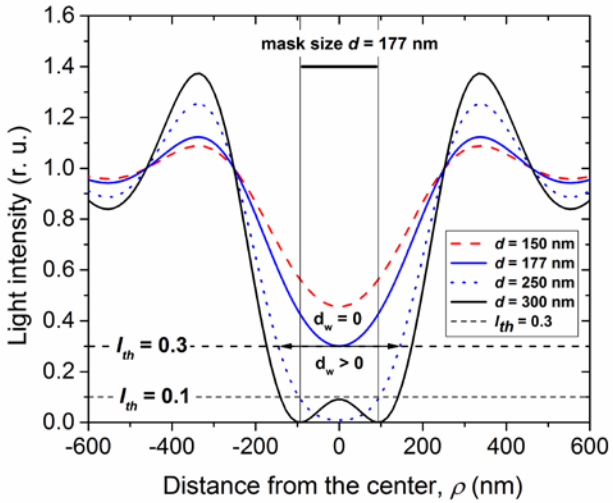


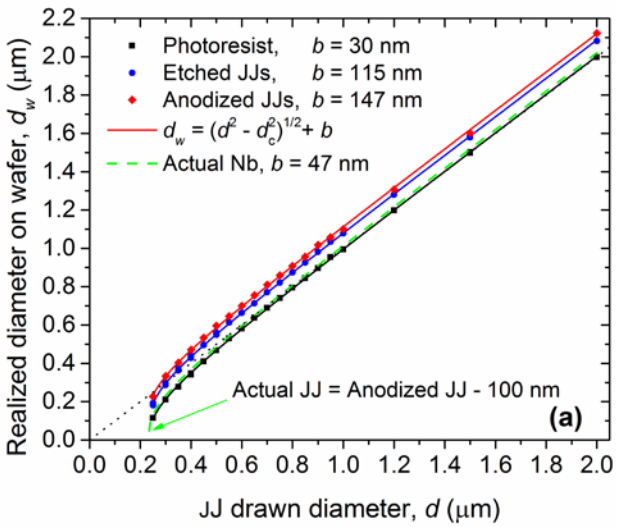
- **Theoretical resolution limit exists for the minimum pitch of periodic structures (line + space)**

$$p_{min} = \frac{\lambda}{NA(1+\sigma)}$$

- **p_{min} ~ 250 nm for 248-nm stepper and about 150 nm for 193-nm scanner**

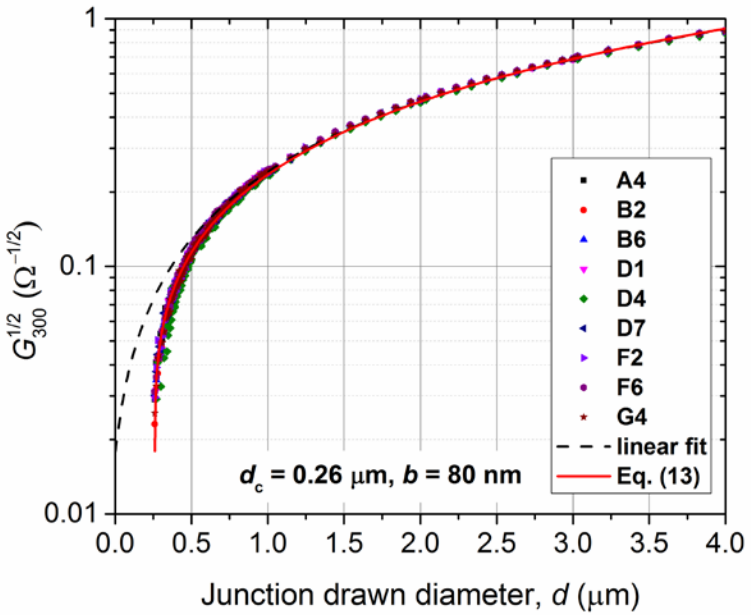
JJ Photolithography





- **Near the cut-off, the size of the image d_w is a highly nonlinear function of the drawn (mask) size d**

$$d_w = (d^2 - d_c^2)^{\frac{1}{2}} + b$$



JJ conductance scaling with d for 1296 test JJs per wafer, sizes from 250 nm to 4 μm; $G_{300} = G_0(\pi/4)[(d^2 - d_c^2)^{1/2} + b]^2$

The minimum printable size $d_c \approx 250$ nm for 248-nm and about 150 nm for our 193-nm photolithography

S.K. Tolpygo *et al.*, *IEEE Trans. Appl. Supercond.* (2015)

IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), October 2015.
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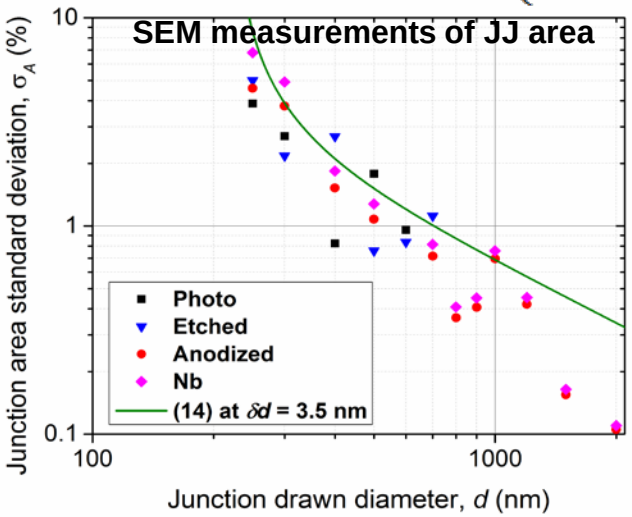
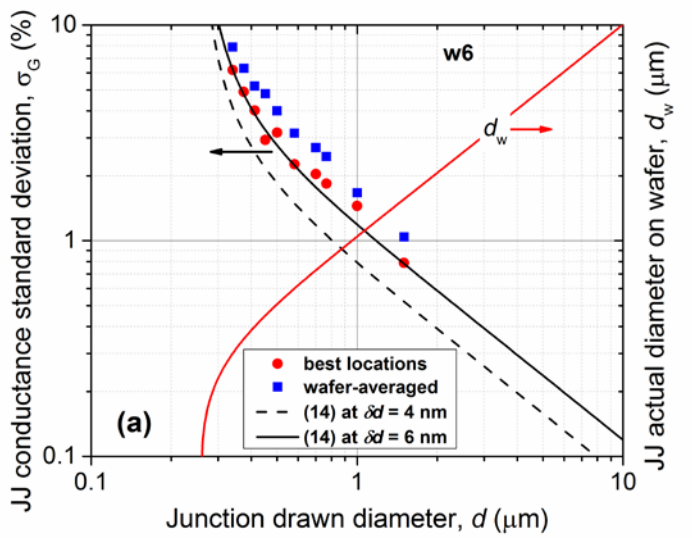
JJ Conductance and Critical Current Spreads

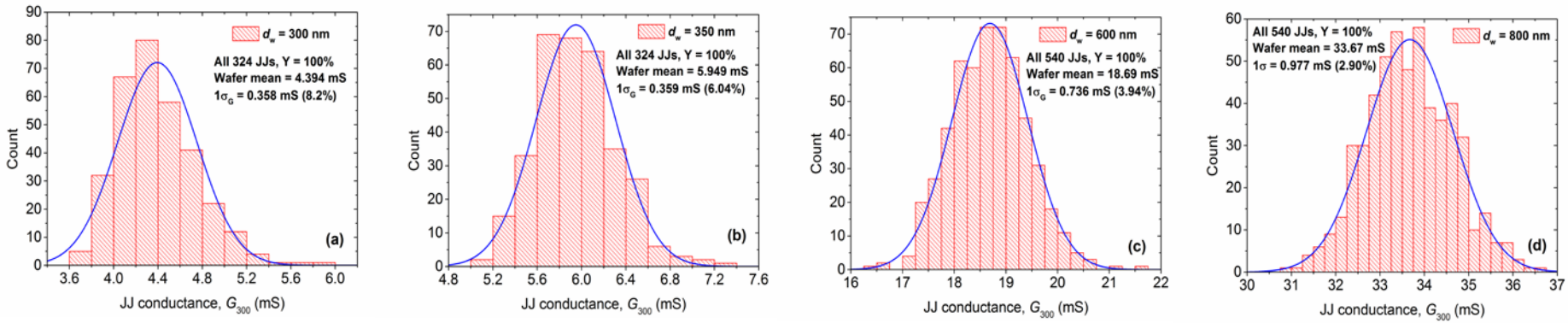
- **JJ area fluctuations are strongly enhanced near the photolithography cut-off size:**

$$\frac{\partial A}{A} = \frac{2(\delta d_w)}{d_w} = \frac{2d(\delta d)}{(d^2 - d_c^2)^{1/2}[(d^2 - d_c^2)^{\frac{1}{2}} + b]}$$





JJ conductance (critical current I_c) standard deviation on a typical wafer



The aggregate distribution of JJs on a 200-mm wafer for JJ diameters from 300 nm to 800 nm

S.K. Tolpygo *et al.*, *IEEE Trans. Appl. Supercond.* (2015)

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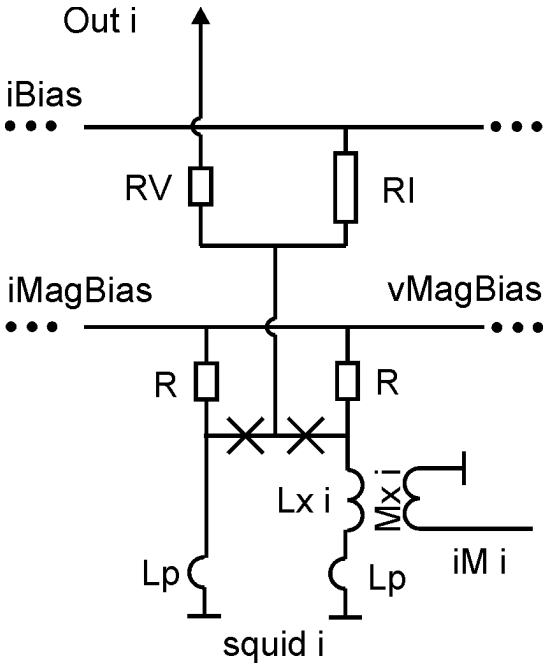
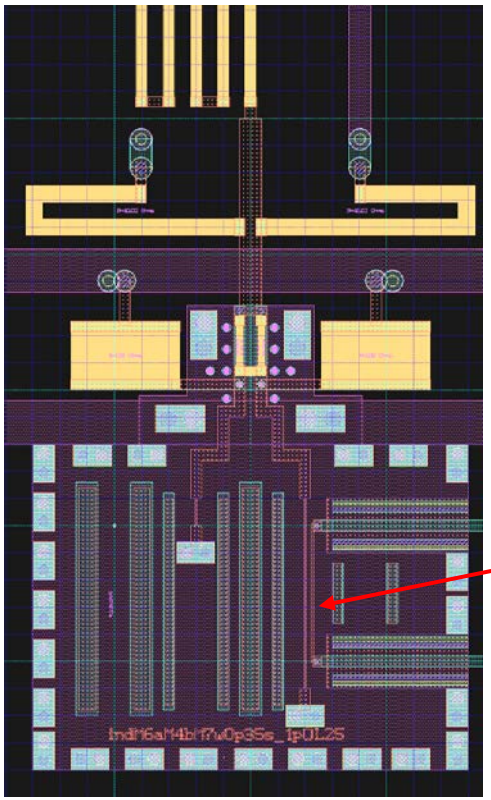
Inductance of Circuit Features

- **Extended inductance measurements down to 200 nm linewidth**
- **Extended measurements to mutual inductance between striplines and microstrips as a function of separation down to 250 nm to assess prospect for circuits densification and for transformers**
- **Measured inductance of etched staggered vias for SFQ4ee and SFQ5ee nodes**





The same circuit utilized to measure self inductance and mutual inductance

Two M4_M6_M7 coupled striplines

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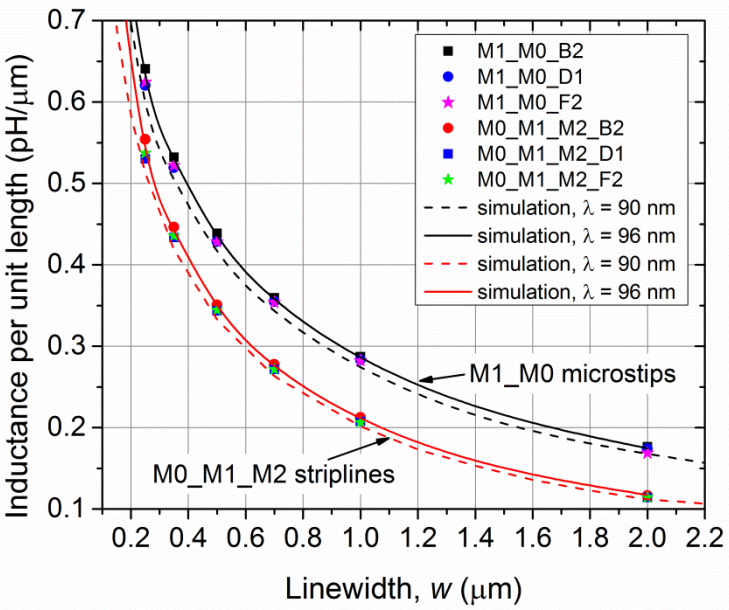
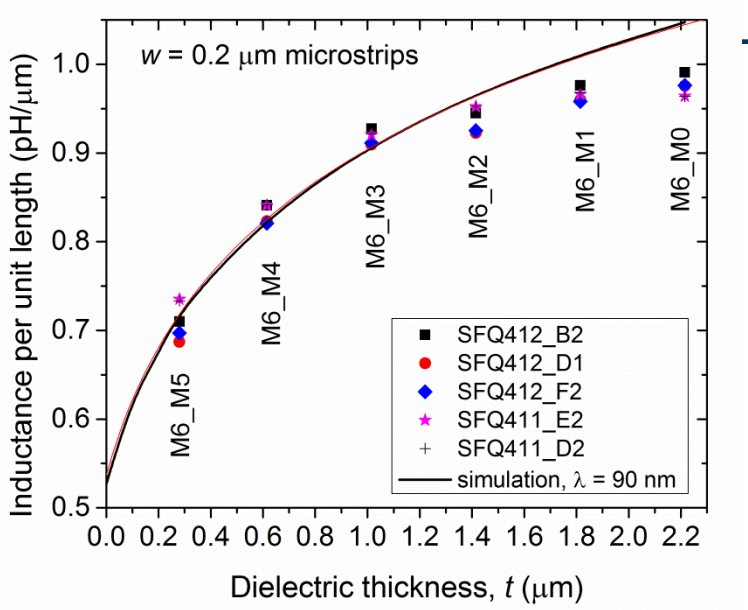
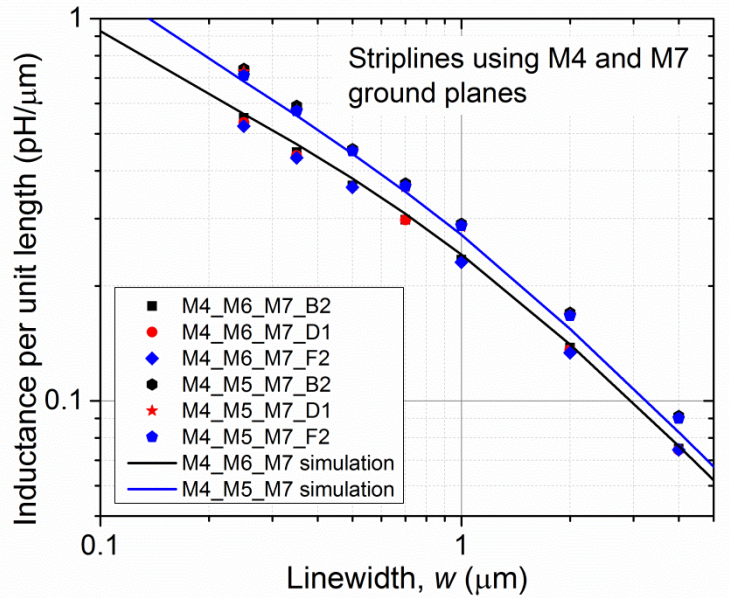
Circuit Inductances







- **Inductance of all microstrips and striplines agrees with the simulations within a few %**
- **Inductance spreads across 200-mm wafers is less than 3% for all linewidths**
- **Average inductance per 700-nm via between two layers:**

  0. 26 pH
- **Maximum circuit inductance is ~ 1 pH/μm**

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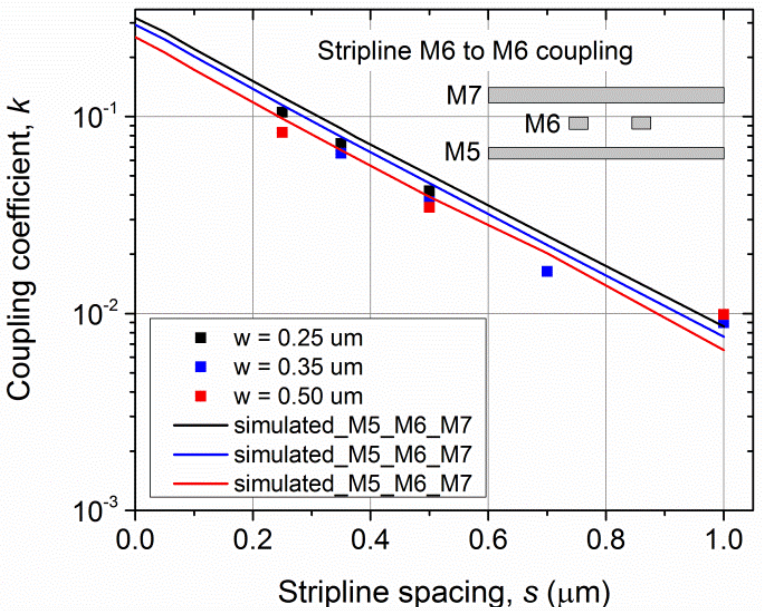
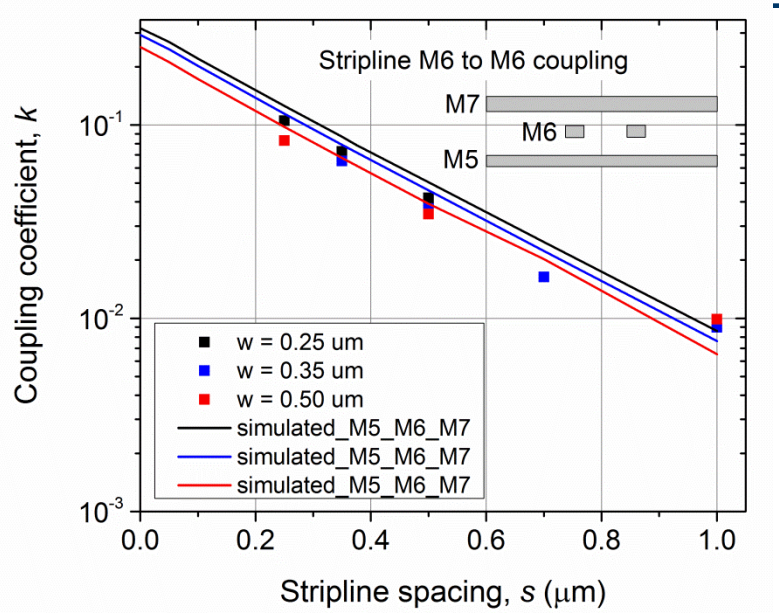
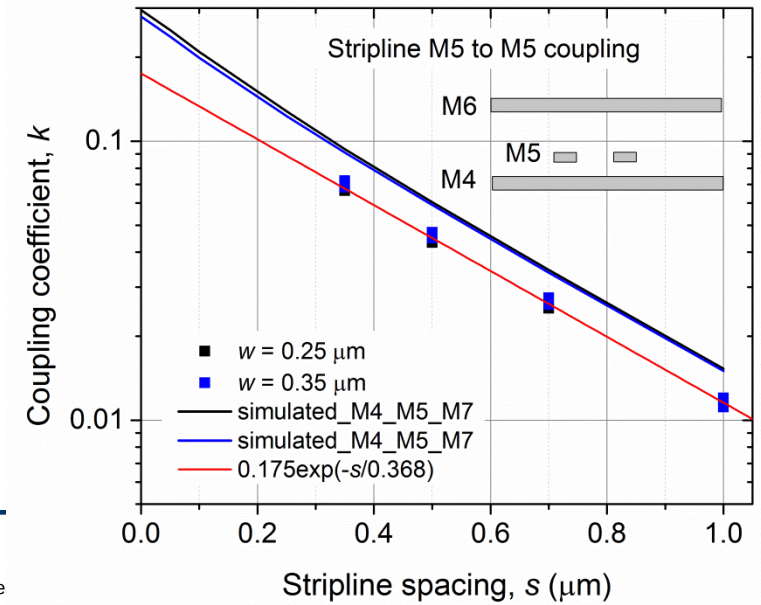
Coupling Between Stripline Inductors







- $M_{12} = k(L_1L_2)^{1/2}$ - mutual inductance
- Coupling was measured between M6-to-M6 and M5-to-M5 striplines. It agrees reasonably well (within ~ 20%) with 3D inductor simulations (LL program of M. Khapaev)
- In all cases, coupling coefficient *k* exponentially decreases with increasing spacing between the striplines, *s* – very sensitive electric test for line spacing

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Advanced Process Test Vehicle

- **Circuits with 1M JJs require yield of components at 99.999999% levels. A "100%" apparent yield of small (10^3) ensembles cannot predict the yield of large circuits**
- **The most comprehensive (but not the easy) way to test the process is to test the actual digital circuits**
- **Unfortunately, the answers are received in a binary format – "Yes" (works) or "No"**
- **Need a digital circuit scalable to ~1M JJs as a process benchmark**
- **Enable access to margins of individual cells in the circuit to see what's wrong**
- **It cannot be a dc-biased RSFQ or ERSFQ circuit with parallel biasing – cannot be scaled to 1M JJs**
- **We employed a very old (before SFQ) idea: ac-biased, "inhomogeneous" flux shuttle**

G.M. Lapir, K.K. Likharev, and V.K. Semenov, *Zh. Tekn. Fiz*. (1977) and K.K. Likharev, *IEEE Trans. Magn*. (1977)

V.K. Semenov, Yu. Polyakov, and S.K. Tolpygo, *IEEE Trans. Appl. Supercond*. (2015)

IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), October 2015.
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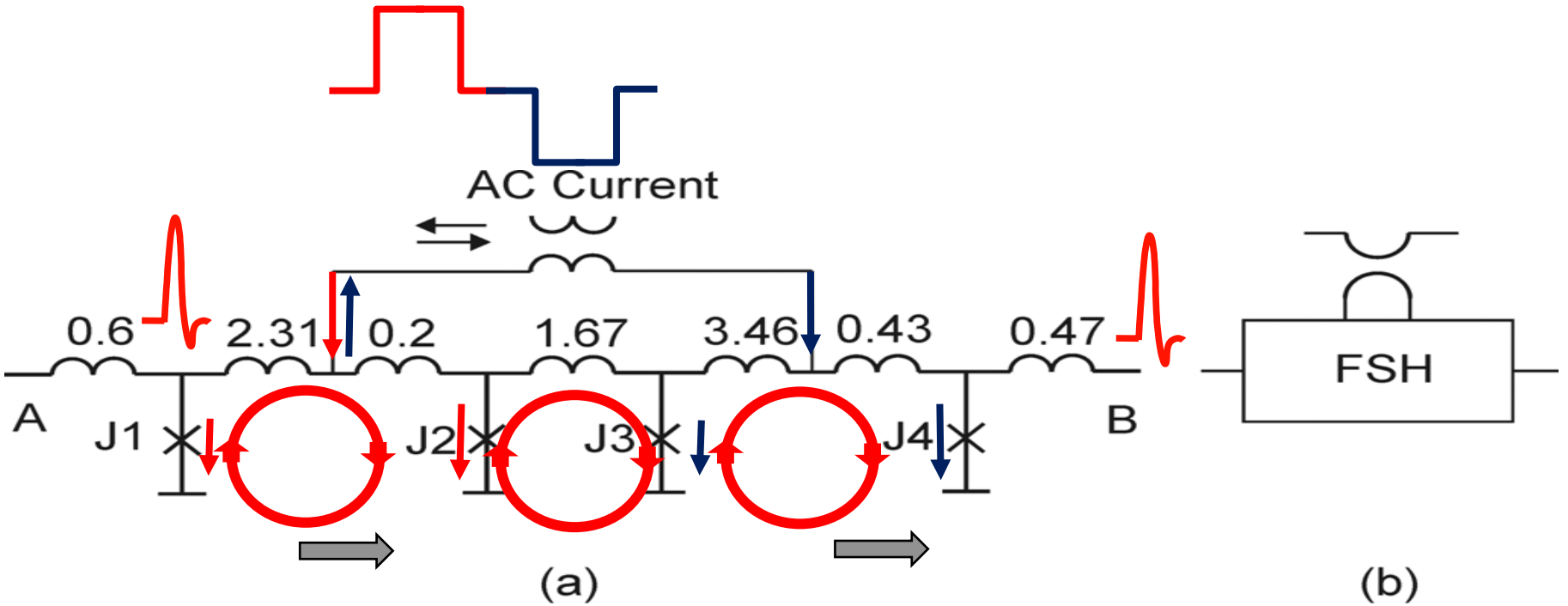
Flux Shuttle (FSH) Cell



- **Write “1” between J1 and J2; fluxon stays there because the induced current is not enough to flip J2**
- **Apply positive half-period of AC clock; it creates positive bias of J2**
- **J2 switches and fluxon (“1”) is pushed through nonquantizing loop between J2 and J3 into a stable position between J3 and J4**
- **“1” cannot move further because J4 is negatively biased (current flows up from GND)**
- **Apply negative half-period of AC clock**
- **Now current in J4 adds to the circulating current. J4 switches producing an output SFQ pulse**
- **During the clock cycle, information in FSH cell is shifted by one cell – ac-biased shift register cell**

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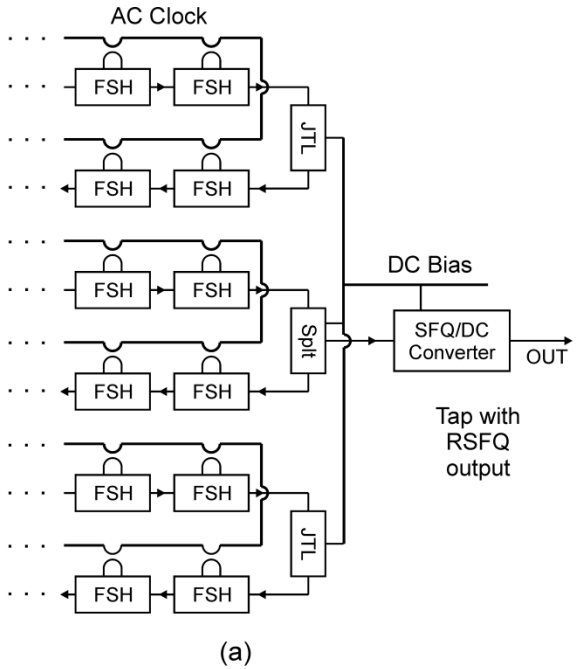
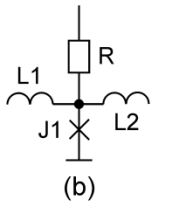
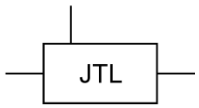
Flux Shuttle-Based Shift Register



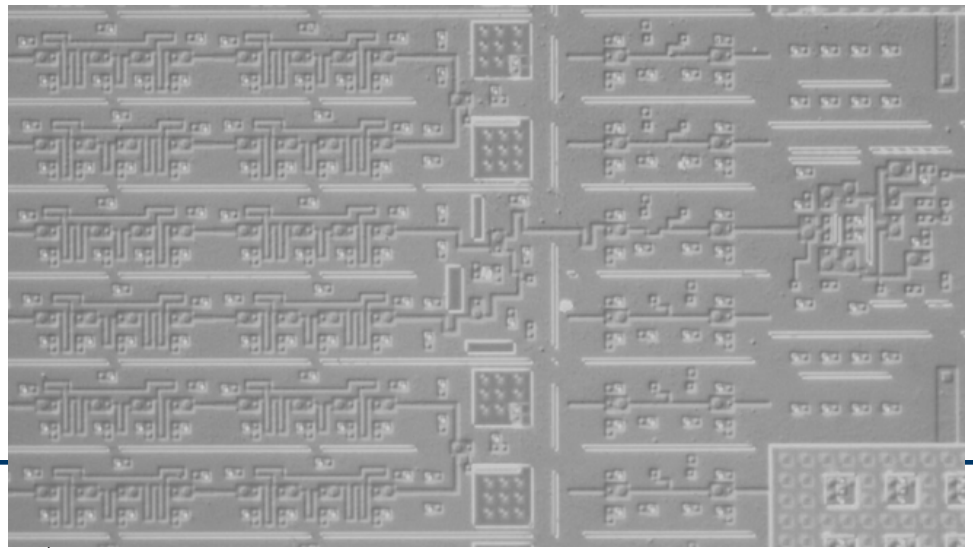
(a)



(b)

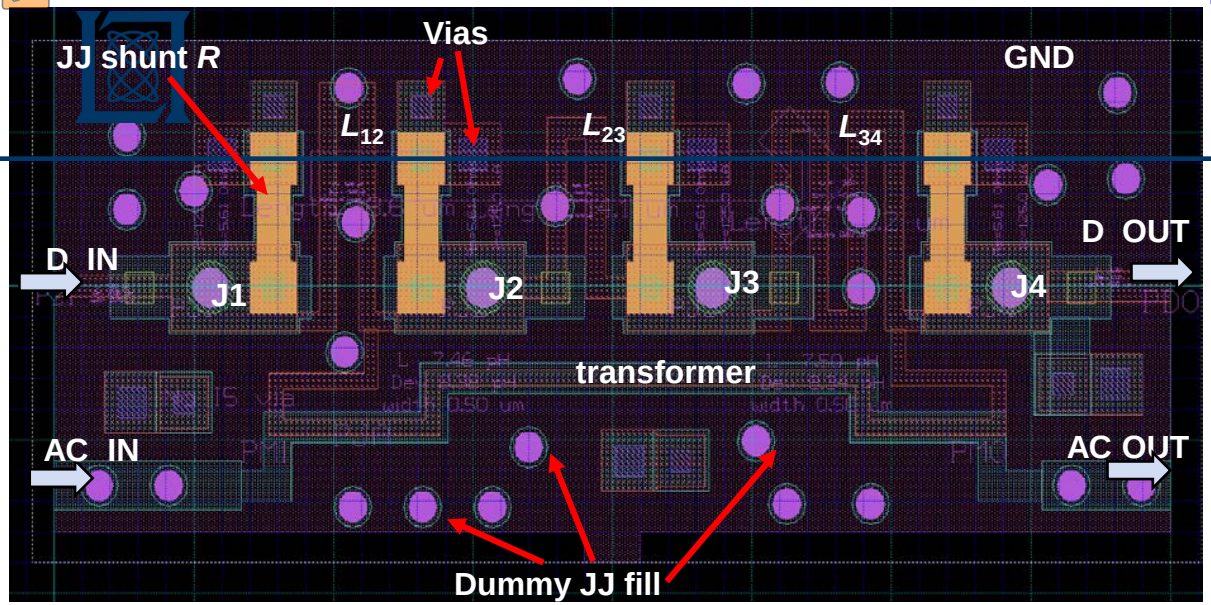


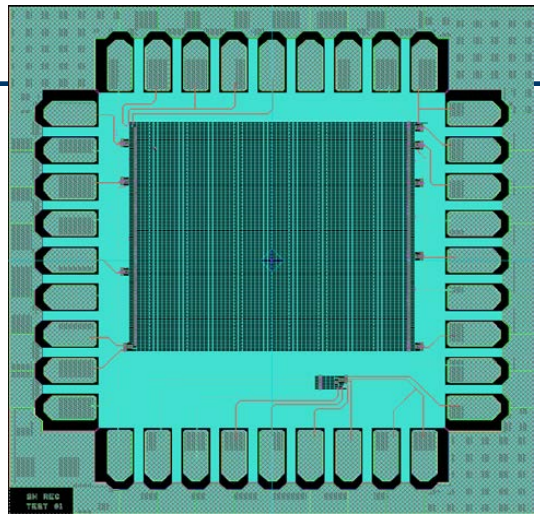
(c)

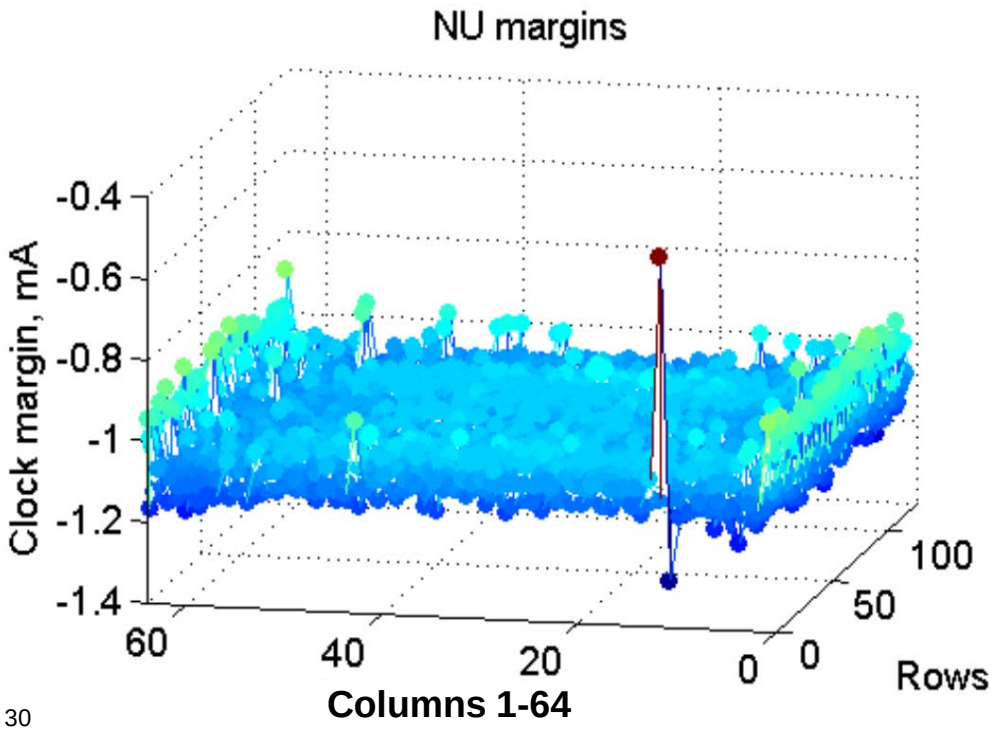


- Meander (snake) configuration
- 64 FSH cells in a row (x-direction), 128 rows (y-direction)
- 64x128 = 8192-bit shift register
- Rows are connected by short JTLs (dc-biased)
- Data propagate to the right (+x-direction) in the odd rows and to the left (-x) in the even rows
- SFQ pulses at the end of each row are transferred in the y-direction to the next row via these JTLs
- There are 7 taps allowing for monitoring the data propagation, using dc-biased Splitters and dc-biased SFQ/DC output converters
- AC-biased and dc-biased cells are used in the same circuit – their data terminals are simply connected
- **Total number of JJs is slightly over 32,800**

V.K. Semenov, Yu. Polyakov, and S.K. Tolpygo, *IEEE Trans. Appl. Supercond.* (2015)







- 8192-bit shift register (128 rows x 64 columns)
- 40 μm x 17 μm cell, 4 JJs per cell
- 32,800+ JJs
- Junction density = $6 \cdot 10^5$ JJ/cm^2
- Fully operational, margins of each cells measured
- Min linewidth: 0.5 μm
- SFQ4ee process, but using only 4 metal layers
- SBU design (V. Semenov)

V.K. Semenov, Yu. Polyakov, and S.K. Tolpygo, *IEEE Trans. Appl. Supercond.* (2015)

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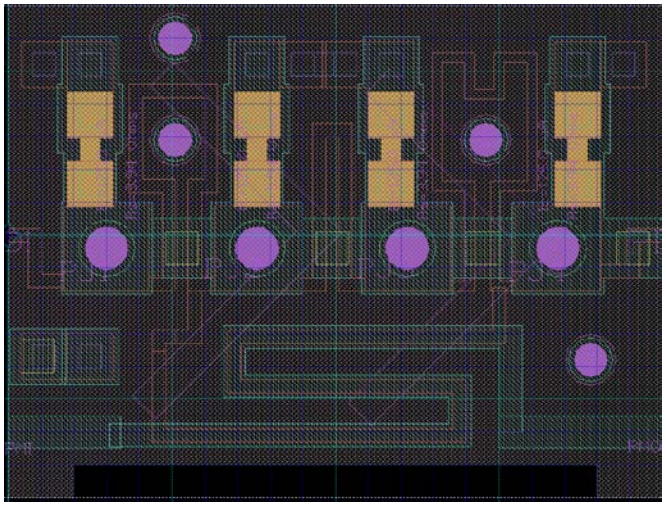
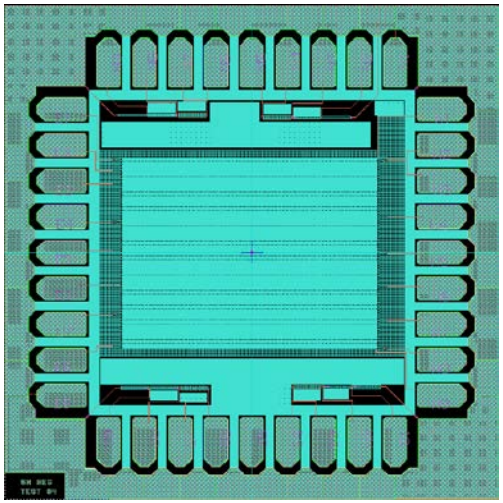
Current Benchmarking Circuits

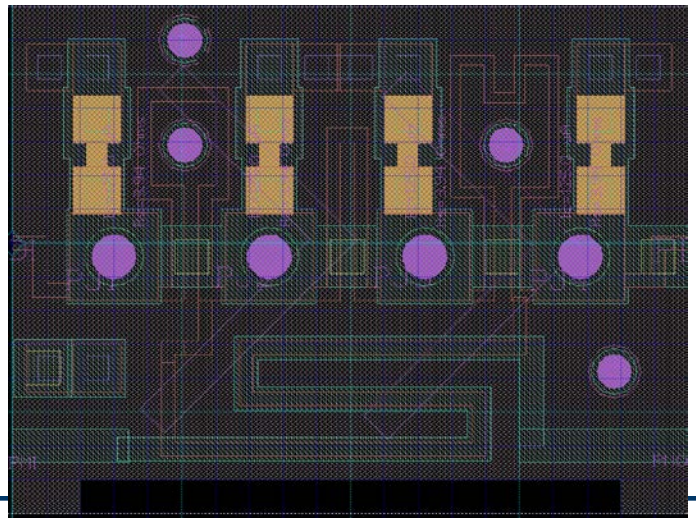
2nd Generation

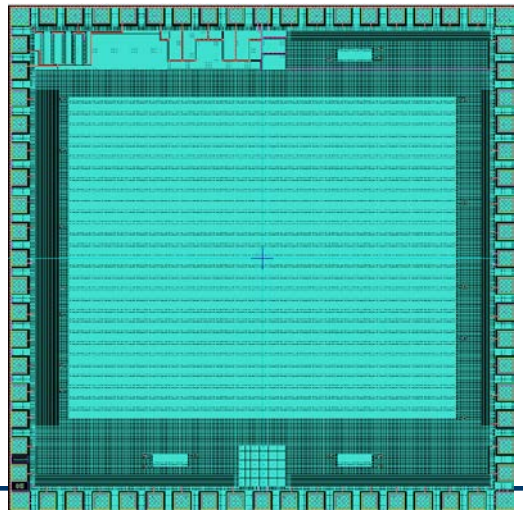




- 16,250-bit ShReg
- Status: fabricated, fully operational
- Cell size: 20 μm x 15 μm
- JJ density: $1.33 \cdot 10^6$ JJ/cm^2
- JJ count: 65,000+
- Min linewidth: 0.4 μm
- SFQ412 reticle set

3rd Generation





- 36,000-bit ShReg
- Status: fabricated, in test
- Cell size: 20 μm x 15 μm
- JJ density: $1.33 \cdot 10^6$ JJ/cm^2
- JJ count: 144,000+
- Min linewidth: 0.4 μm
- SFQ413 reticle set

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Outline

- **Introduction**
  - **MIT-LL Fab description**
  - **SFQ fabrication process nodes and the roadmap**
- **SFQ4ee process characterization and highlights**
  - **Photolithography and junctions**
  - **Circuit inductors**
  - **Process benchmarking circuits: AC-biased shift registers**
- **SFQ5ee process highlights: linewidth reduction to 0.35 μm**
  - **High-sheet-resistance layer**
  - **Second resistive layer: sandwich-type interlayer resistors**
  - **High-kinetic inductance layer (9th superconducting layer)**
- **Conclusion**

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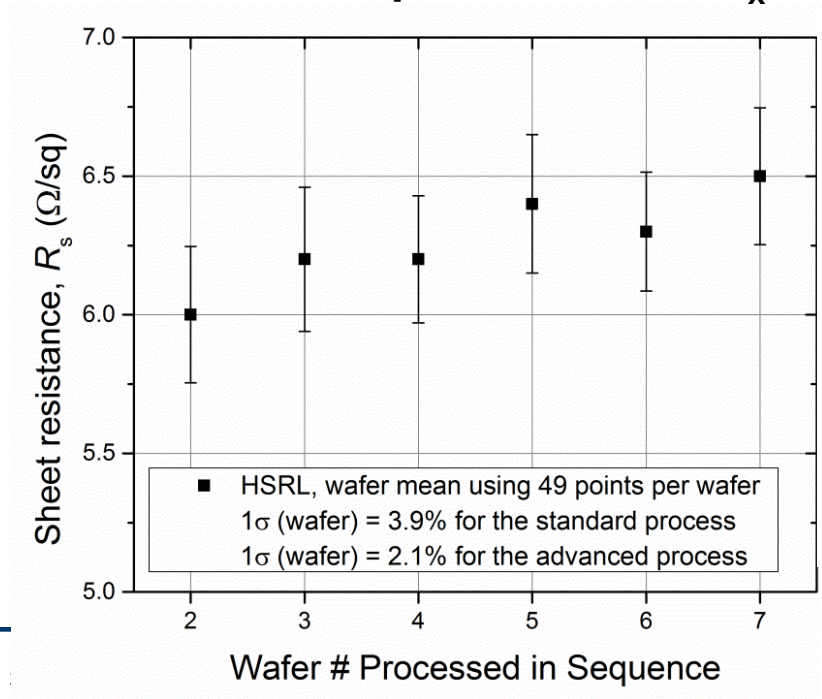
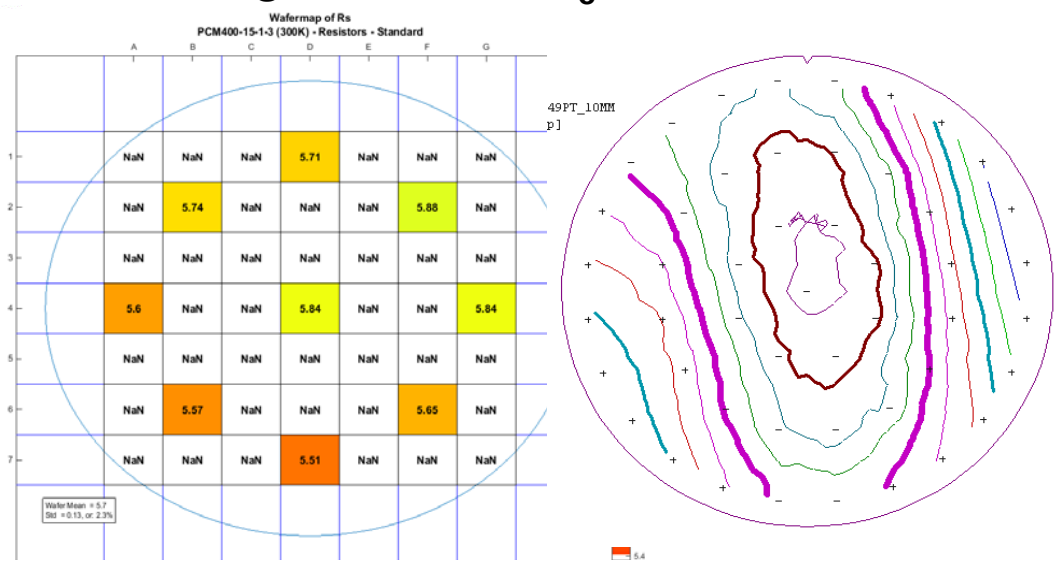
High Sheet Resistance Layer (HSRL)

- **Technical need: decrease area occupied by resistors**
  - **At current DRs (w = 0.5 μm, R_s = 2 Ω/sq), A_r ~ 5 μm² for a 1-μm² JJ (5x JJ area)**
- **Technical solutions:**
  - **Increase R_s to 6 – 7 Ω/sq**
  - **Decrease linewidth to 0. 25 μm**
  - **Reduce resistor vias area down to ~ 0.3 μm²**
  - **Self-shunted JJs (A_r = 0)**

  } **– Resulting in A_r ~ A_J**

Implemented MoN_x with low nitrogen content, T_c < 3 K





R_s wafermap for an advanced MoN_x process
Wafer 1σ = 2.3% on patterned resistors

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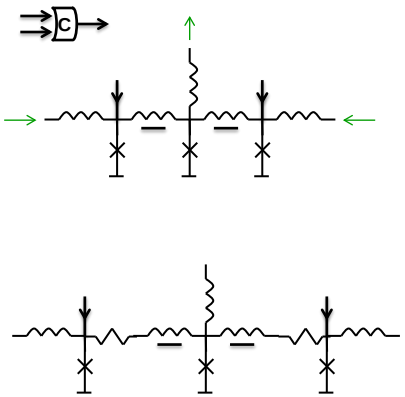
Second Resistive Layer for mΩ-range Resistors

Miller cell ("C" element)

Courtesy of A. Kirichenko, HYPRES



- Simplest cell in RSFQ
  - Only 3 JJs
  - Very reliable
  - Major cell in synchronization and handshaking
- Never "forgets"
  - Sometimes it's useful
  - If faulted, requires complete "defluxing"
    - Solution: breaking superconducting loop with tiny (~ 1 μΩ) resistors

- **Technical need**
  - SFQ circuits are sensitive to flux trapping: external and internally generated flux
  - With circuit density increasing, flux trapping may increase due to diminishing distance from flux-trapping moats and inductors and due to reducing size of the moats
  - Some SFQ cells are particularly sensitive, e.g., a C-cell

- **Possible solutions:**
  - Breaking some of the superconducting loops by a mΩ-range resistors
  - Improving circuit immunity to flux trapping by optimizing moat design and finding critical fields (Vasili Semenov, SBU)
  - Reduction of linewidth should reduce flux trapping in circuit traces (but not in ground planes)
- **Fab solution: add an extra resistive layer**
  - Planar resistor does not give mΩ range
  - Film resistance in a perpendicular to the plane direction (z-direction) can be utilized

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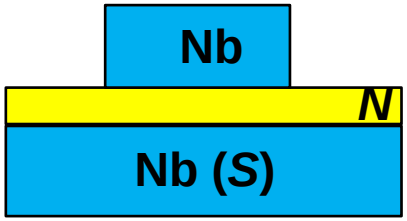
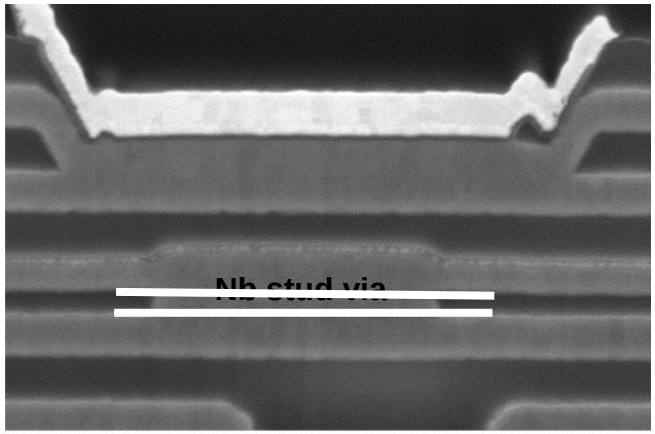
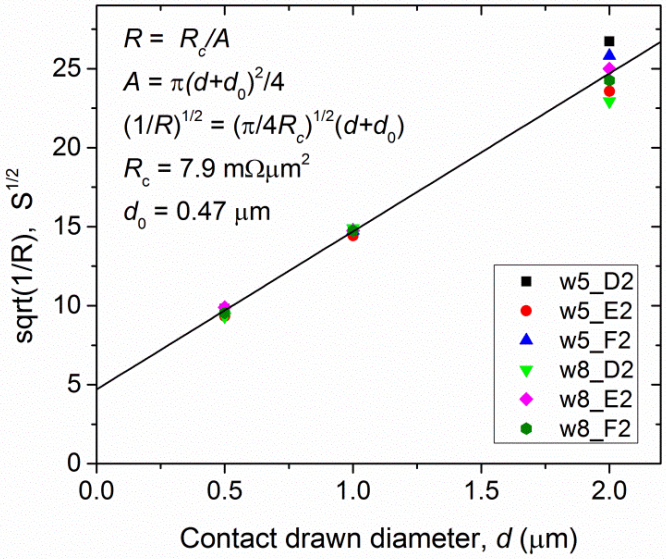
Interlayer, Sandwich-Type Resistors







Resistance of an SNS junction: $R = R_s t^2/A + \rho_c/A$

- A – junction (contact) area
- R_s – sheet resistance of the *N* (resistor) layer
- t – resistor thickness, >> superconducting coherence length
- ρ_c – interface (contact) resistance of unit area

Typical parameters (*e.g.*, Ti, Mo, MoN_x, W, etc. films):
R_s = 2 - 6 Ω/sq, t = 40 nm – 80 nm
$RA = 3.2\ m\Omega\mu m^2 + \rho_c$ and $1/R = A/(R_s t^2 + \rho_c)$

Results

- **Implemented with our stud-via technology (Nb pillars as interconnects) and *R*-layer between Nb stud and Nb wiring layer**
- **Main difficulty: not form a Josephson junction with $I_c > L/\Phi_0$**
- ***RA* (specific resist.) measured = 7.9 mΩμm²**
- **Interface resistance ρ_c = 4.7 mΩμm² after deducting resistive component due to *N*-film of 3.2 mΩμm²**

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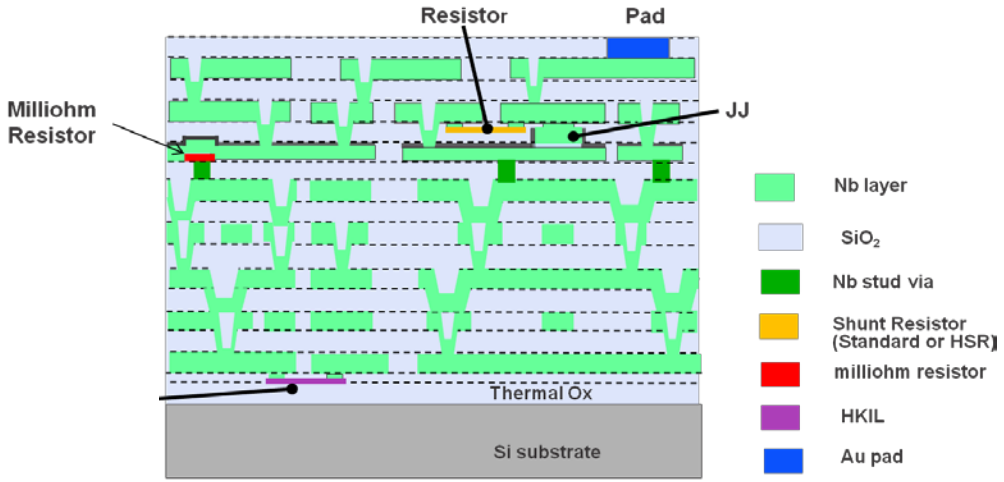
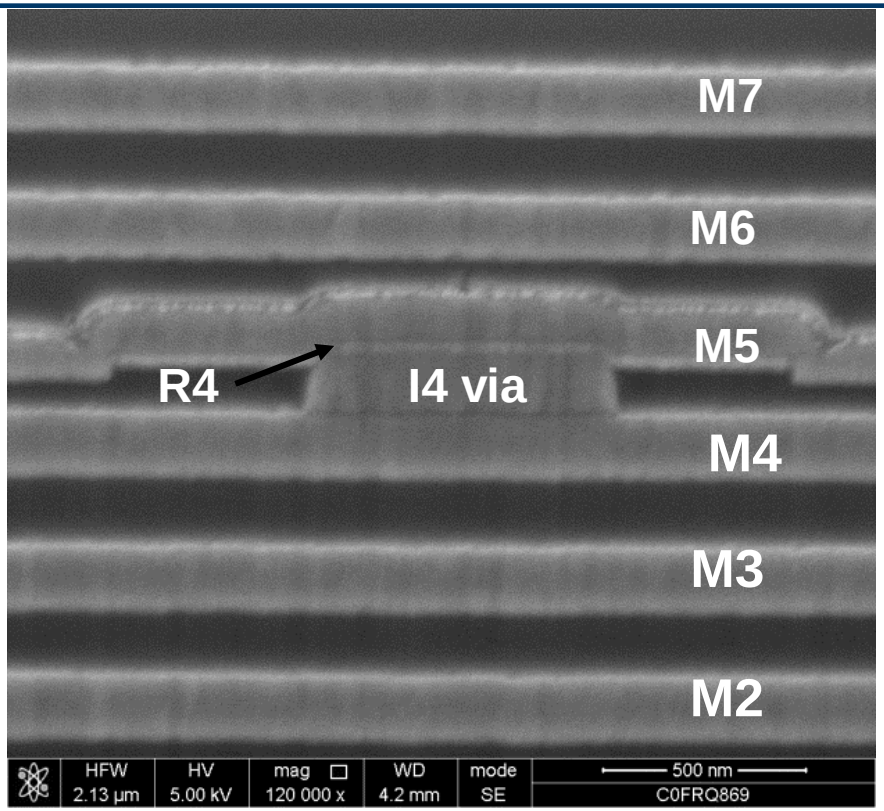
Summary on mΩ-range Resistors



Cross-section of the SFQ5ee process with mΩ-resistor layer, R4, between layers M4 and M5



- **Sandwich-type resistors between two Nb layers (SNS junctions) have been realized using our stud-via technology (using Nb pillars as interconnects)**
- **Standard resistor layer materials (Mo, Pt, Ti, etc.) are fine for the task unless Josephson JJ is formed.**
- **Extensive tests have been done on perpendicular Mo and MoN_x resistors with t = 40 nm – 80 nm; ± 25% variation run-to-run is expected – fine for the application intended**

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High-Kinetic-Inductance Layer

- **Technical need:**
  - **Energy-efficient RSFQ requires multiple 100-pH bias inductors replacing bias resistors in RSFQ in order to eleminate static power dissipation**
  - **Each (geometric) inductor occupies typically ~ 100 μm^2 area, L_g < 1 pH/sq**
  - **No VLSI is possible with such geometric inductors**
- **Kinetic inductance L_k of thin superconducting films is much larger than their geometric inductance:**
  - **$L_k = N_{sq}\mu_0\lambda^2/d$, λ is magnetic field penetration depth, d film thickness (d << λ), and N_{sq} number of squares**
  - **$L_g \sim \mu_0(2\lambda+t)N_{sq}$ for microstrips, where $t \sim d$ is the dielectric thickness**
  - **If λ >> d, $L_k/L_g \sim \lambda/3d$ >> 1 (microstrips and striplines)**
  - **For a planar coil, $L_k/L_g \sim 2\pi\lambda^2/(dw)$ >> 1 if λ >> d and λ > $w/(2\pi)$**
- **For practicality: d ~ 35 nm - 40 nm, so λ needs to be ~ 400 nm – 500 nm**
- **Area savings: at L_k = 10 pH/sq and w = 0.7 μm, $A_k \sim A_g/20$**

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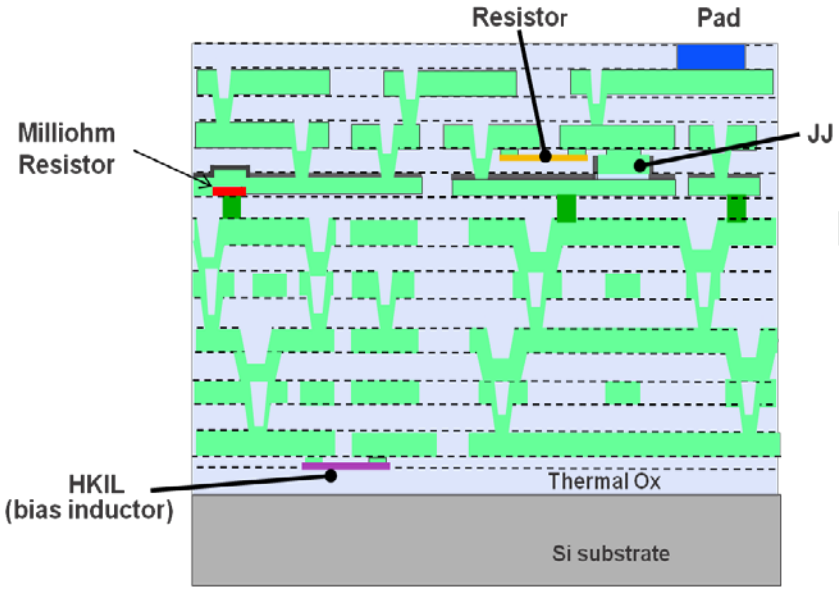
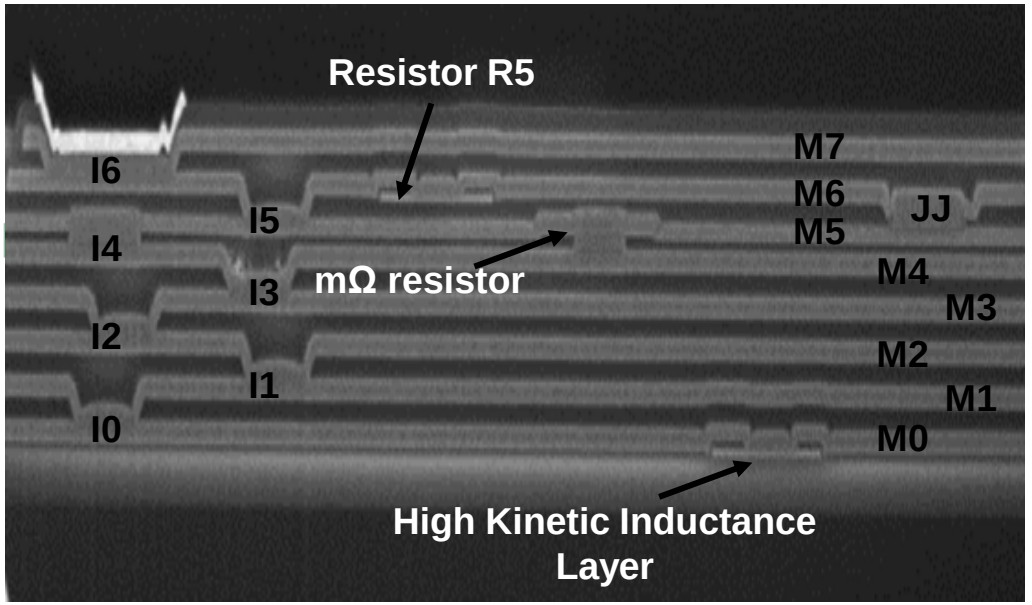
HKIL Summary





- **Wide selection of materials: nitrides, carbo-nitrides, and silicides of transition metals and alloys have large λ**
- **Any new material requires additional deposition chamber: Molybdenum (resistors)**
- **Trade-offs: T_c, I_c, d vs L_k, film stability and uniformity**
- **Quick screening on unpatterned films using dielectric resonator techniques**
- **Inductance measurements of fully processed inductors using SQUIDs**
- **Full process runs with MoN_x HKIL have been done: L_k, I_c, targeting and uniformity measurements**

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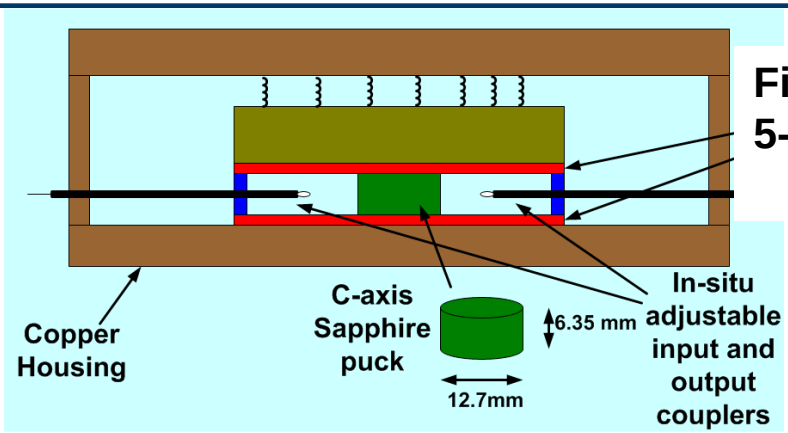
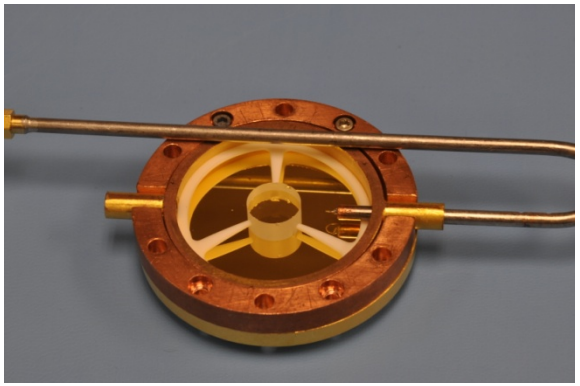
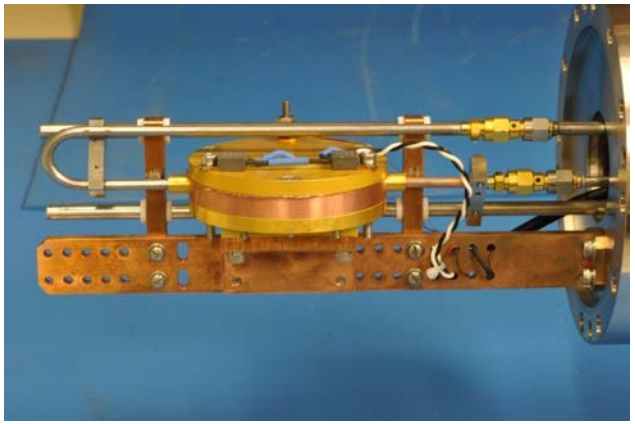
Dielectric Resonator Technique

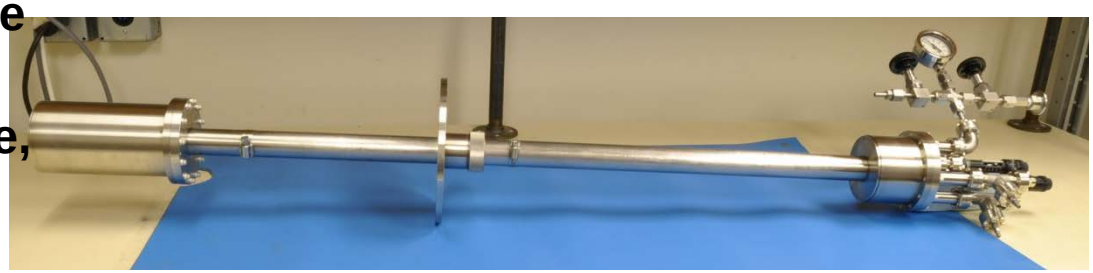


Films under test, 5-cm diameter





- **Can be used with metallic or dielectric substrates**
- **Designed for relatively high-power measurements**
- **Fundamental frequency = 10.7 GHz**
- **TE_{011} mode**
- **Unpatterned film, nondestructive test**
- **Magnetic field parallel to surface, similar to cavity**



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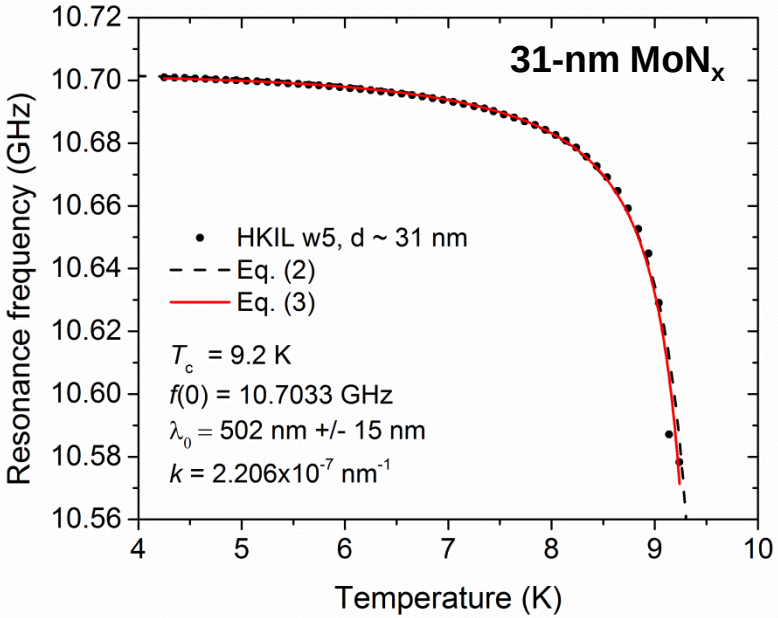
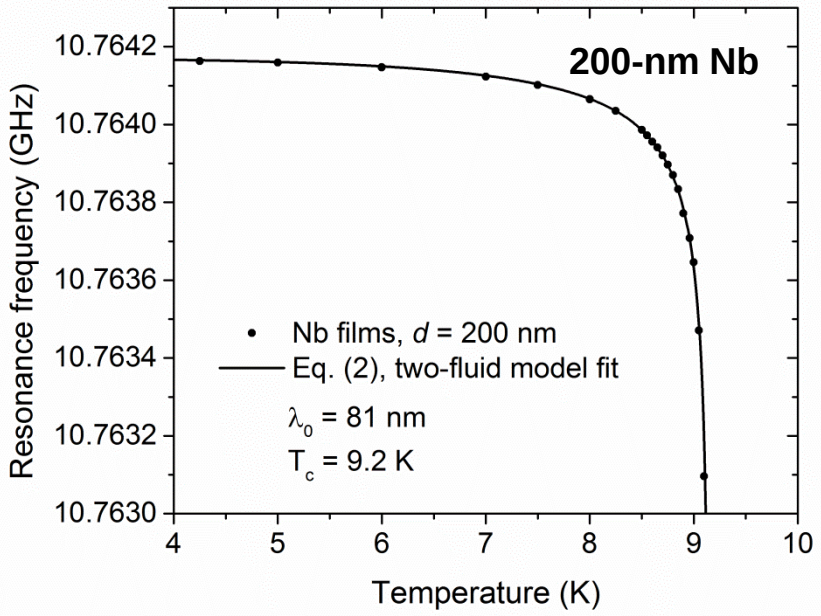
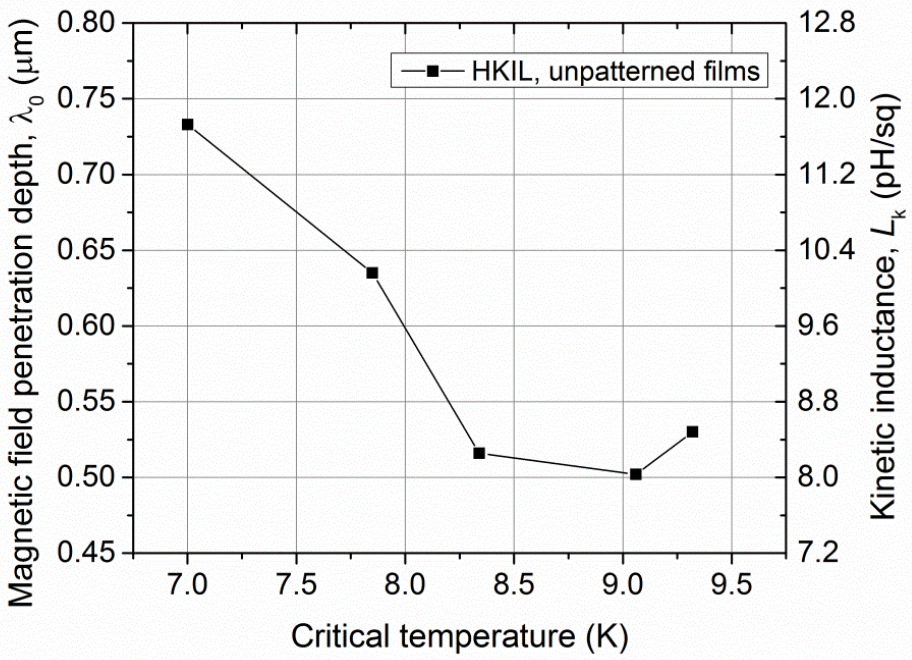
Examples of HKIL Results







- **For Nb films, the typical frequency shift with *T* is ~ 1 MHz**
- **For HKIL, the shifts are ~ 100 MHz, indicating a 100x higher effective penetration depth**
- **Indeed, at λ_0 = 502 nm, λ(4.2K) = 512 nm and**
  $\lambda_{eff} = \lambda^2/d$ = 8.5 μm (vs 81 nm in Nb)
- **$L_k = \mu_0\lambda_{eff}$ = 10.4 pH/sq, and a 100-pH inductor requires only 10 squares, A ~ 6 μm²**

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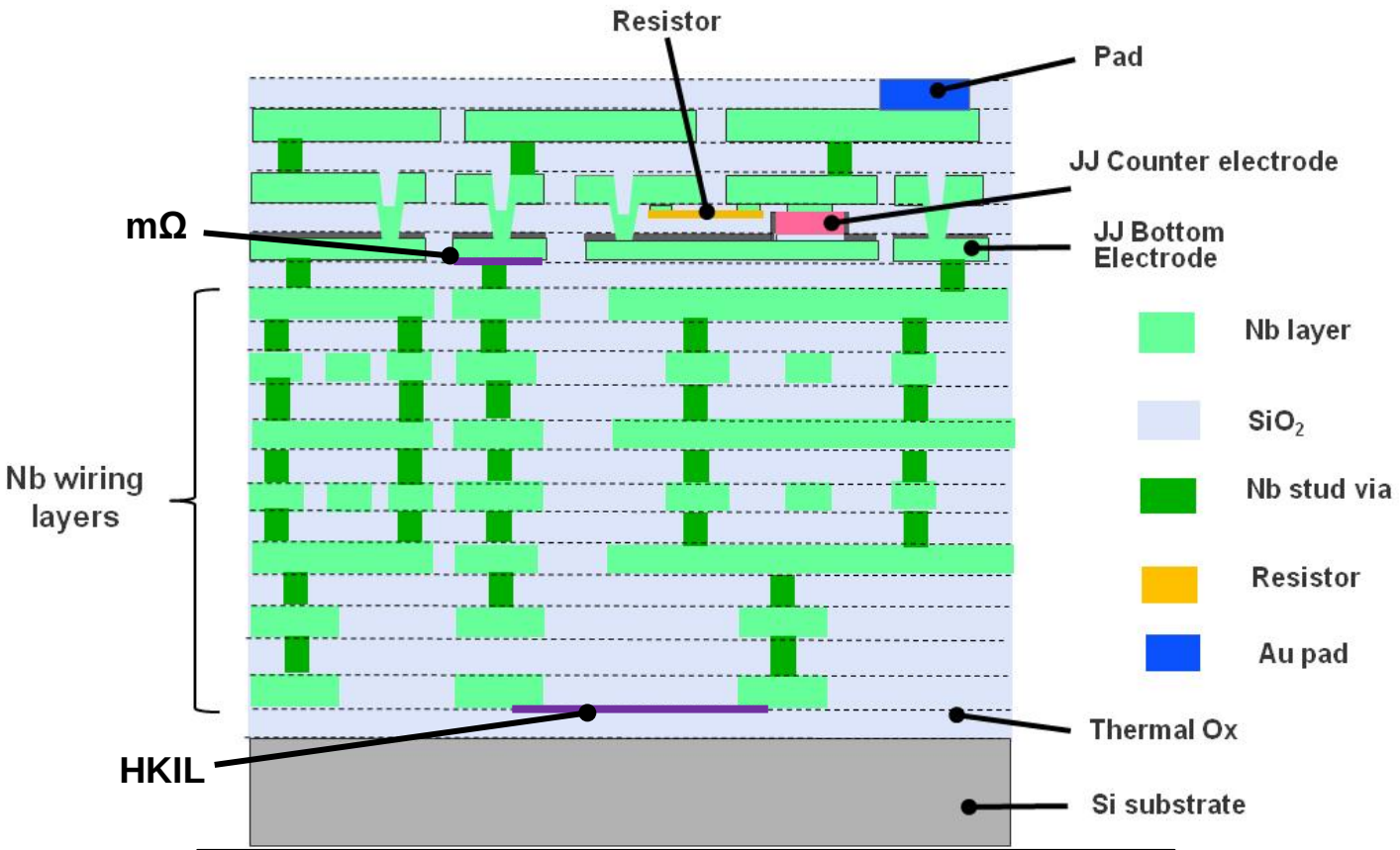
SFQ7ee Node: Target 10-Nb + 1 Pro



- 10 Nb layers
- 500 nm diameter Josephson junctions
- Wiring: 250 nm width, 250 nm spacing
- Stud vias: 300 nm
- Two layers of resistors (HSRL + mΩ)
- High-kinetic-inductance layer

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Conclusion

- **We have developed a fully planarized 8-Nb-layer fabrication process on a tool set of a typical CMOS foundry with 248-nm photolithography → transition to 193-nm**
- **Our SFQ4ee process is high yielding based on extensive PCM data and high yield of operational circuits with 33k, 65k, and 72.8k JJs**
- **We have demonstrated high uniformity and reproducibility of JJ with diameters down to 500 nm and below, and inductors down to 250 nm, sufficiently high to enable VLSI superconducting circuits with over 10^6 JJ/cm^2 at 10 kA/cm^2 and 20 kA/cm^2 current densities**
- **We have also developed the next process node, SFQ5ee (8+1), with an additional layer of mΩ resistors, 6 Ω/sq resistors, and a high-kinetic-inductance layer**
- **Our goal is a 10-Nb+1 layer planarized process with 180 nm linewidth and 380 nm pitch in 3 years**
- **VLSI SFQ circuits with > 100,000 JJs will be demonstrated before the end of this year, and with ~ 1,000,000 JJs before the end of this decade**
- **Many new circuit design, materials, and fabrication process innovations and discoveries will be needed in order to cross over the 10M - 20M JJs per circuit barrier**
- **Design for manufacturability and increasing circuit margins are the key to VLSI of SFQ circuits**

An animated PowerPoint version of this presentation is available here.