IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), February 2019.
Invited presentation 1EOr2A-01 given at ASC 2018, October 28-November 02, 2018, Seattle, (USA).

Digital Output Data Links from Superconductor Integrated Circuits

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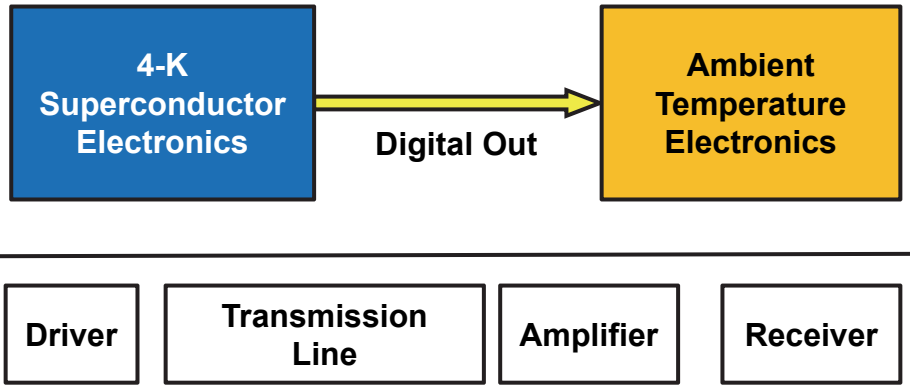
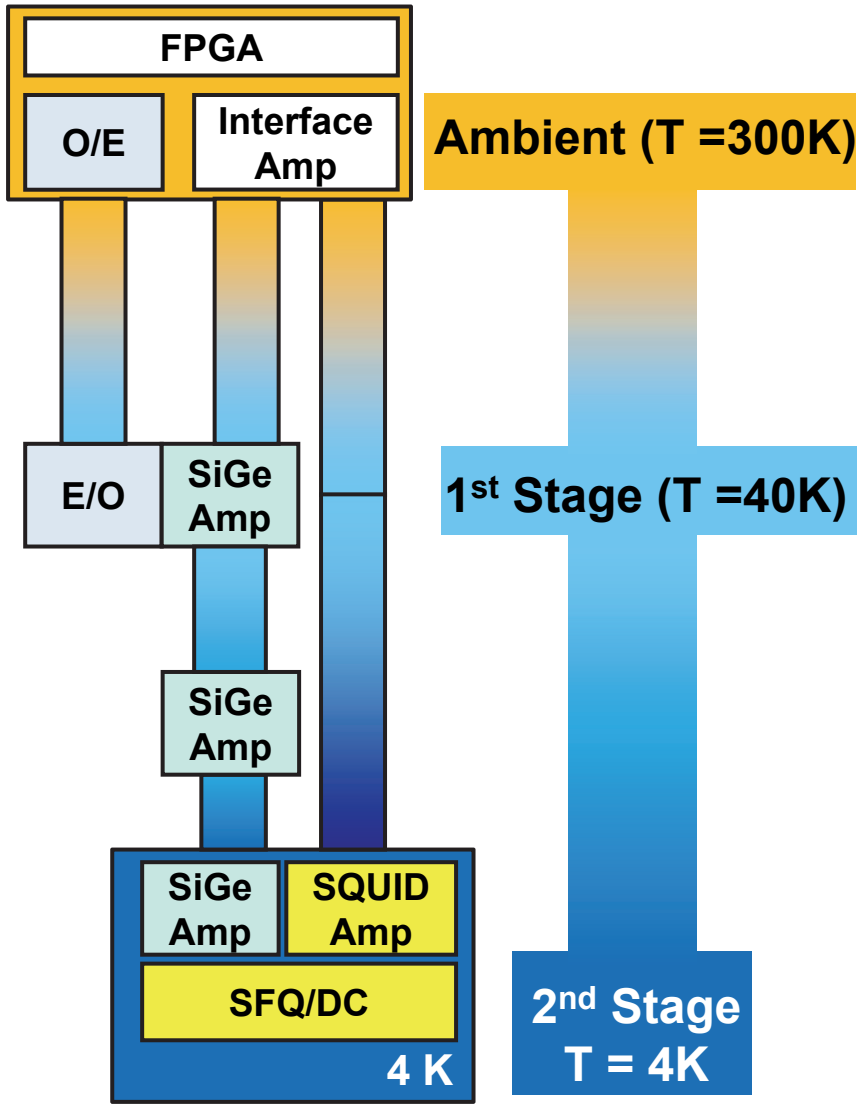
Digital Data Link from SCE to Room Temperature



- **Baseline: Current All-electrical Data link Chain**
  - **Drivers on superconductor IC**
  - **Transmission line from 4-300K**
  - **Semiconductor Amplifier**
  - **FPGA data receivers**



Faster Datalink – SCE IC to FPGA

Driver on superconductor IC

- Converts SFQ pulses to voltage
- SQUID based amplifier stages
- 3 - 5mV output amplitude
- >20 Gbps

Flexible transmission line

- Transfer signal from 4K to 300K
- 10 signal lines per cable assembly
- Heat load vs. bandwidth optimized for 10 Gbps

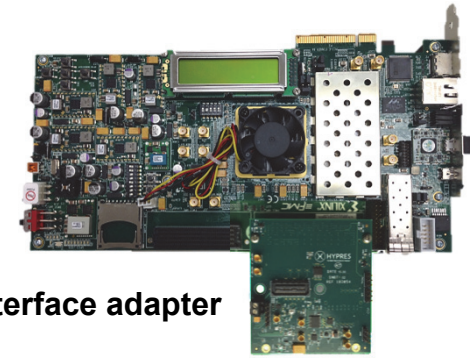
20 channel amplifier at 300K

- Custom multistage amplifier design
- >10 Gbps differential CML output

High-speed FPGA transceivers

- Using Xilinx GT* transceiver family
- Enables single links up to 32 Gbps
- >100 GT* available per FPGA chip

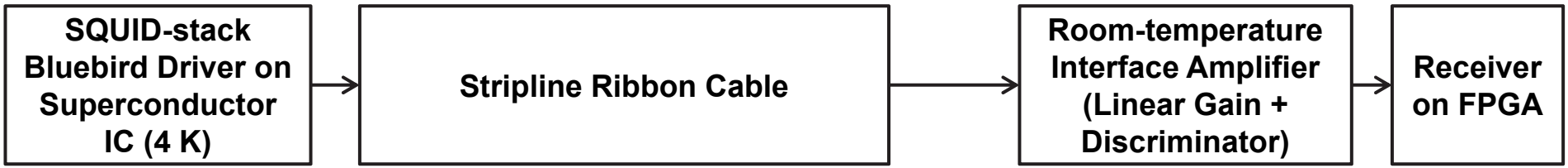
Xilinx FPGA Board



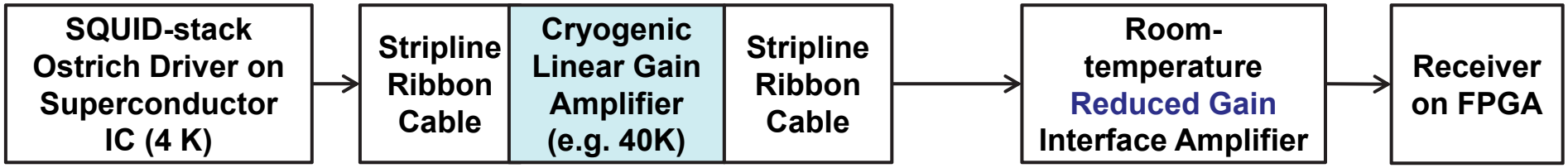
Custom Interface adapter

Example Data Link Configurations

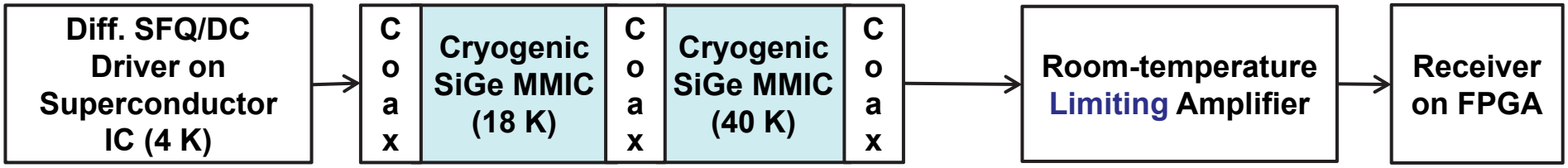
(1) 10 Gbps Data Link



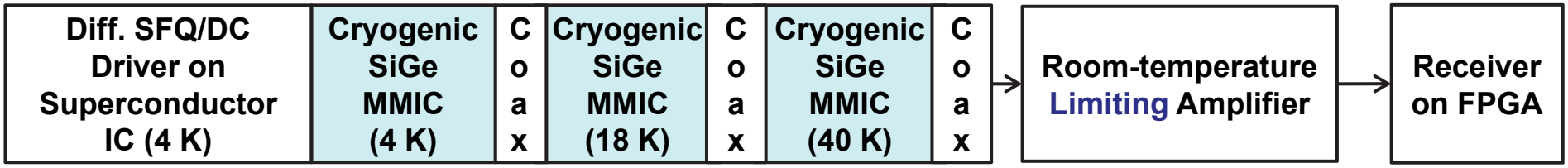
(2) 20 Gbps Data Link



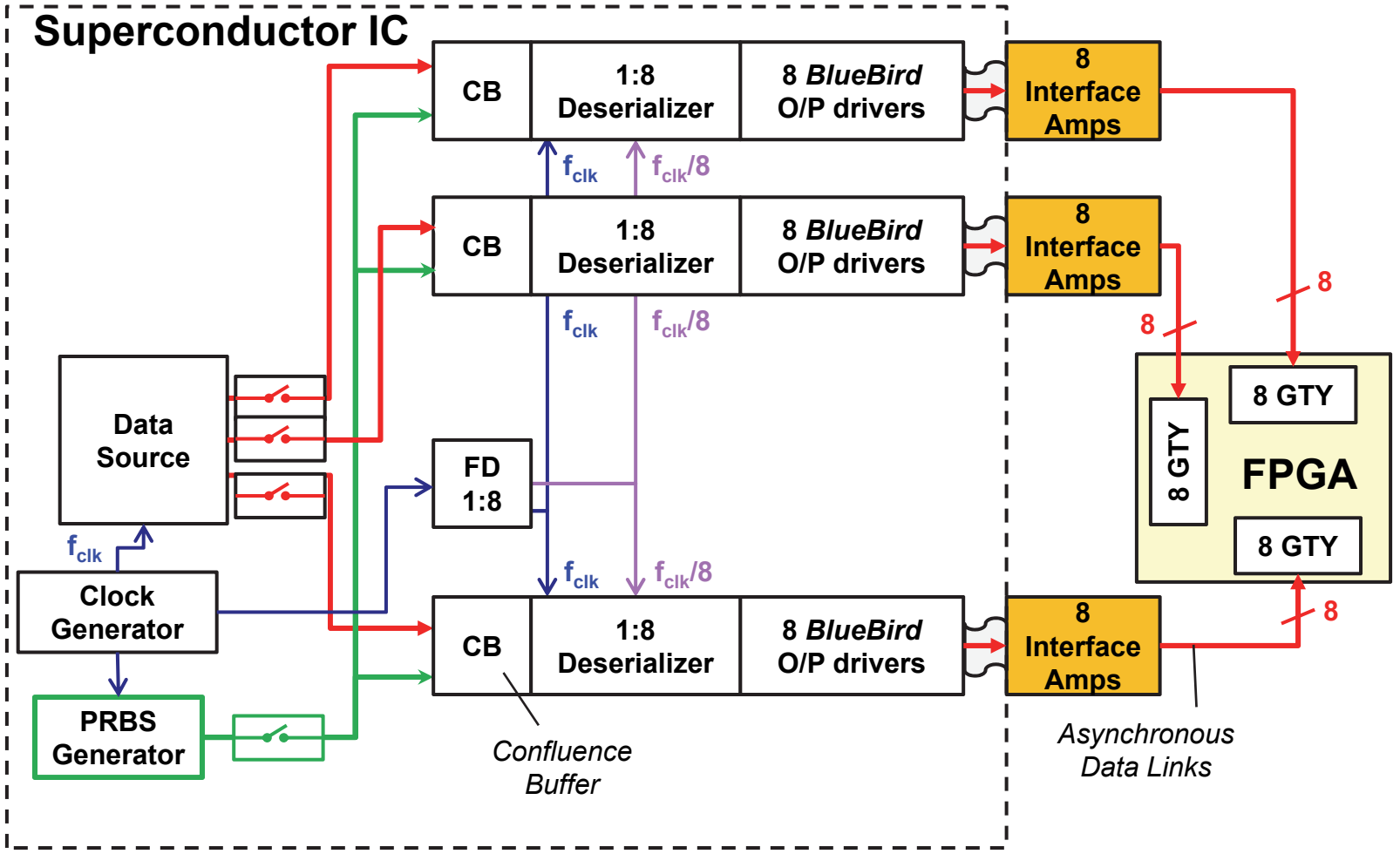
(3) 30 Gbps Data Link



(4) 30 Gbps Data Link



120 Gbps Data Transport from 4K to 300 K



Superconductor Output Driver for Digital Output Data Link

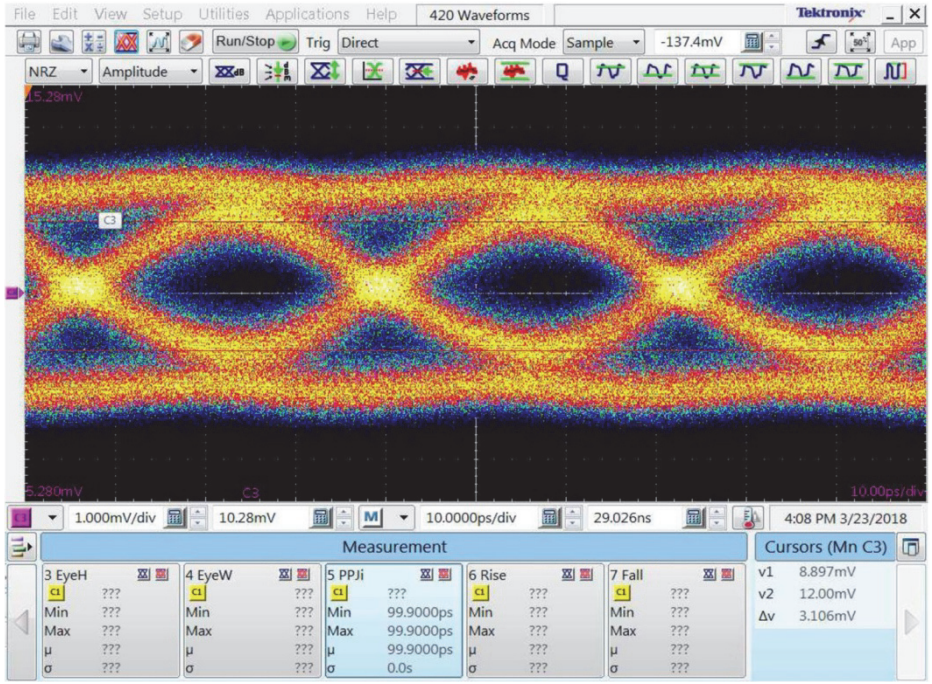
Comparison of Superconductor Output Drivers

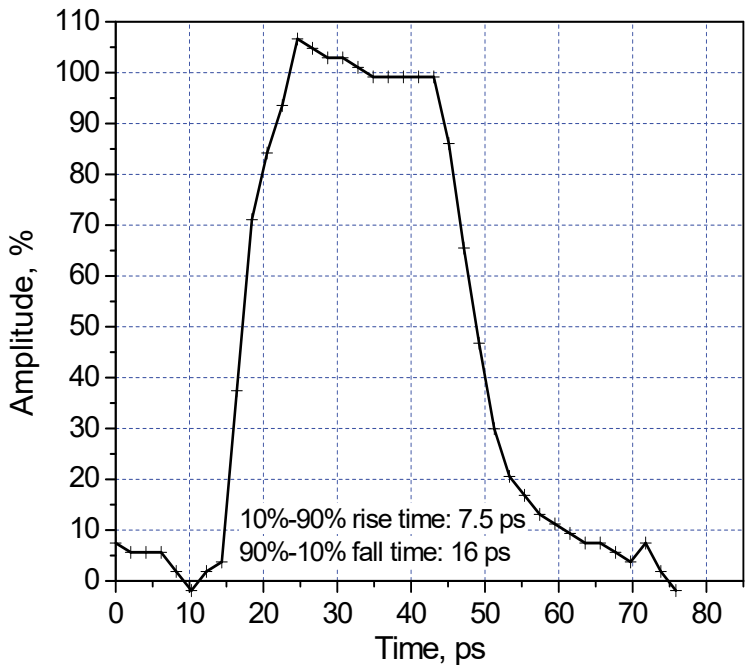
Output Drivers	Data rate (Gbps)	Swing @50Ω (mVpp)	Power (μW)	FOM (fJ/bit)	Area $(\mu m)^2$
SQUID-stack "Dodo"	6	5	99.0	16.5	22,800
SQUID-stack "Bluebird"	14	5	134.0	9.6	29,400
SQUID-stack "Ostrich"	30	5	157.6	5.3	63,800
Differential SFQ/DC	40*	1.3	13.4	0.3	12,000

***Projected. Differential SFQ/DC driver with cryogenic SiGe amplifier chain has been tested up to 22 Gbps.**

- **Bluebird is the most used**
  - **Ostrich is faster but takes >2x area and 17% more power**
  - **Dodo was made for lower power for slower data links**
- **SFQ/DC is fast but requires cryogenic amplification**

Ostrich Driver tested at 30 Gbps

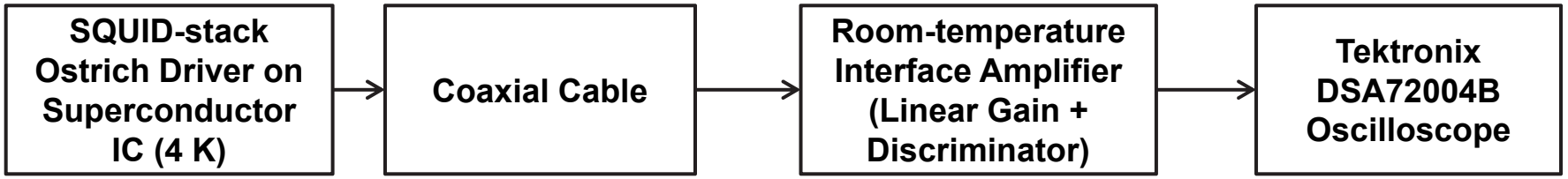


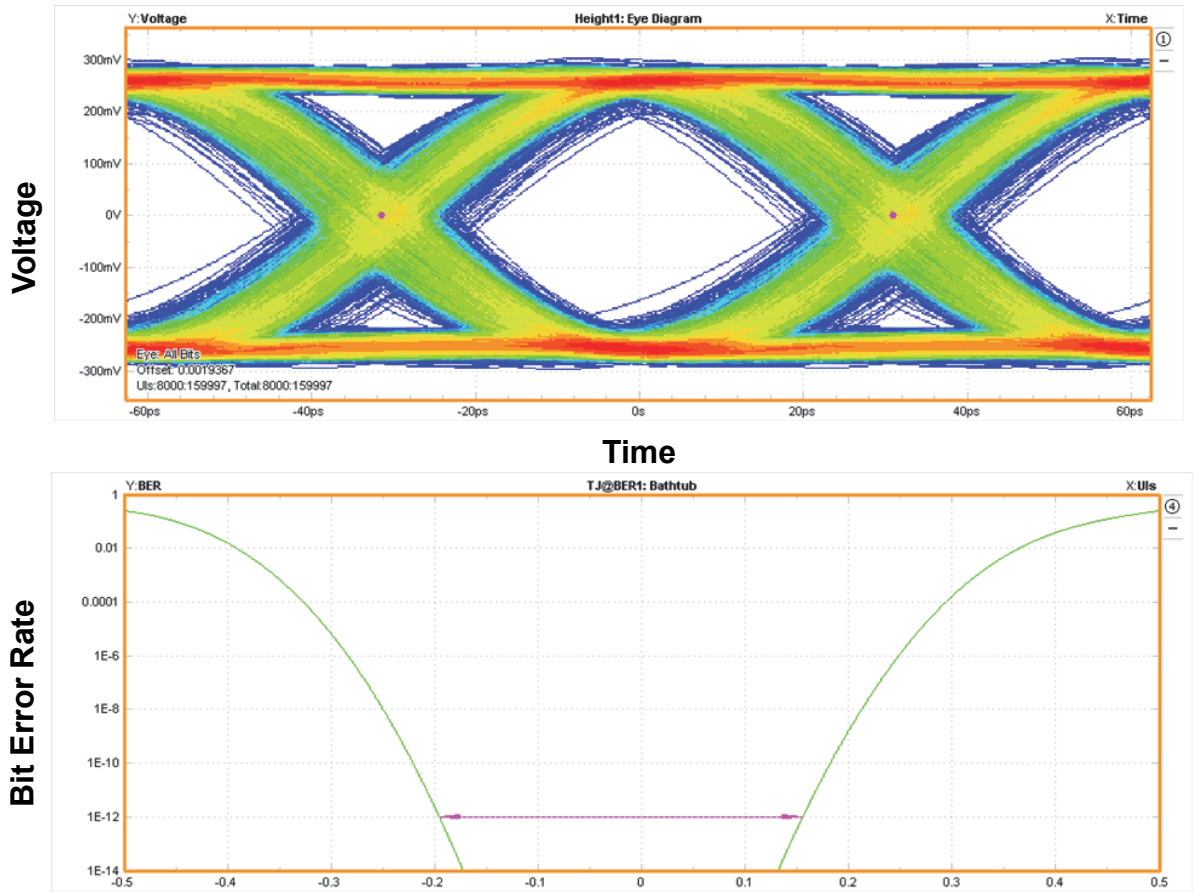


- **Direct measurement of Ostrich SQUID-stack driver at 30 Gbps using fast sampling module (80E09B) on Tektronix sampling oscilloscope**
  - **Measured without any amplifier in ICE-T insert at 3.7 K**

- **Direct measurement of Ostrich SQUID-stack driver at 30.48 Gbps using on-chip sampler**
  - **Measured in He immersion cryoprobe at 4.2 K**

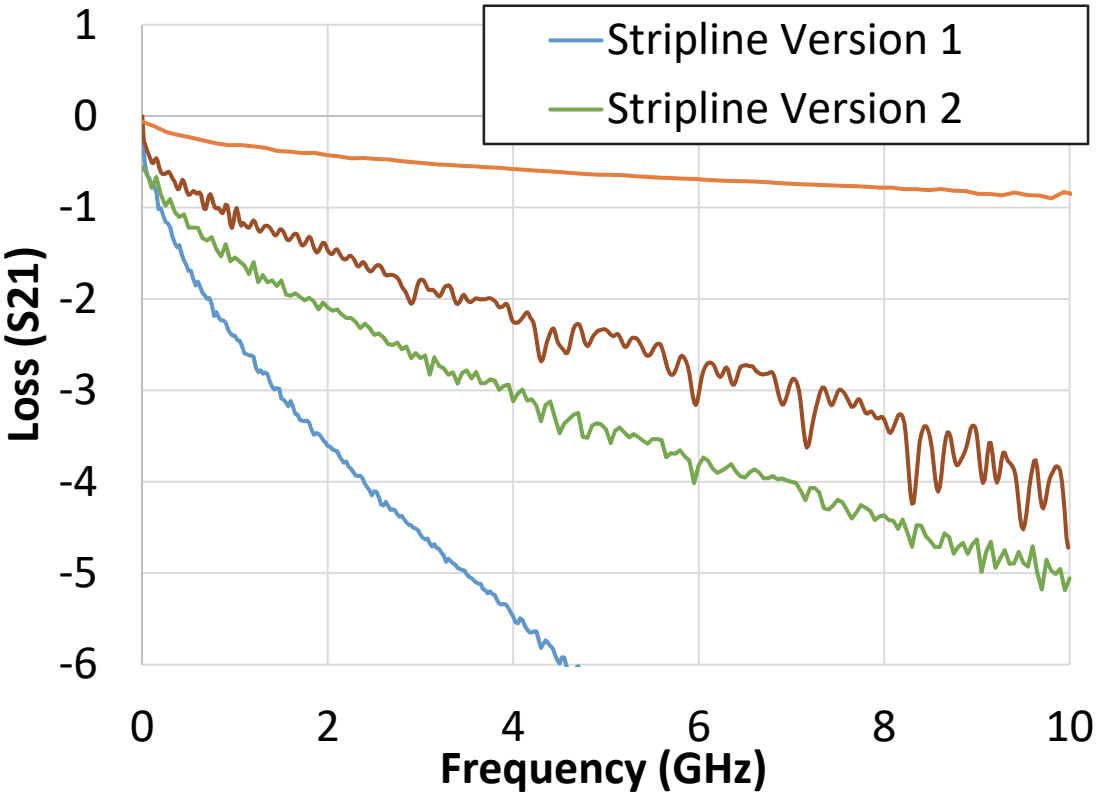
Data Link with Ostrich Driver at 16 Gbps

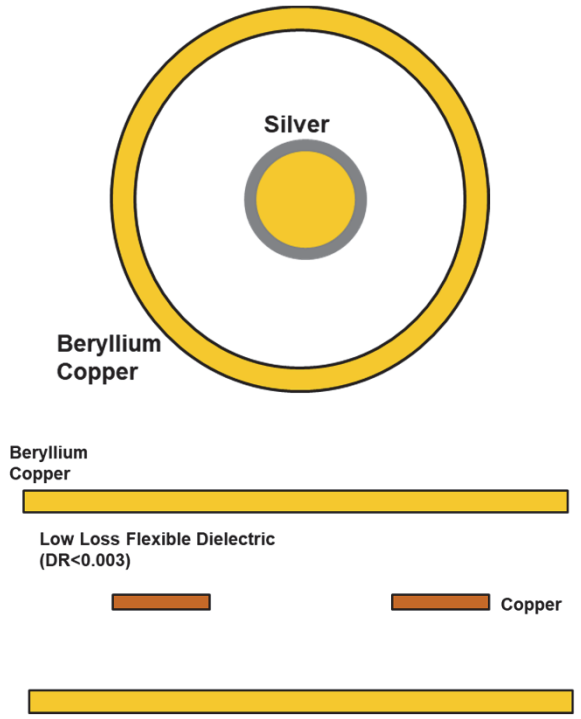




Electrical Transmission Line (Flexible Ribbon Cable) Development for Digital Output Data Link

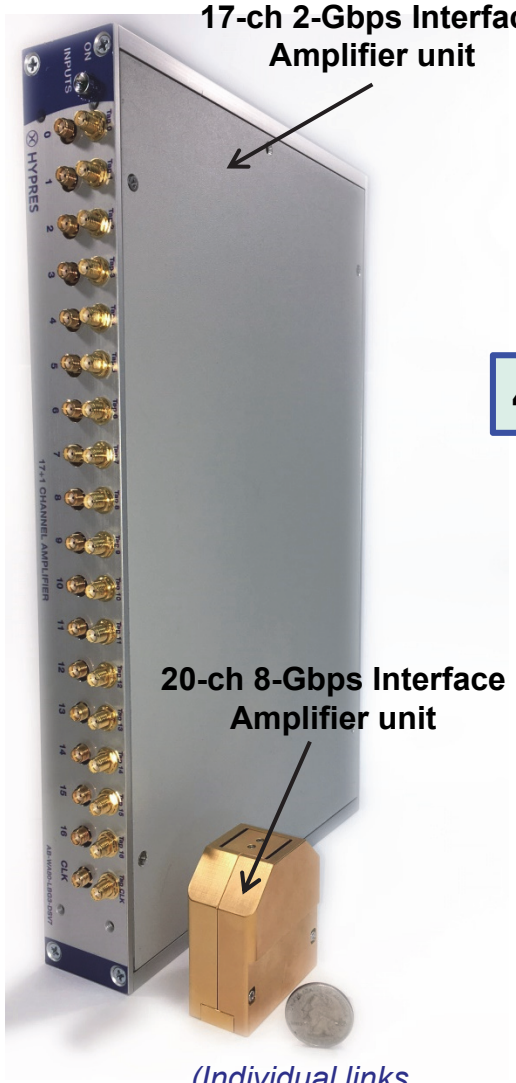
Transmission Line



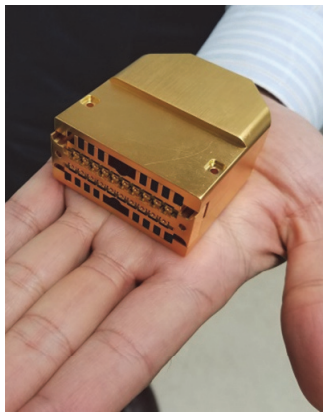


Transmission Line	3-dB BW (GHz)	Data Rate (Gbps)	4 K Heat load (µW)	FOM (fJ/bit)
Ag-coated BeCu Coax	30	42.9	2473	57.7
Stripline Version 1	1.5	2.1	440	205.3
Stripline Version 2	4	5.7	740	129.5
Stripline Version 3	7	10.0	1118	111.8

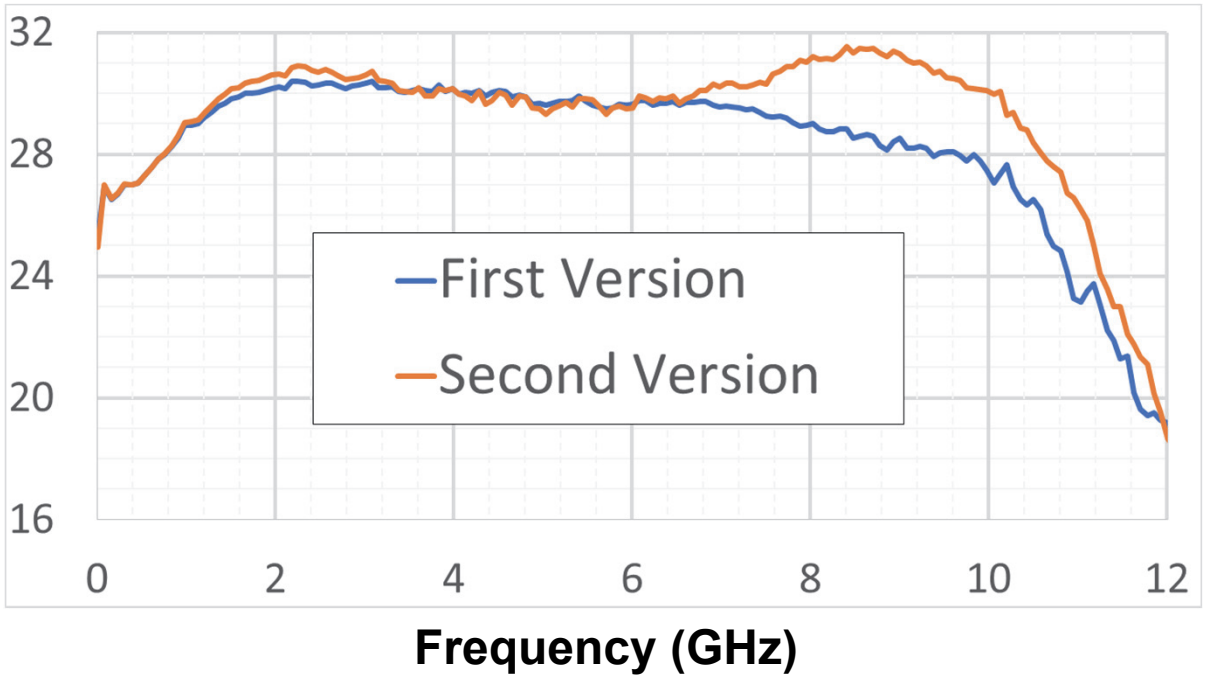
Semiconductor Interface Amplifier for Digital Output Data Link



(Individual links demonstrated up to 14 Gbps)

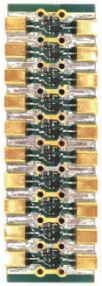


4 W, 2.18 in. × 1.19 in. ×2.3 in.

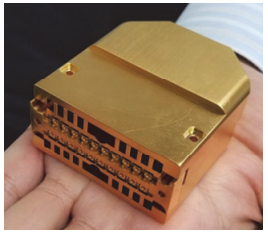


Cryogenic Amplification

Shorter ribbon cables



Shorter ribbon cables

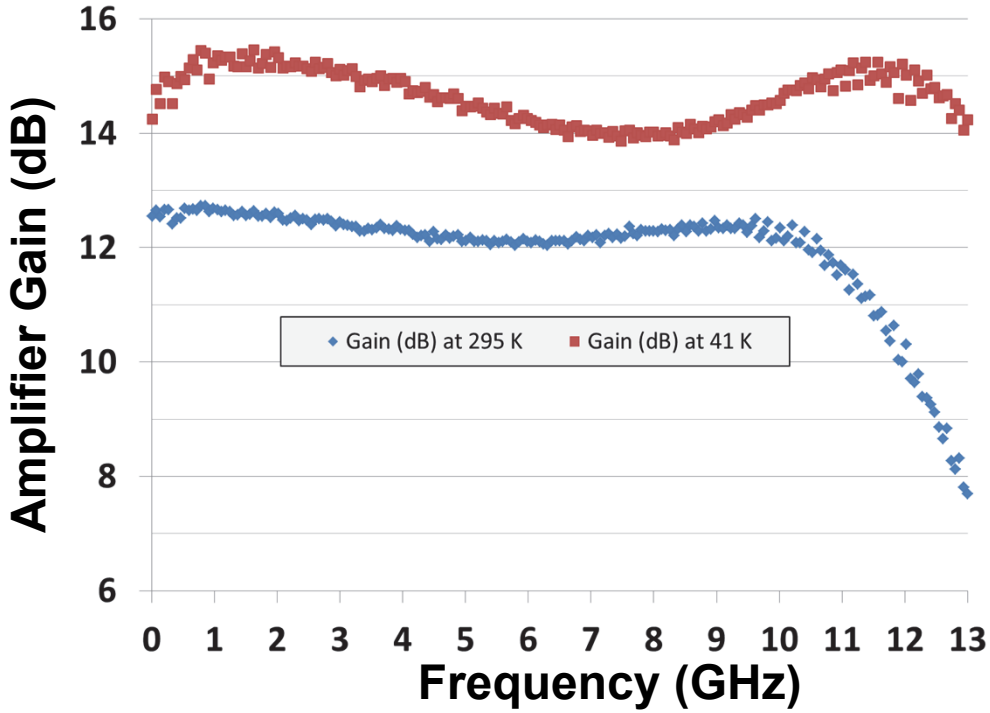


4 K

40 K

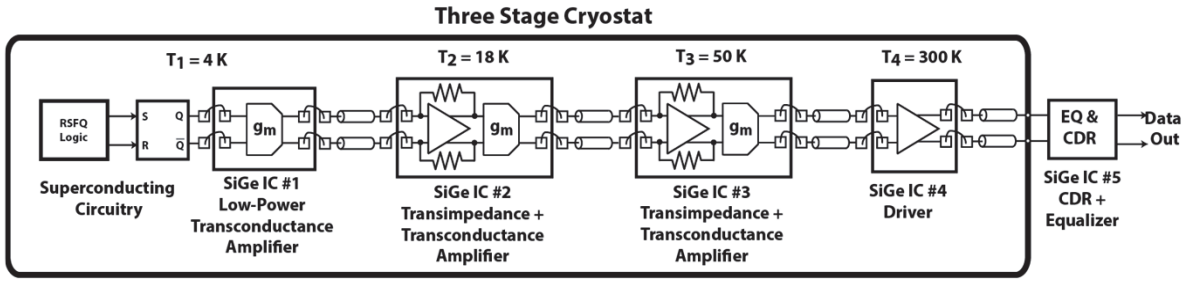
300 K

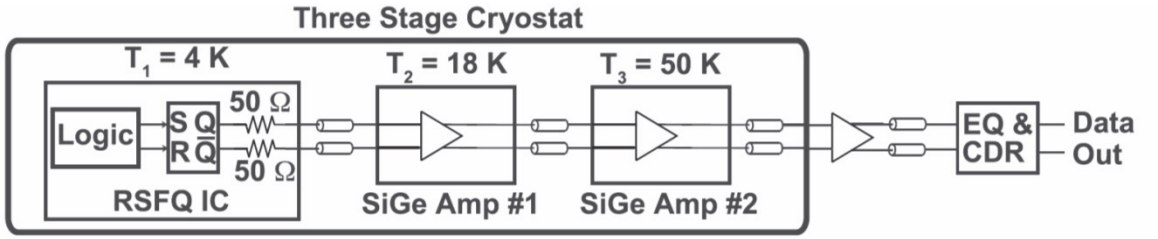
- **Cryogenic amplifier derived by cooling part of the room-temperature amplifier gain**
  - **Amplifier's gain and bandwidth improve at lower temperature**



HTHT Data Link with SiGe Amplifiers

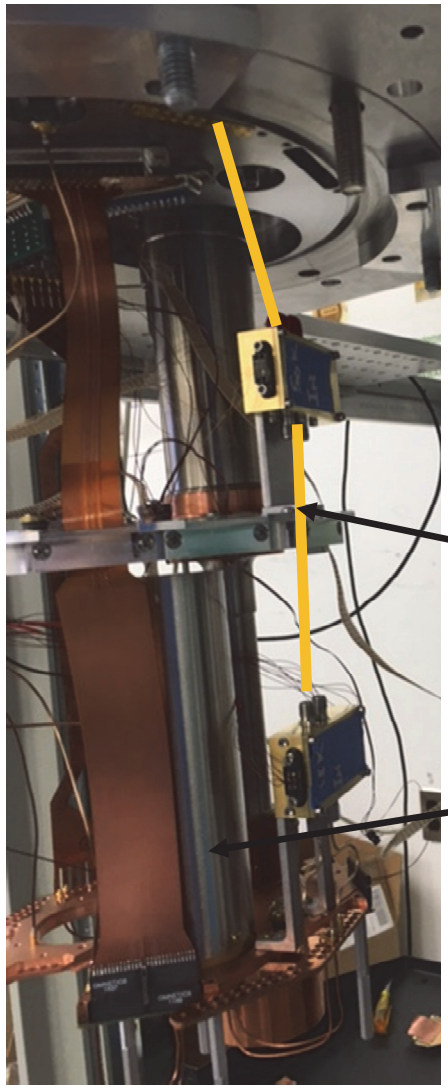
- **Concept: Distribute amplification (and corresponding power consumption) over the 4–300 K temperature range**
  - **Heterogeneous Technology: Nb JJs, SiGe HBT and Si CMOS**
- **Collaboration with UMass Amherst (Prof. Bardin)**
  - **Approach-1: Active Matching Circuit (Gain at 4 K with transistor)**
  - **Approach-2: Passive Matching Circuit (Loss at 4 K)**

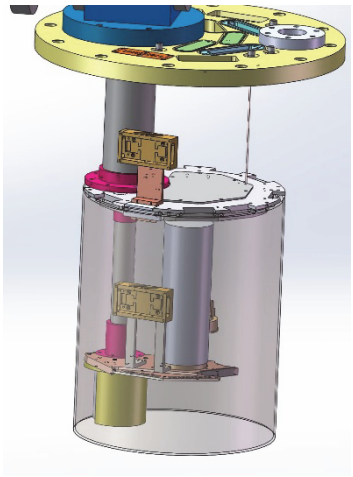


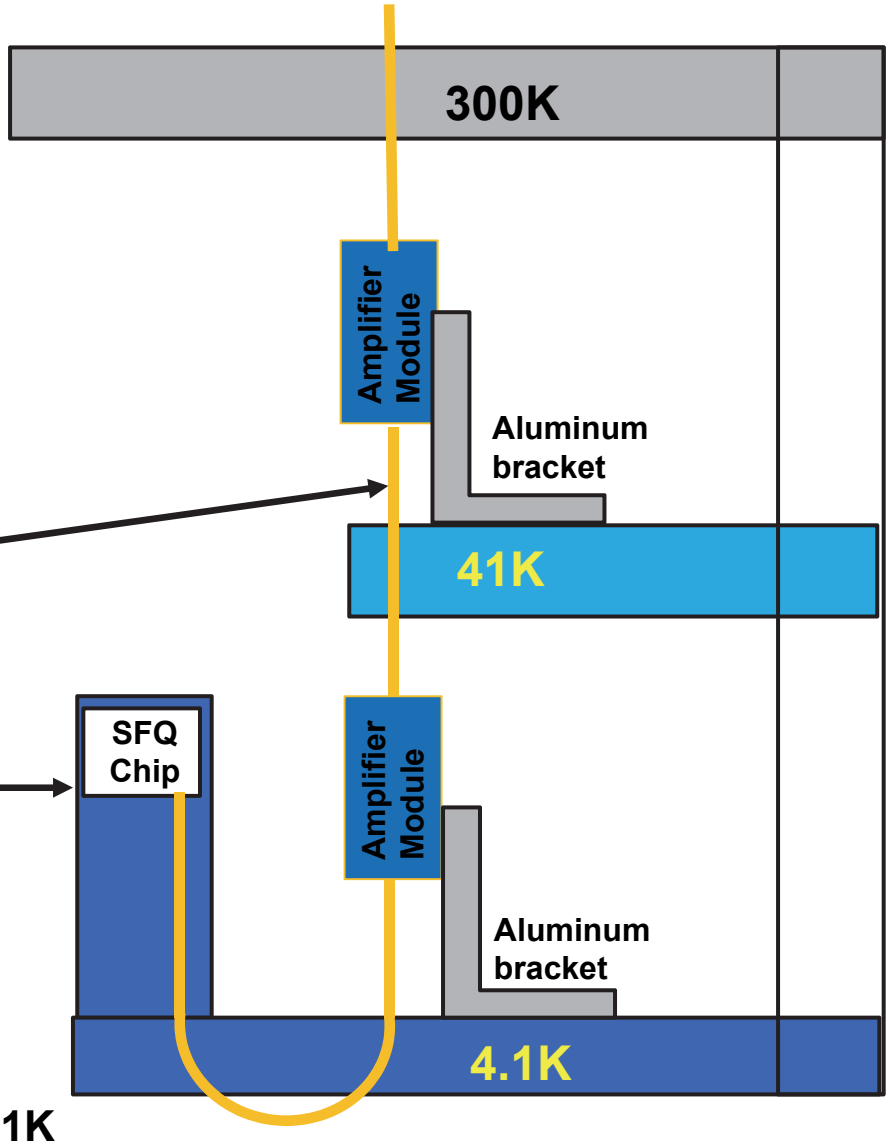


1) *D. Gupta, J. C. Bardin, et al., "Low-Power High-Speed Hybrid Temperature Heterogeneous Technology Digital Data Link," IEEE Trans. Appl. Supercond., vol. 23, no. 3, pp. 1701806, June 2013*
2) *Prasana Ravindran, Su-Wei Chang, et al., "Power-optimized Temperature-distributed Digital Data Link," IEEE Trans. Applied Superconductivity, vol. 25, no. 3, June 2015.*
3) *P. Ravindran, Su-Wei Chang, et al., "Energy Efficient Digital Data Link", IEEE Trans. Applied Superconductivity, December 2016*

Cryocooled Test Set-up for HTHT Links

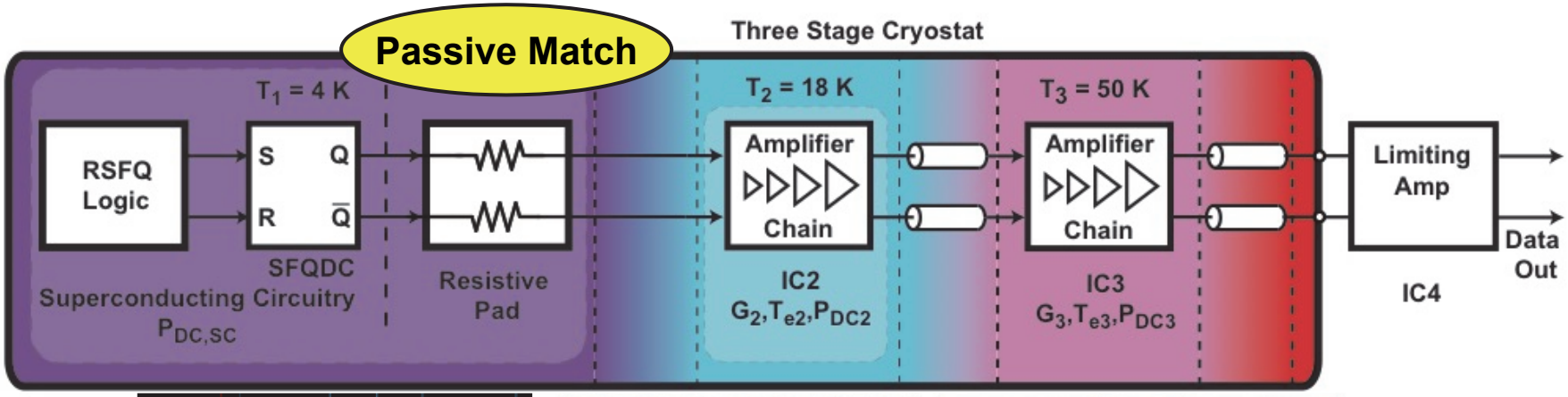


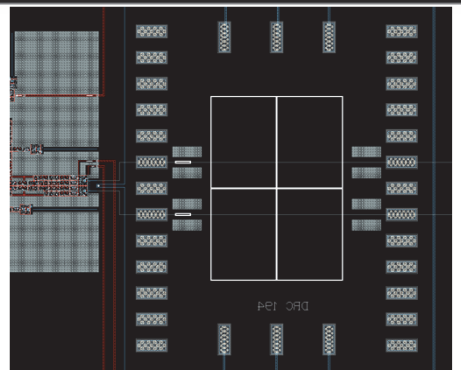


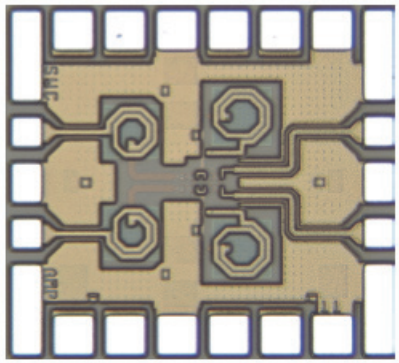


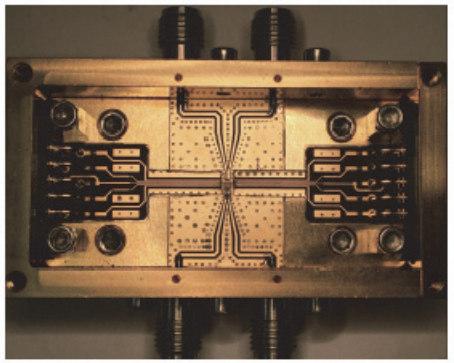
Cryomodule reaches a base temperature of 4.1K

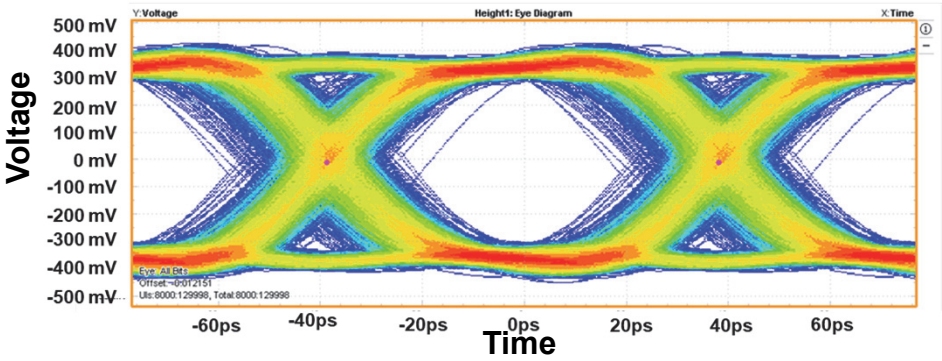
13 Gbps HTHT Link with 2-stage Cryo Amplifier

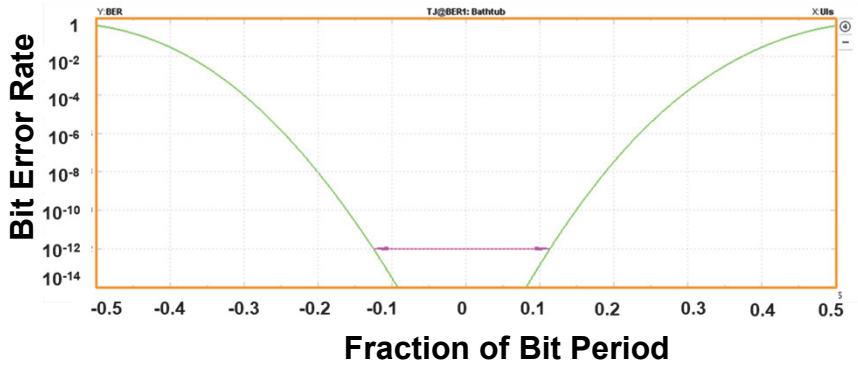




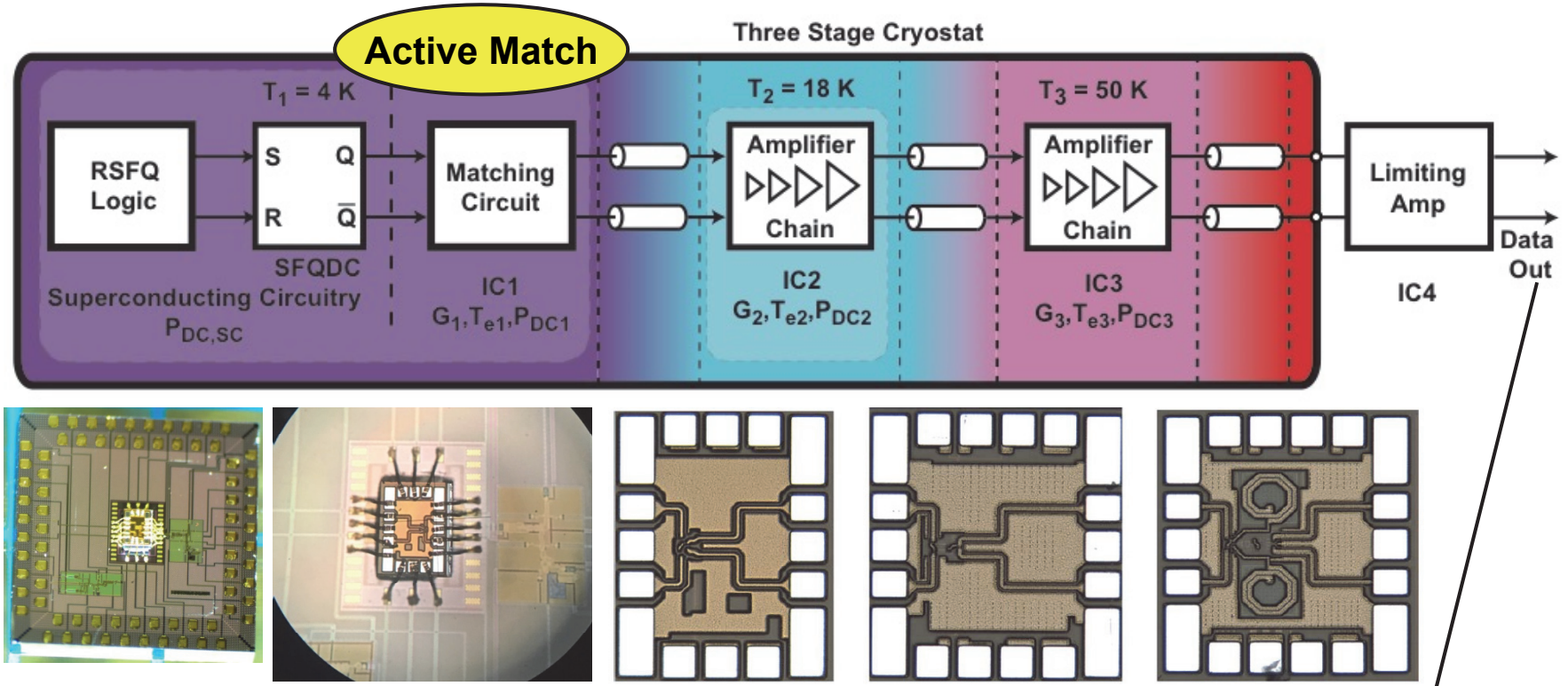


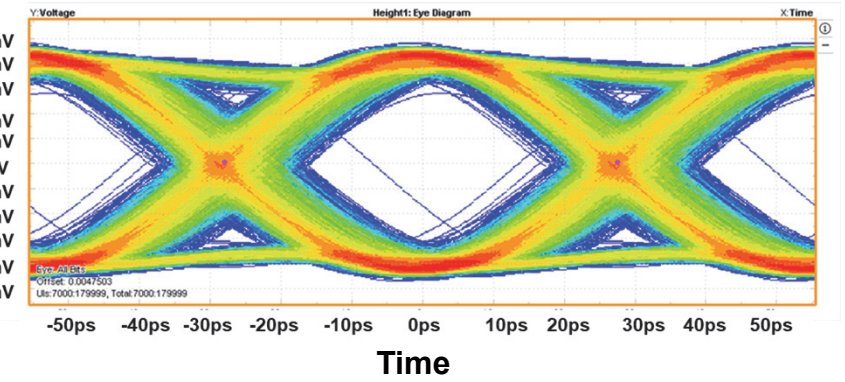


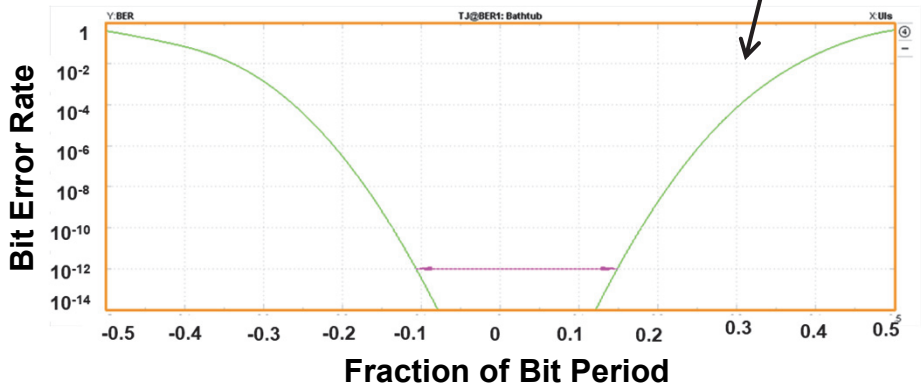




18 Gbps HTHT Link with 3-stage Cryo Amplifier







Performance Summary

Example	Data Rate (Gb/s)	4 K Power (mW)	18 K Power (mW)	40 K Power (mW)	300 K Power (mW)	
					Amplifier	Discriminator
RT	18				200	
Cryo-40 + RT	21			7.6	26.4	300
Cryo-18-40 + RT	30		6.3	6.3		300
Cryo-4-18-40 +RT	30	0.14	3.3	29.5		300

- **Hybrid-temperature Heterogeneous-technology (HTHT) design approach**
  - **Step-1: Cool part of the room-temperature interface amplifier to enhance bandwidth**
  - **Step-2: SiGe custom amplifier chain with ("active match") and without ("passive match") a 4 K stage**

FPGA Receivers for Digital Output Data Link

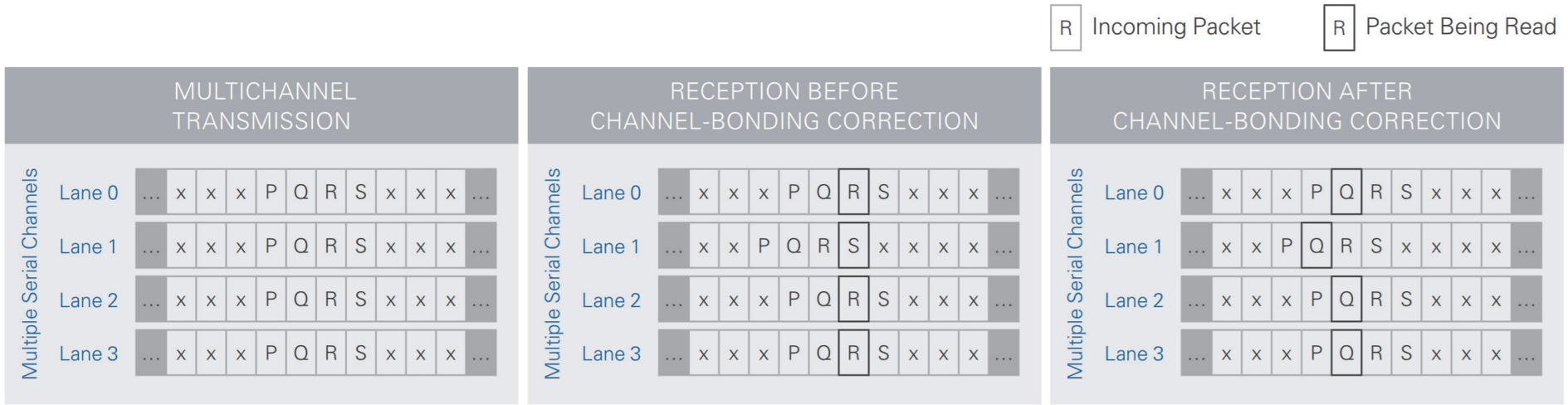
Datalink – Channel Bonding

Introduction

- Required data throughput exceeds single lane, multiple lanes are used
- At high rates propagation delays cause the data to arrive at different times to each receiving lane
- Aligning the data across all lanes at the receiver is needed, a process known as *channel bonding*

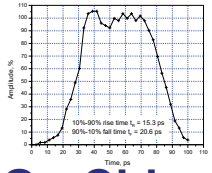
Channel bonding for SFQ

- Encoding schemes like 8b/10b or 64b/66b are difficult to implement in RSFQ and large in size
- Common data source (e.g. PRBS) on all output lanes can be used instead
- Same sequence can be found in each receivers elastic buffer at offset
- Read pointers are adjusted to offset of the same sequence location

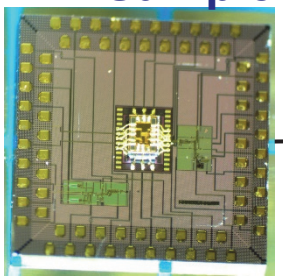


A.E. Lehmann, et al., "Embedded RSFQ pseudo-random binary sequence generator for multi-channel high-speed digital data link testing and synchronization," IEEE Trans. Appl. Supercond., vol. 27. no. 4, Art. no. 1301806, June 2017.

Signal Path

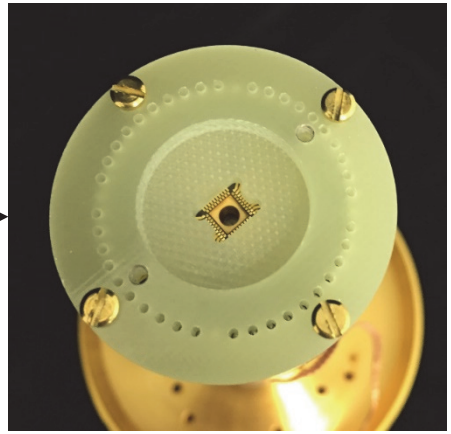


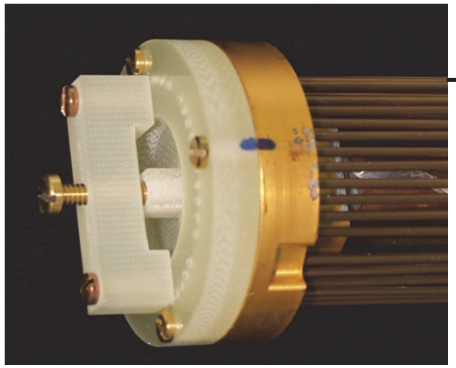
On Chip Sampler



SFQ chip

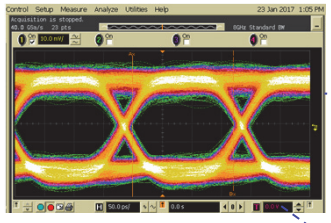
Chip Nest





Coax or Stripline

Before Amp



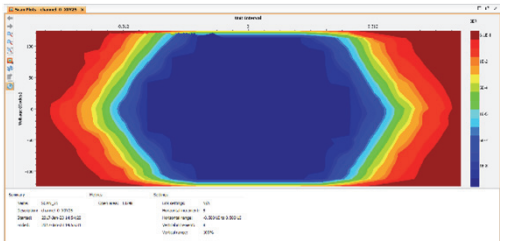
Amplifier

After Amp but before logic

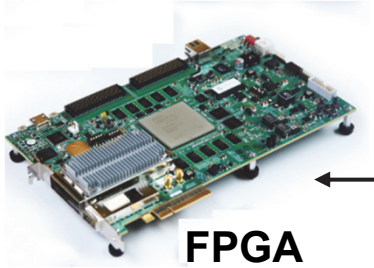
Limiting Amplifier

After Limiting Amplifier/Comparator

CML

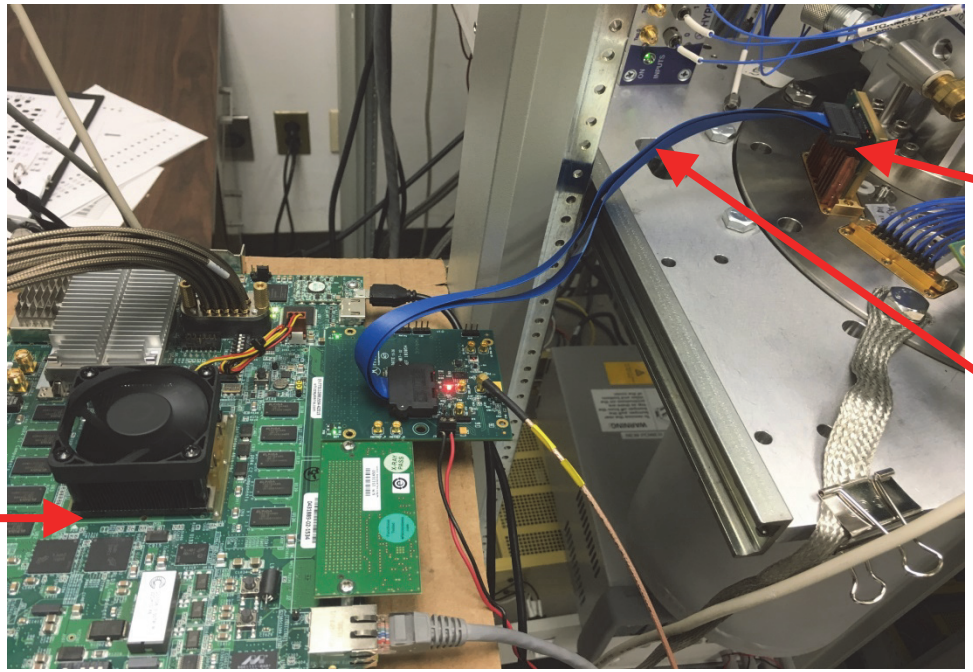


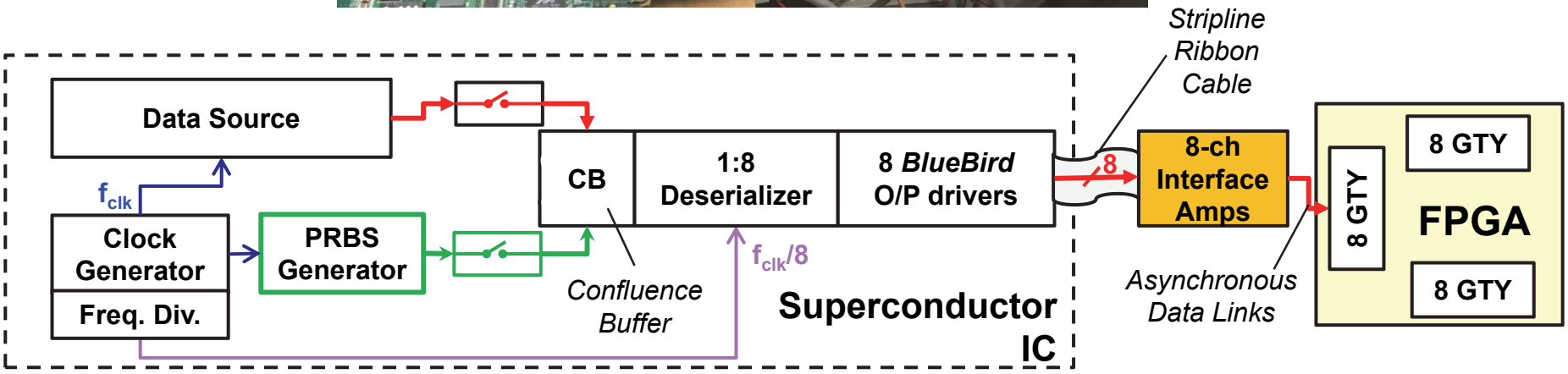
Eye Scan
Bit Error Rate



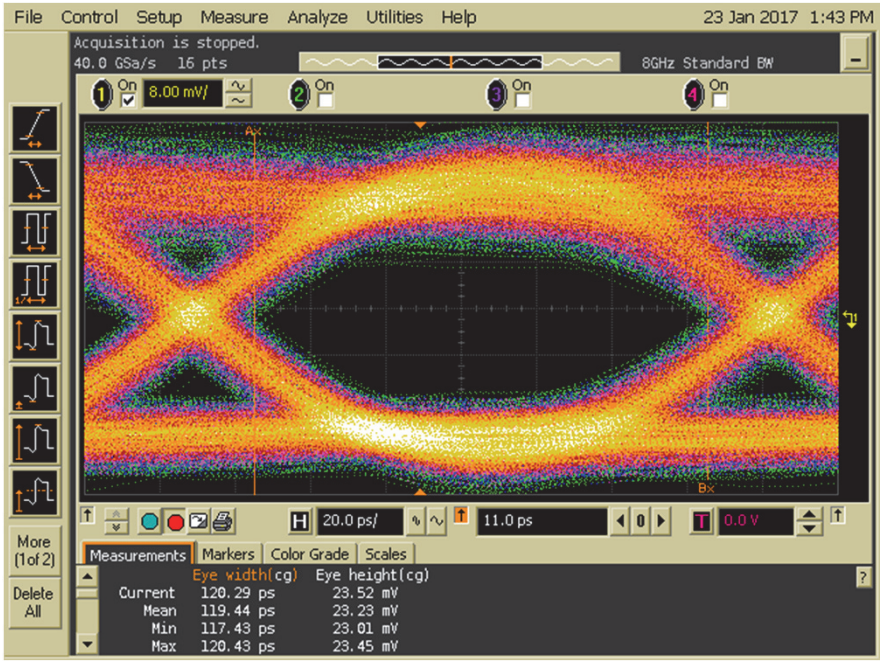
FPGA

64 Gbps Data Transport: 8 channels × 8 Gbps/ch

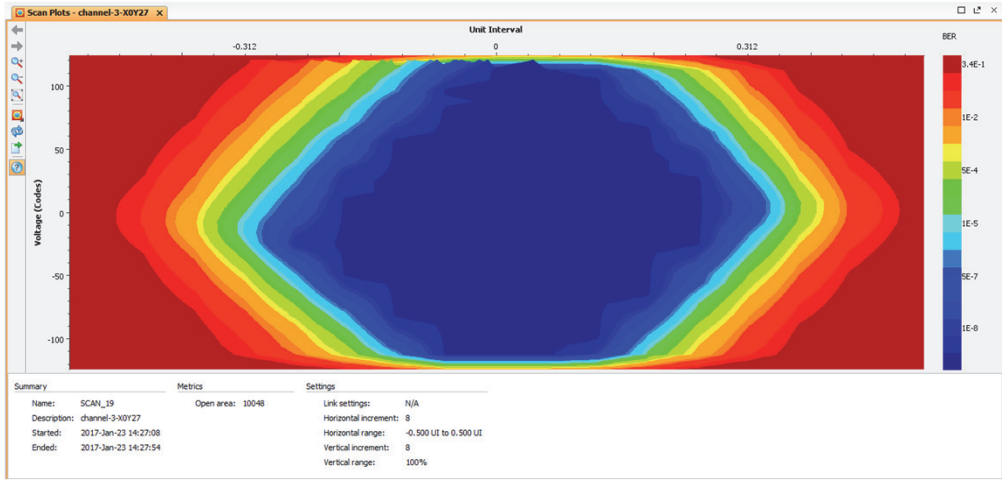




Eye Diagram: 6.5 Gbps Data Link



Eye after 2 stages of amplification

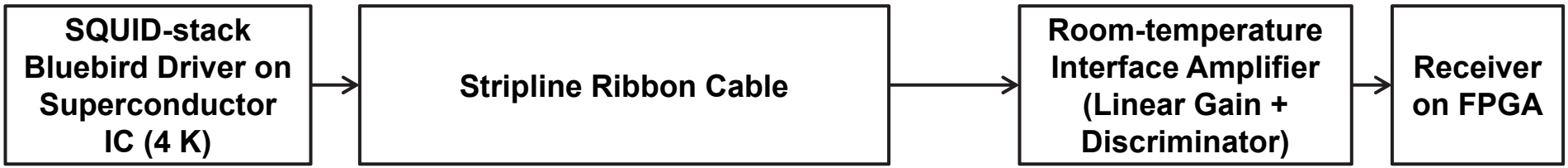


After two stages of amplification and discrimination to CML logic as interpreted by the FPGA

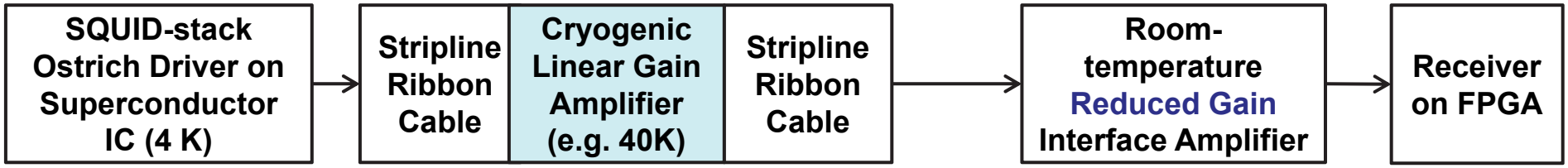
- 52 GSps data generated on superconductor IC, deserialized by a factor of 8
- Acquired by Xilinx UltraScale FPGA
- Superconductor IC in cryocooled testbed

Example Data Link Configurations

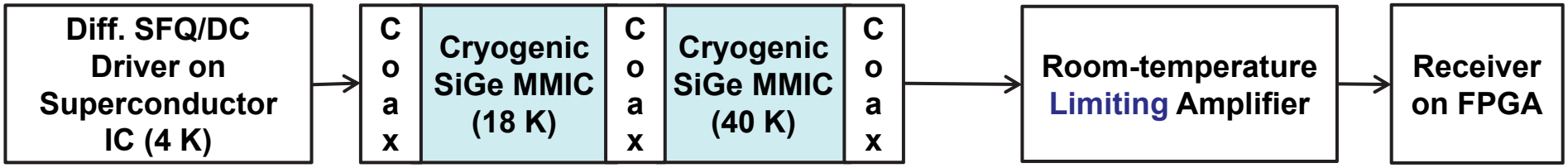
(1) 10 Gbps Data Link



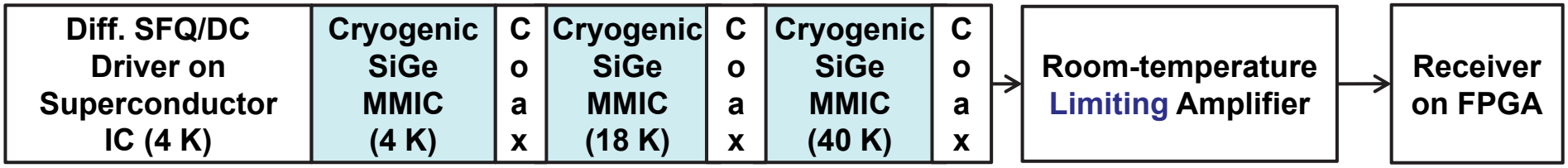
(2) 20 Gbps Data Link



(3) 30 Gbps Data Link



(4) 30 Gbps Data Link



Why we need "SuperCables"

Example	Data Rate (Gb/s)	4K Heat Load (mW)			18K Heat Load (mW)			40K Heat Load (mW)		
		TL	Amp	**Total**	TL	Amp	**Total**	TL	Amp	**Total**
1	10	1.12	0.134	**1.25**				13.0		**13.0**
2	20	1.12	0.158	**1.28**				13.0	7.6	**20.6**
3	30	4.74	0.013	**4.75**	12.8	6.3	**19.1**	149.0	6.3	**155.3**
4	30	4.74	0.153	**4.89**	12.8	3.3	**16.1**	149.0	29.5	**178.5**

- **Metallic transmission lines dominate heat loads**
- **Optical fibers offer little heat load and are immune to EMI**
  - **Power for E/O and O/E conversion needs be included calculation**

Complete Data Link Figure-of-Merit

Example	Data Rate (Gb/s)	4K Heat Load × 500 (mW)	18K Heat Load × 100 (mW)	40K Heat Load × 40 (mW)	300K Heat Load (mW)		Total Equivalent Heat Load at 300 K (W)	FOM (pJ/bit) at 300 K
					Amp	GTY		
1	10	626	0	520	200	242	1.346	135
2	20	638	0	824	305	337	1.767	88
3	30	2377	1910	6212	300	452	10.799	360
4	30	2447	1610	7140	300	452	11.497	383

- **Heat loads at different stages are converted to equivalent room-temperature power consumption representing large cryocoolers**
  - **4K: 500 W/W, 18 K: 100 W/W, 40 K: 40 W/W**

Conclusions

- Complete SFQ-to-FPGA data links at 6-10 Gbps/channel now routinely used for superconductor digital circuits
  - Single links with no cryogenic amplification work up to 16 Gbps
  - Multiple parallel links work up to 8 Gbps/channel
  - Transport rate up to 120 Gbps demonstrated, limited by data source on superconductor IC not data link
- Established framework for data link design with examples of 10, 20, and 30 Gbps/channel configurations
  - Superconductor drivers up to 30 Gbps are available
  - FPGA-based receivers up to 30 Gbps are available
  - Coaxial lines support high rates but conduct excessive heat, whereas metallic striplines have attenuation and crosstalk
  - Cryogenic amplification helps increase data rate
  - Current electrical links can support small-scale systems in the short-term with some refinements in cryopackaging
- Improvement in transmission media (e.g. hybrid E/O, superconductor lines) necessary, especially for larger systems