

# 30-GHz Operation of Datapath for Bit-Parallel, Gate-Level-Pipelined Rapid Single-Flux-Quantum Microprocessors

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## Acknowledgment

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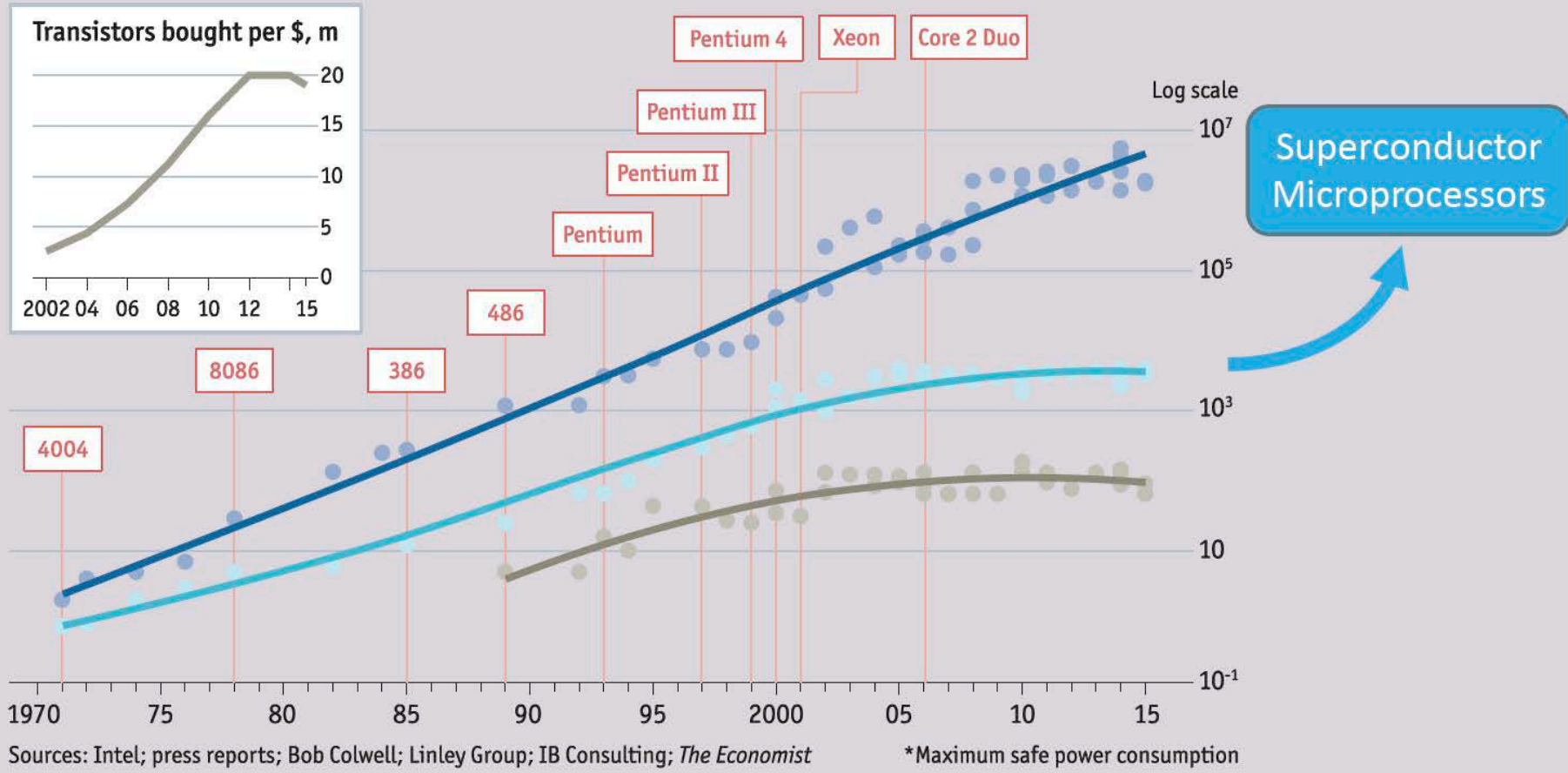
# Outline

- Background
- Co-design in device/circuit/architecture levels toward throughput-oriented microprocessors
- Demonstration of datapath and design of microprocessor prototype
- Summary

# Moore's Law

## Stuttering

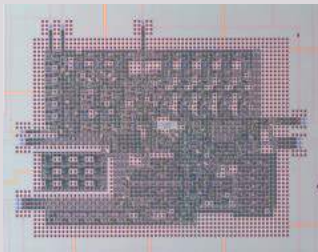
● Transistors per chip, '000   ● Clock speed (max), MHz   ● Thermal design power\*, w   □ Chip introduction dates, selected



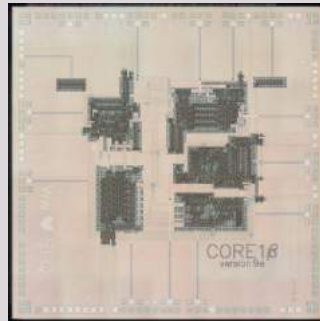
"Technology Quarterly: After Moore's Law," *Economist* (2016)

# RSFQ Microprocessor Projects

- FLUX-1: SUNY Stony Brook, TRW, and JPL
- CORE: Nagoya U., Yokohama National U., Kyoto U.

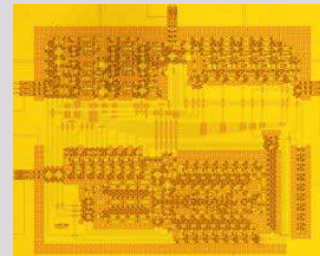


**CORE1 $\alpha$  (2003)**  
4999 JJs, 15 GHz  
167 MIPS, 1.6 mW



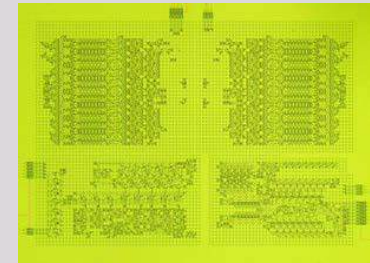
**CORE1 $\beta$  (2006)**  
10955 JJs, 25 GHz  
1400 MOPS, 3.3 mW

Pipeline  
processing



**CORE100 (2015)**  
3073 JJs, 100 GHz  
800 MIPS, 1.0 mW

Ultra high-  
frequency



**CORE e2 v5h (2016)**  
10603 JJs, 50 GHz  
333 MIPS, 2.5 mW

Stored-program  
computing demo

# Program Execution with 50-GHz Clock

IM		DM	
00:	LD 00	00:	X: input
01:	MV	01:	Y: result
02:	DEC	02:	
03:	ST 01	03:	
04:	LD 00	04:	
05:	MV	05:	
06:	LD 01	06:	
07:	SUB	07:	
08:	SKNE	08:	
09:	HLT	09:	
0a:	SKLT	0a:	
0b:	JMP 07	0b:	
0c:	LD 01	0c:	
0d:	JMP 01	0d:	
0e:		0e:	
0f:		0f:	

Input

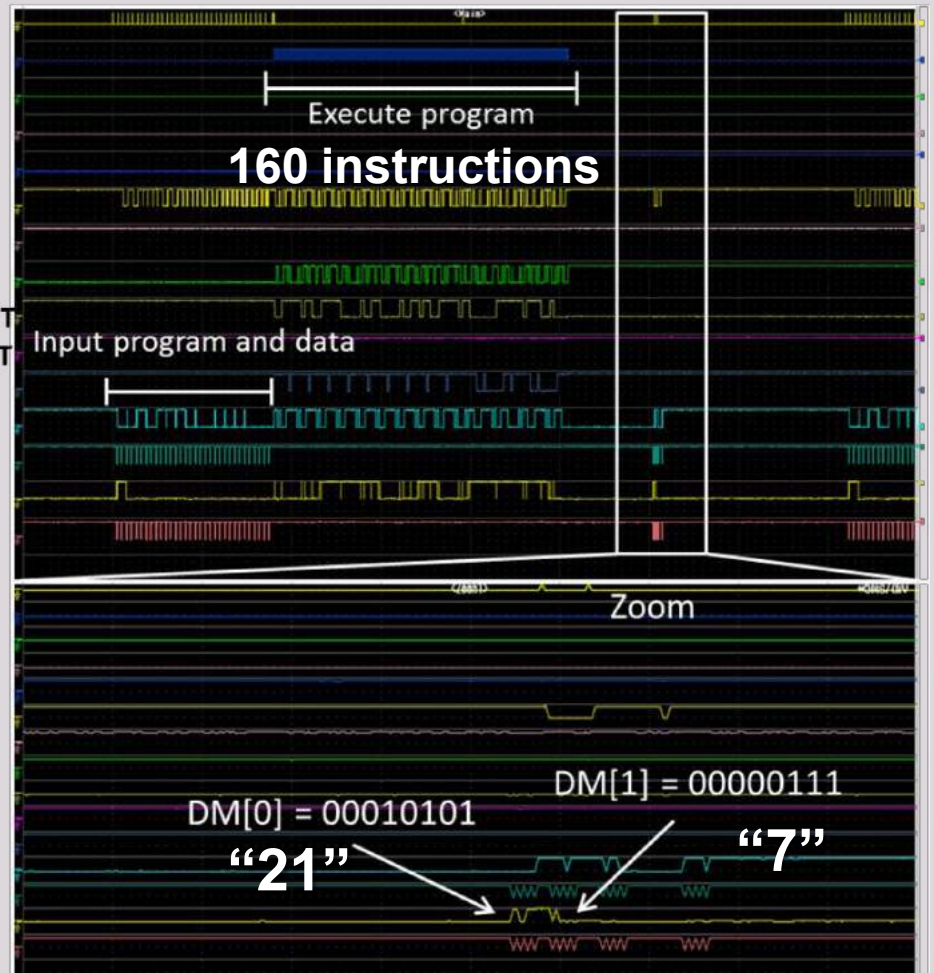
- INIT
- SYS\_LF
- IR\_DIN
- IR\_CIN
- HLT\_TRG
- PC\_ADDR
- LF

output

- ALU\_OUT
- REG1\_DOUT
- REG1\_COUT
- TAKEN
- IM\_DOUT
- IM\_COUT
- DM\_DOUT
- DM\_COUT

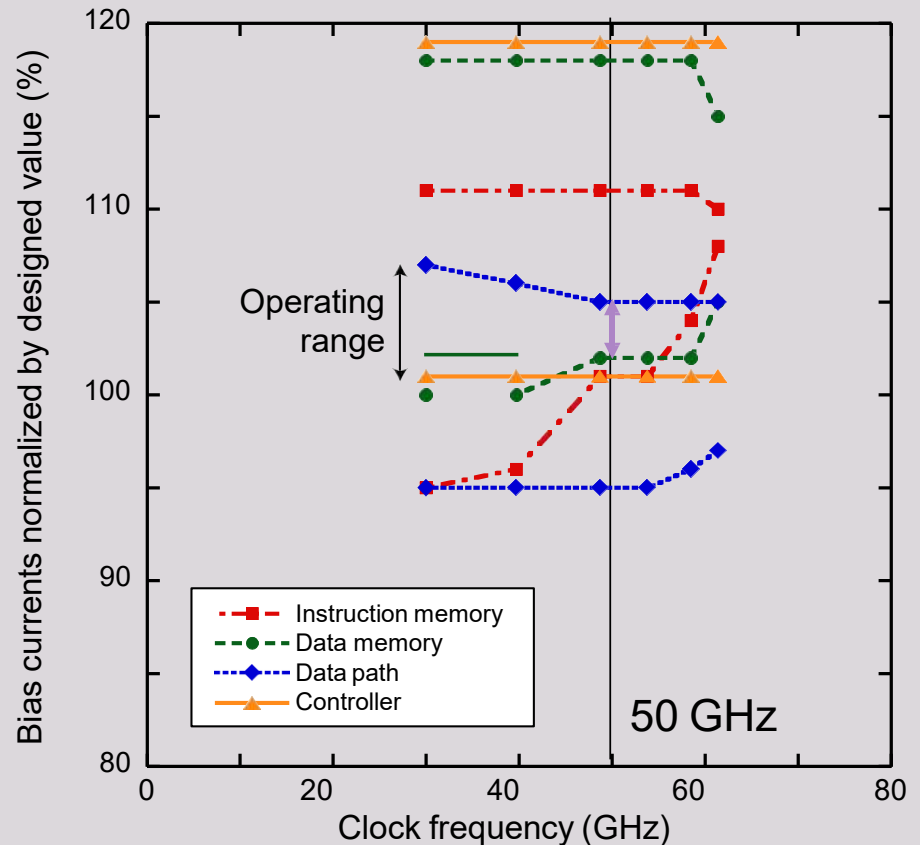
Double loops

Find the greatest divisor of X (X = 21)



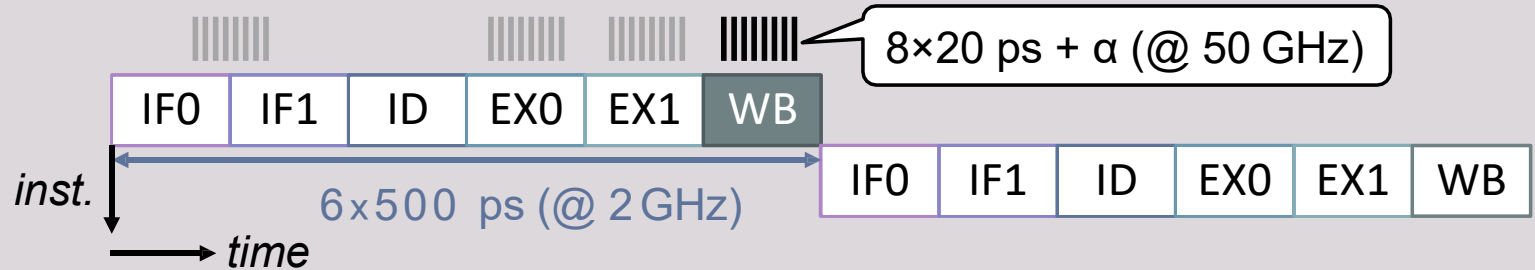
# Demonstration of Stored-Program Computing with CORE e2

- Successfully executed several test programs
  - Small-scale programs written within 16 lines
    - ✓ Calculate  $1 + 2 + \dots + N$
    - ✓ Calculate sum of an array
    - ✓ Integer division
    - ✓ Find the greatest divisor
    - ✓ Euclidean algorithm (GCD)



# Expected Maximum Performance in Bit-Serial Processing (8-bit)

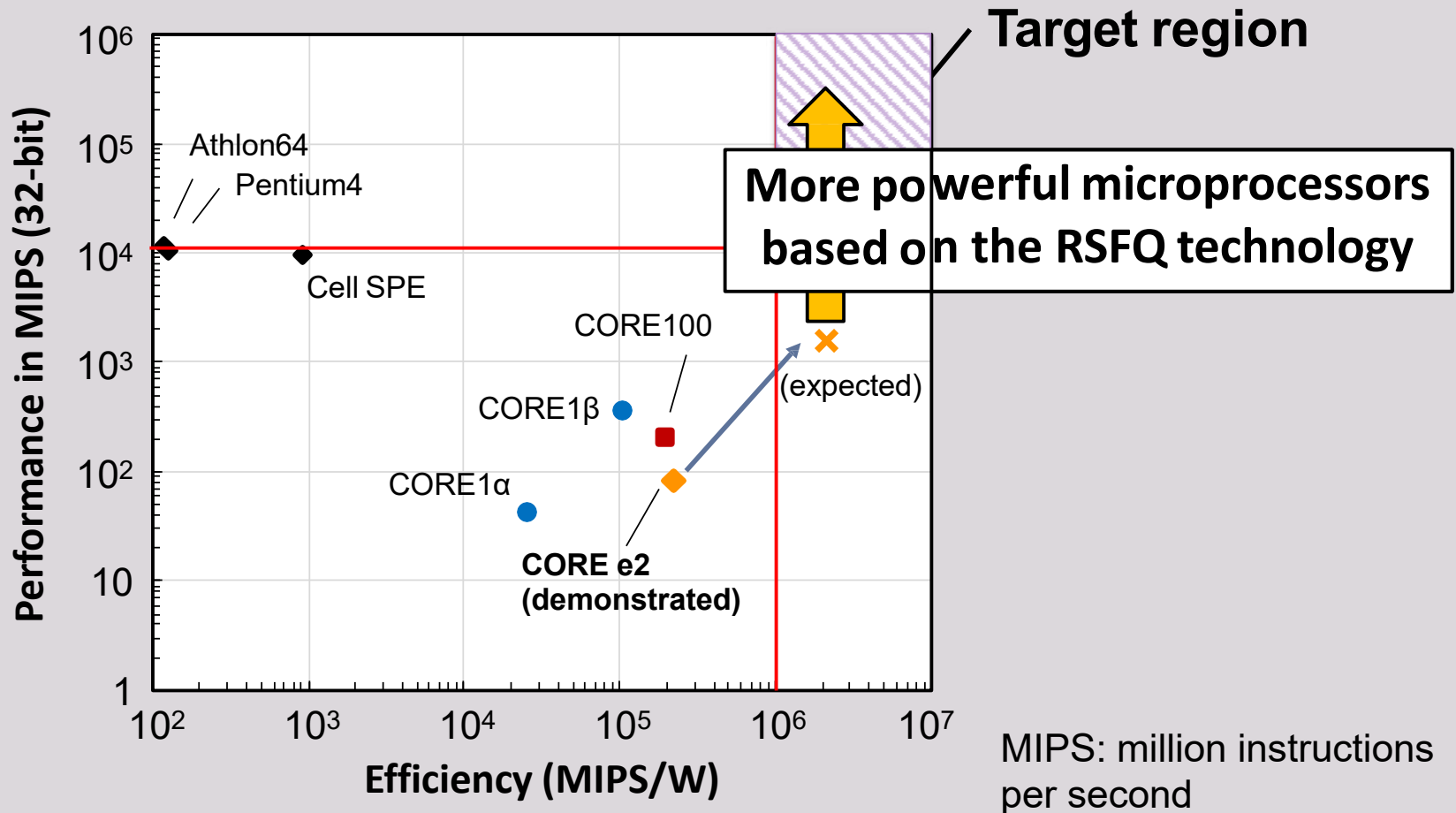
- CORE e2: 333 million-instructions/s (MIPS)



- Pipelining execution: up to 6250 MIPS (ideal case)



# Purpose of This Study



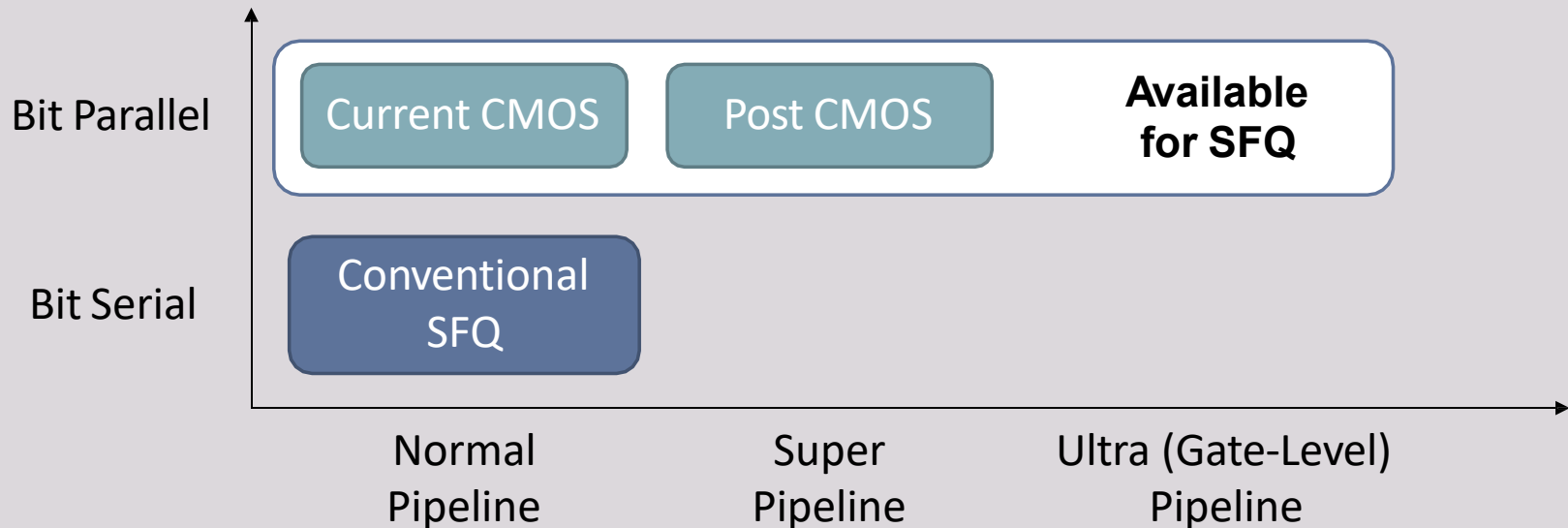


# Outline

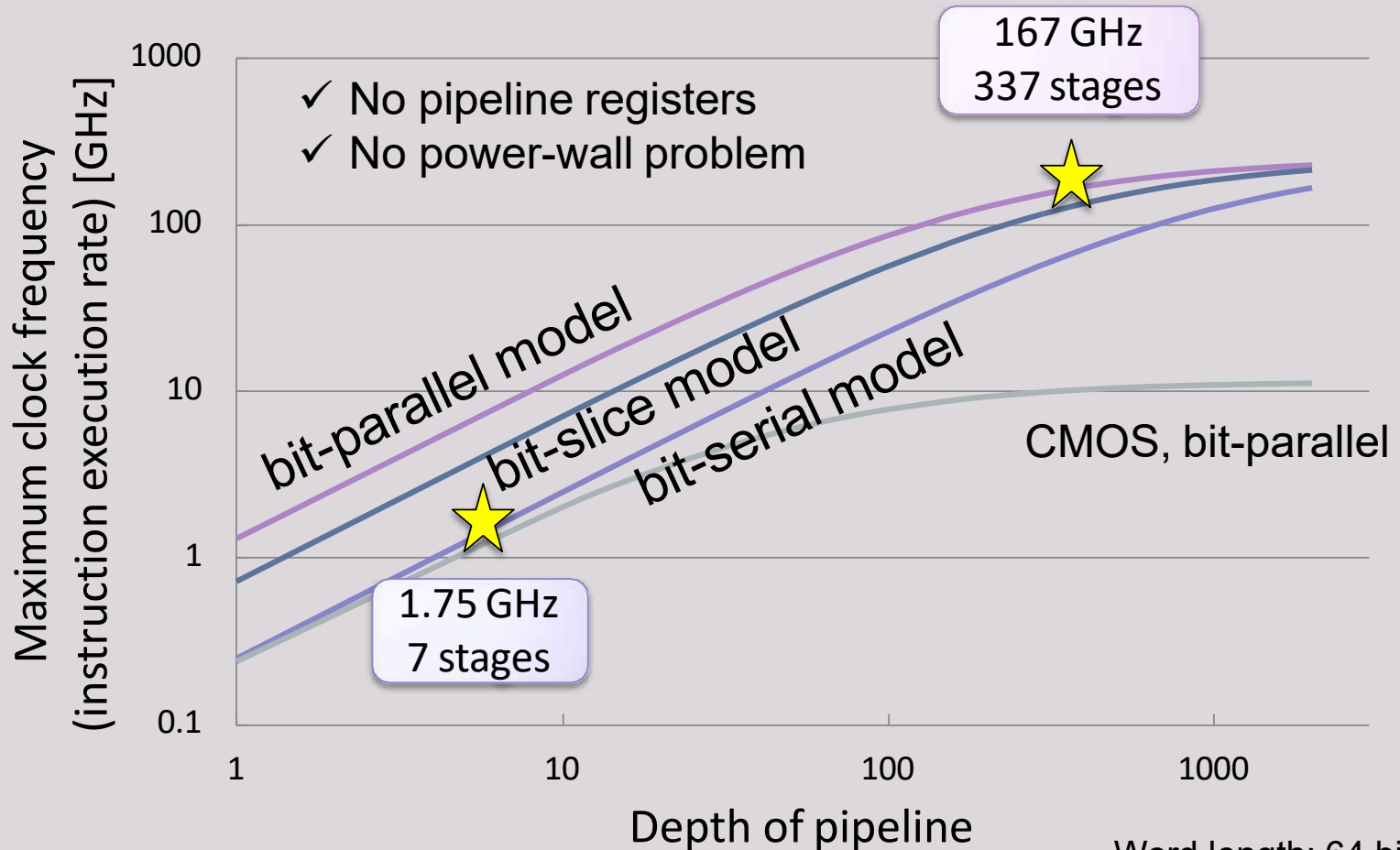
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# Revisiting Microarchitecture Design for More Powerful Computing

- Exploring architecture space optimized for RSFQ.
  - Bit-serial, bit-slice vs. bit-parallel processing
  - Depth of pipelines
  - How to eliminate pipeline hazards?



# Pipeline Depth vs. Clock Frequency



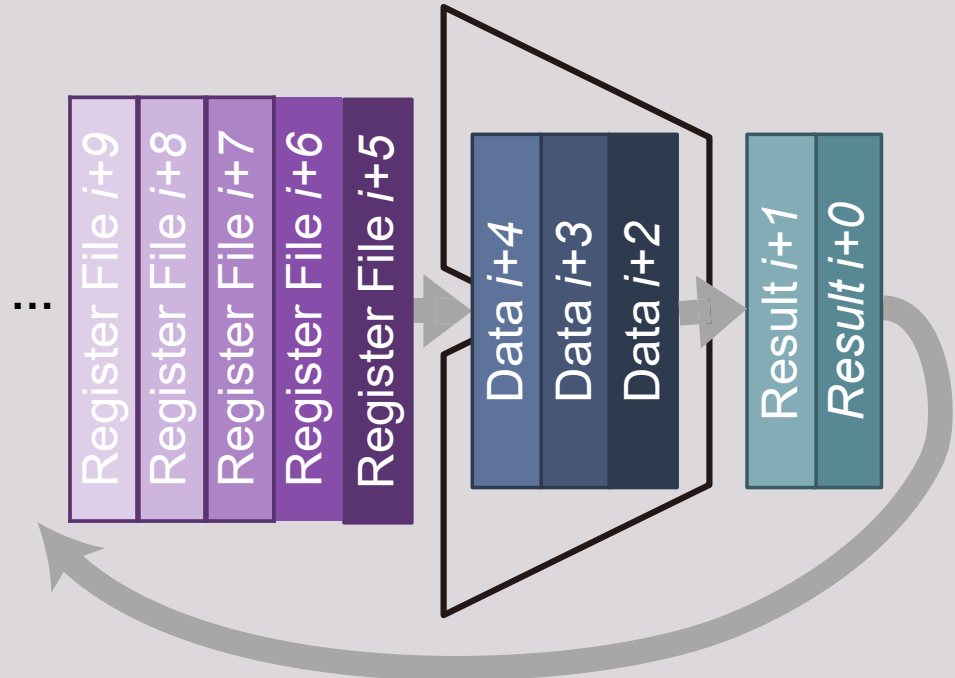
# Eliminating Pipeline Hazards

- Fine-grained multithreading
  - Number of threads = Number of pipeline stages

## Example:

$$\begin{pmatrix} ! & ! & ! & ! & ! & " \\ ! & " & ! & ! & " & " \end{pmatrix} \times \begin{pmatrix} \# \\ \# \end{pmatrix} = \begin{pmatrix} ! & ! & ! & \# & ! & + & ! & " & \# & " \\ ! & " & ! & \# & ! & + & ! & " & \# & " \end{pmatrix}$$

1 element → 1 thread



# Results of Architectural Optimization

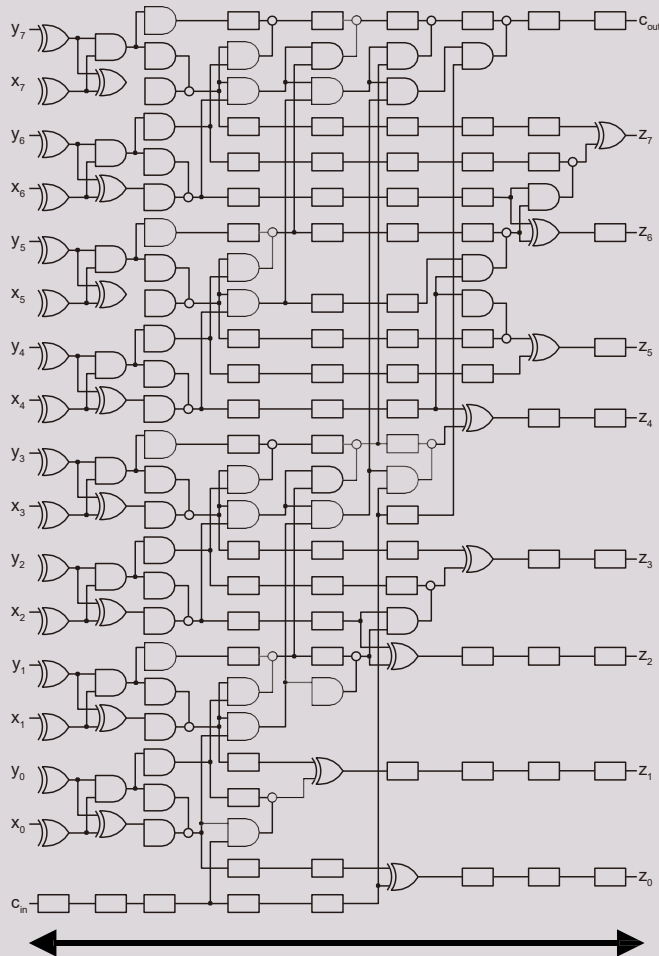
- Our approaches:

- Bit-parallel processing
- Ultra-deep (gate-level) pipelining
- Fine-grained multithreading

- We started development of throughput-oriented microprocessors with bit-parallel, gate-level-pipelined processing.
  - Challenges: hardware complexity and timing design

Can bit-parallel RSFQ circuits operate at very high clock frequencies?

# 8-bit ALU Design



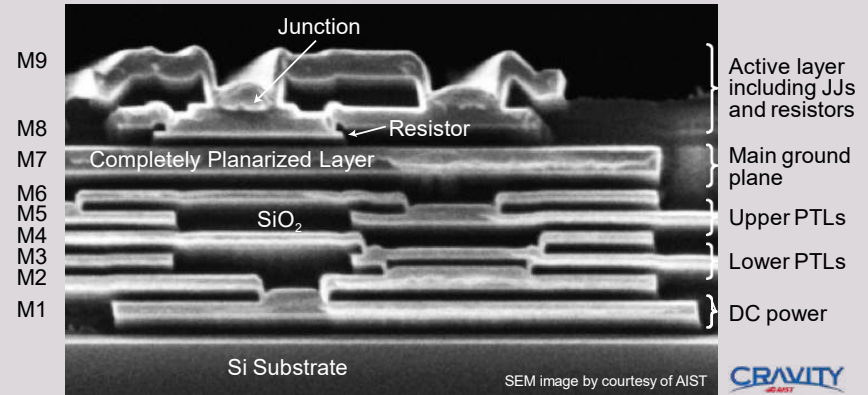
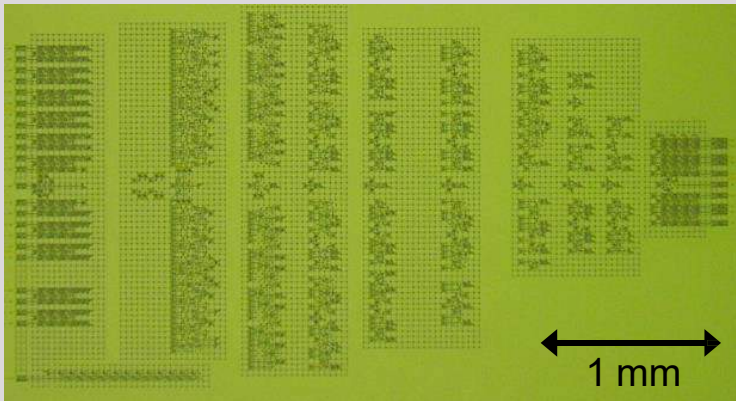
Number of pipeline stages: 9

- ✓ Target frequency: 50 GHz
- ✓ Gate-level pipelining
- ✓ Functions: ADD, SUB, AND, OR, XOR, NOR, etc.
- ✓ Data length: 8 bits

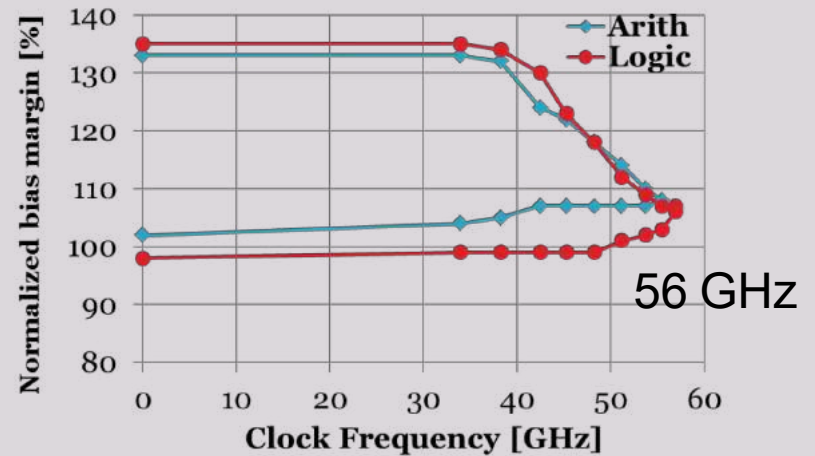
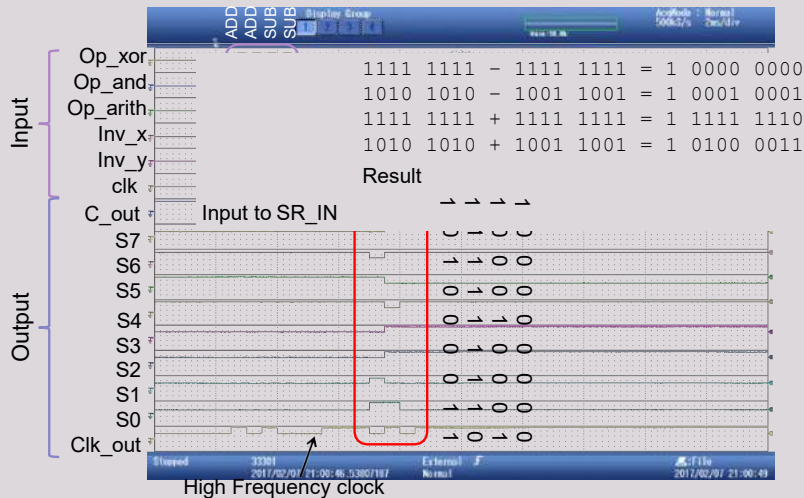
## Based on Brent-Kung adder

- Minimum number of logic gates (w/o D flip-flops)
- Sparse wiring tracks
- Small fanouts (Max. 3)
- Maximum logic depth

# Demonstration of Gate-Level-Pipelined ALU up to 56 GHz



S. Nagasawa et al. *IEICE Trans. Electron.* **E97-C** (2014) 132–140.



# Results of Architectural Optimization

- Our approaches:

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- Fine-grained multithreading

- We started development of throughput-oriented microprocessors with bit-parallel, gate-level-pipelined processing.

- Challenges: hardware complexity and timing design

Can bit-parallel RSFQ circuits operate at very high clock frequencies? **...YES**



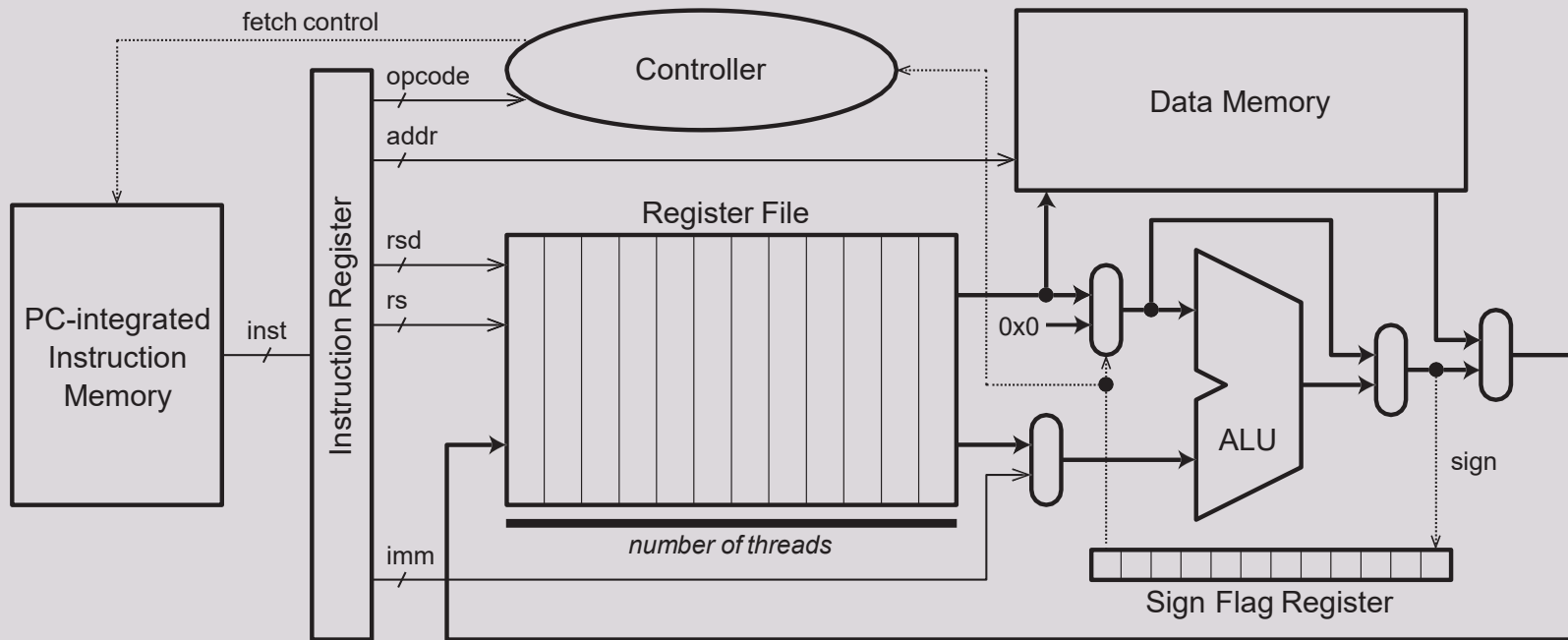
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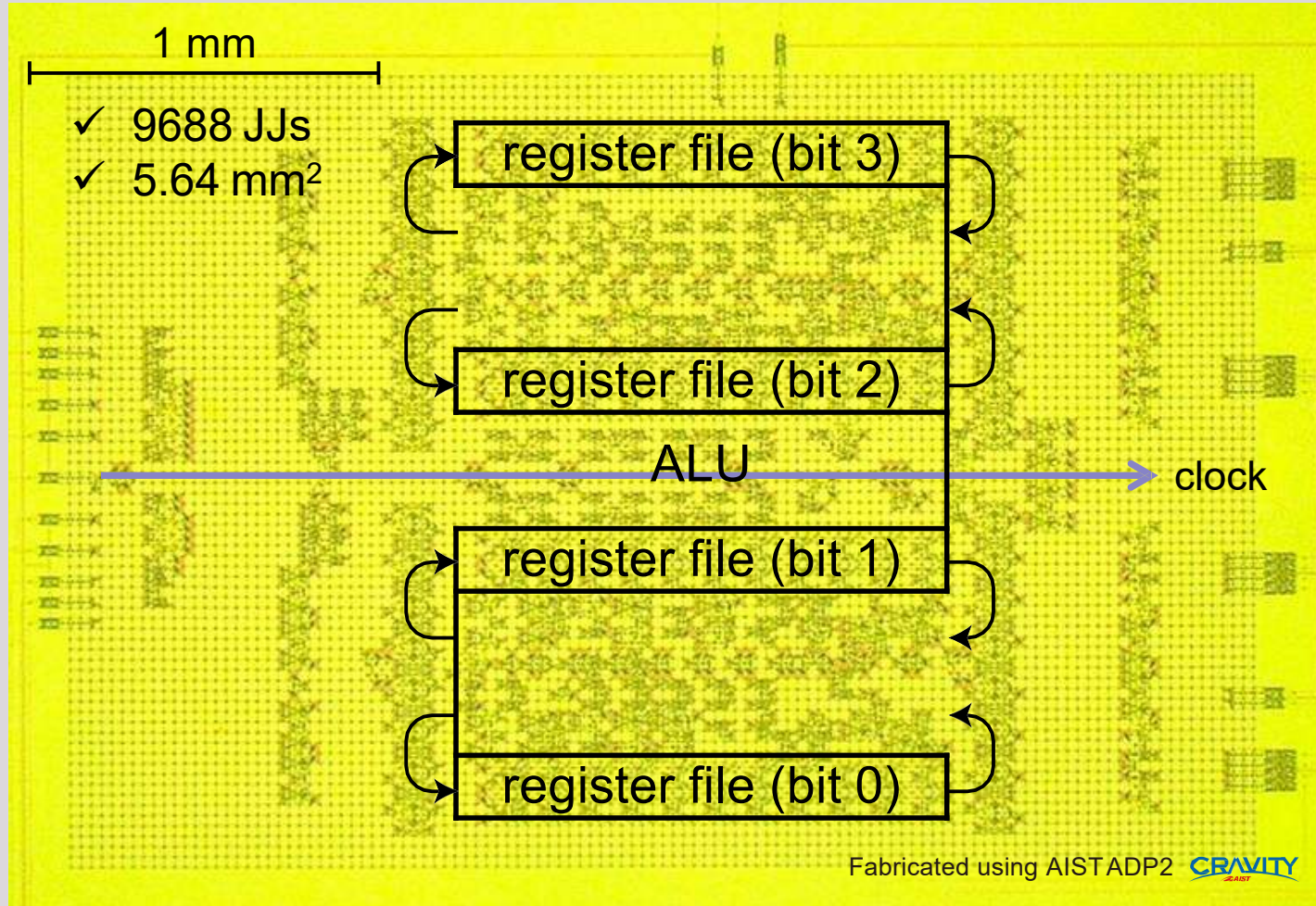
# Architectural Design of Gate-Level-Pipelined Microprocessor Prototype

- We designed 4-bit microprocessor prototype with 12-threads support.

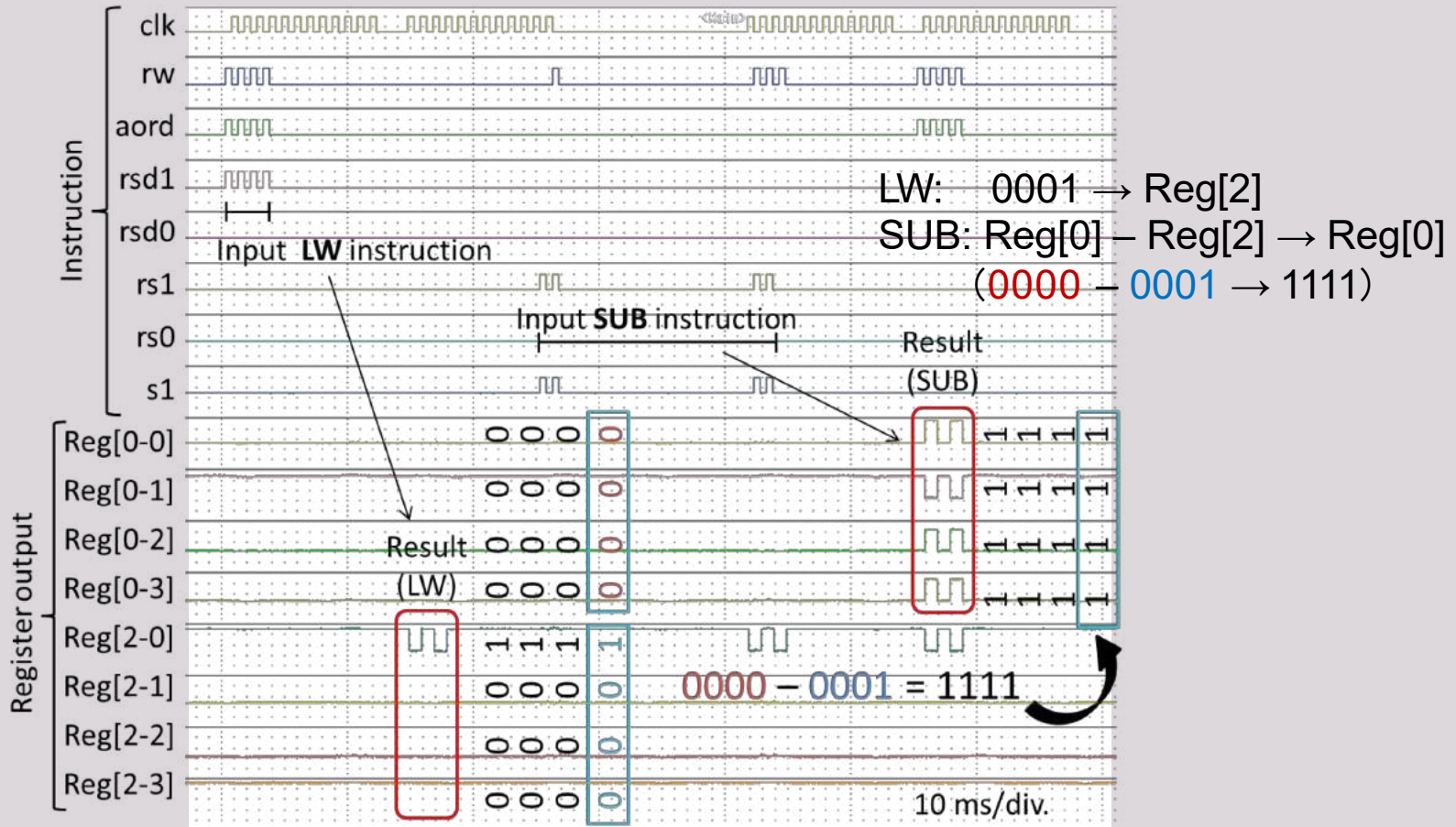
- ✓ 24 pipeline stages
- ✓ 12 threads (SIMT)
- ✓ 12 instructions



# Fabrication of Datapath Test Circuit

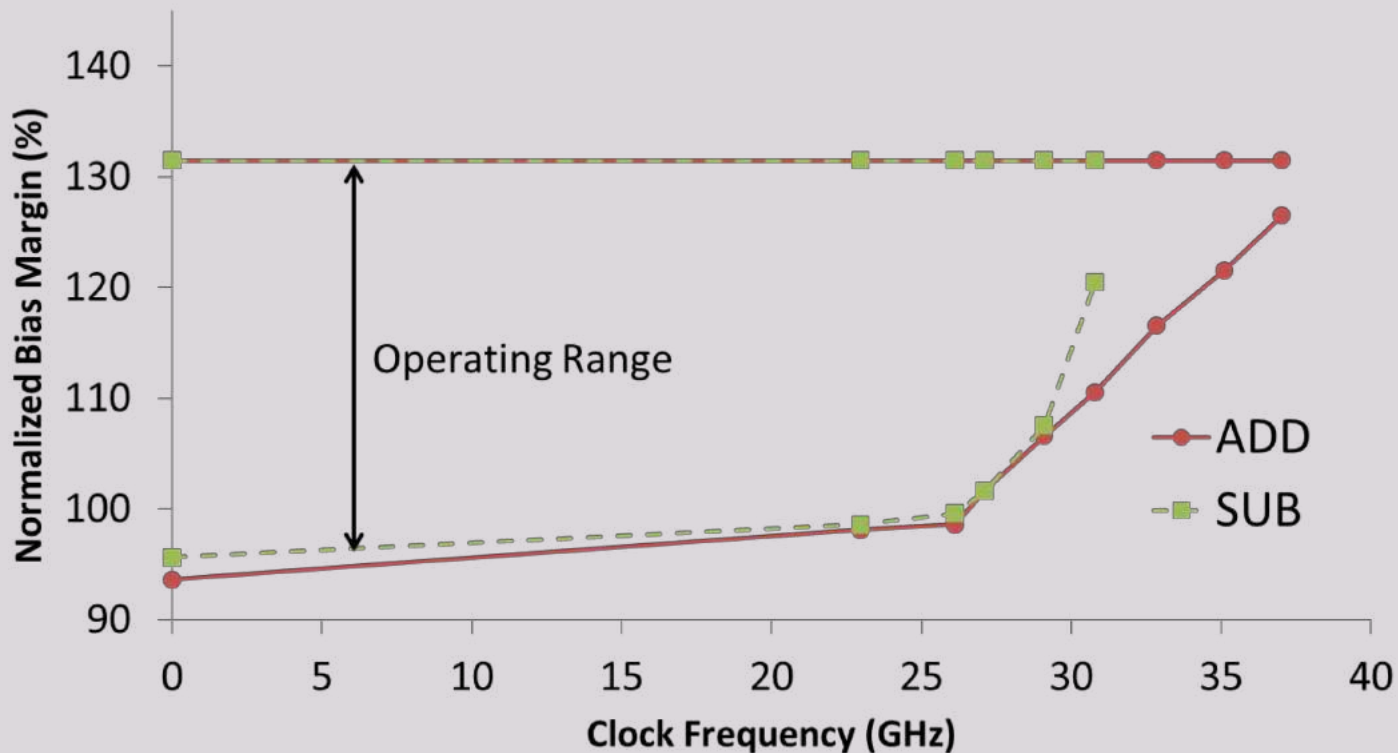


# Demonstration



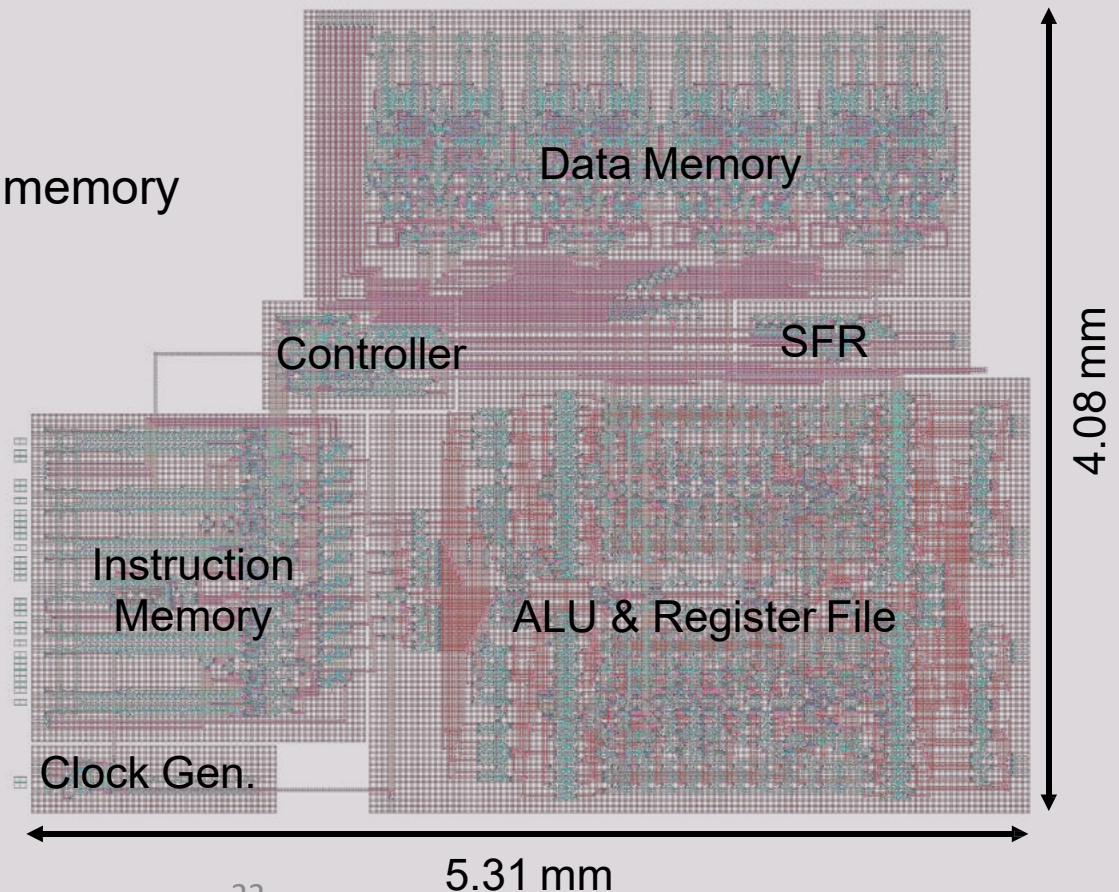
# High-Frequency Test Results

- We confirmed several successful gate-level-pipelined operations at high clock frequencies up to 31 GHz.



# Gate-Level-Pipelined Microprocessor Prototype

- ✓ 24 pipeline stages
- ✓ 12 threads, SIMT
- ✓ 12 x 10-bit instruction memory
- ✓ 4 x 4-bit register file
- ✓ 4 x 4-bit data memory
- ✓ 23,713 JJs
- ✓ Up to 31.3 GHz  
@6.9 mW



# Summary

- We designed and tested an RSFQ 4-bit datapath toward extremely high-throughput, bit-parallel microprocessors.
- Gate-level (ultra-deep) pipelining and fine-grained multi-threading will be a promising architectural approach for RSFQ-based high-performance computing.
- We demonstrated high-speed operation up to 31 GHz with power consumption of 2.5 mW. Introduction of energy-efficient techniques, such as LV-RSFQ or ERSFQ, will provide much better efficiency.
- Fabrication and testing of the prototype microprocessors including the designed datapath is ongoing.